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LR3617 Up/Down Counter LSI with LCD Decoder-Driver

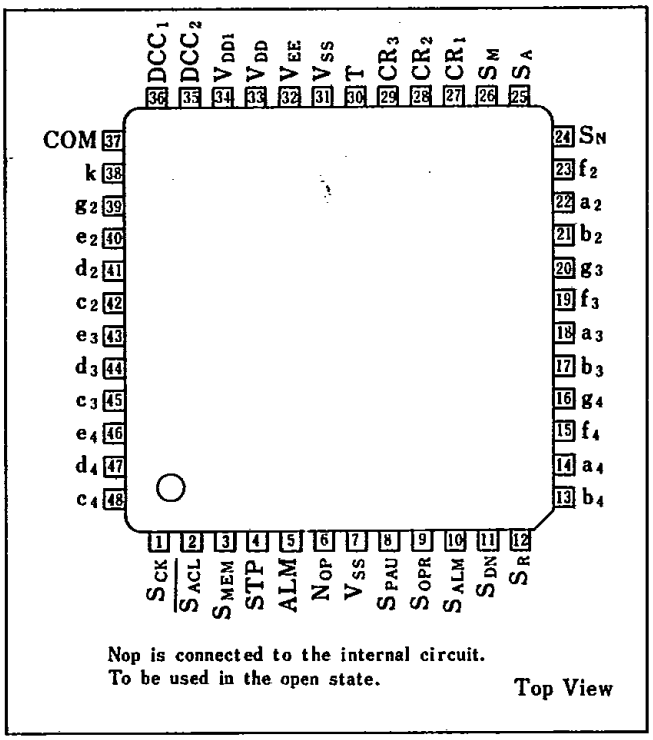
■ Description

The LR3617 is a CMOS up/down counter LSI with a decoder driver for $3^1/_2$ digit LCDs. It is best suited to tape counters for use in micro cassette tape recorders and VTRs.

■ Features

1. $3^1/_2$ digit static LCD
2. Leading zero suppression
3. Minus sign floating position
4. Memory stop
5. End-of-tape stop
6. Single power supply : − 1.5V
7. CMOS process
8. 48-pin quad-flat package

■ Pin Connections



Nop is connected to the internal circuit.
To be used in the open state.

Top View

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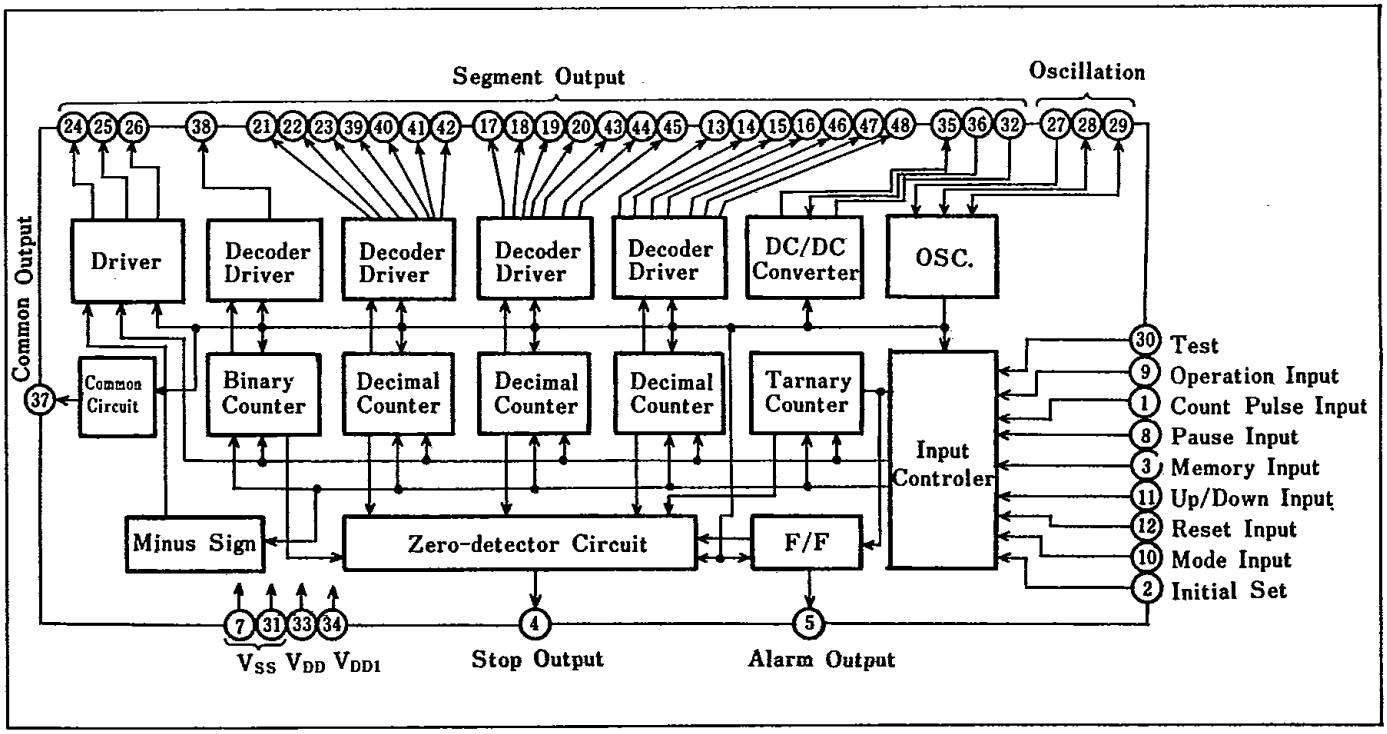
■ Block Diagram



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■ Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Note
Pin voltage*	V_{T1}	0.3 to −2.5	V	1
	V_{T2}	0.3 to −5.0	V	2
	V_{T3}	+0.2 to V_{DD}−0.2	V	3
Operating temperature	T_{opr}	−10 to +60	℃	
Storage temperature	T_{stg}	−55 to +150	℃	

*Referenced to Vss

Note 1: Applied to pins V_{DD} and V_{DD1}.
Note 2: Applied to V_{EE} pin.
Note 3: Applied to all input pins except V_{SS}, V_{EE}, V_{DD}, V_{DD1} pins.

■ Recommended Operating Conditions

Parameter	Symbol	Ratings	Unit	Note
Supply voltage*	V_{DD}, V_{DD1}	−1.3 to −1.8	V	1
Input voltage*	V_{IN}	0 to V_{DD}	V	2

Note 1: Do not allow a sudden change to occur even within the rated value.
Note 2: Applied to pins S_{CK}, S_{ACL}, S_{MEN}, S_{PAU}, S_{OPR}, S_{ALM}, S_{DN} and S_R.

■ Electrical Characteristics

($V_{DD}=V_{DD1}=-1.5V$, Ta=25℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Current consumption	$(I_{DD}+I_{DD1})$	All input pins V_{SS}, f_{OSC}=64kHz, with no load		13.5	25	μA	1
Input voltage	V_{IH}		−0.3			V	2
	V_{IL}				V_{DD}+0.3		
Input current	I_{IH}	$V_{IH}=0V$			5	μA	2
	I_{IL}	$V_{IL}=V_{DD}$			5		
CR oscillator frequency	f_{OSC}	R_1=5.1kΩ, R_2=150kΩ, C=47pF	32	48	64	kHz	3
Output current 1	I_{OH1}	$V_{OH}=-0.5V$, $V_{EE}=-3.0V$	10			μA	4
	I_{OL1}	$V_{OL}=-2.5V$, $V_{ER}=-3.0V$	10				
Output current 2	I_{OH2}	$V_{OH}=-0.5V$, $V_{ER}=-3.0V$	100			μA	5
	I_{OL2}	$V_{OL}=-2.5V$, $V_E=-3.0V$	100				
Output current 3	I_{OH3}	$V_{OH}=-0.4V$	10			μA	6
	I_{OL3}	$V_{OL}=-1.1V$	10				

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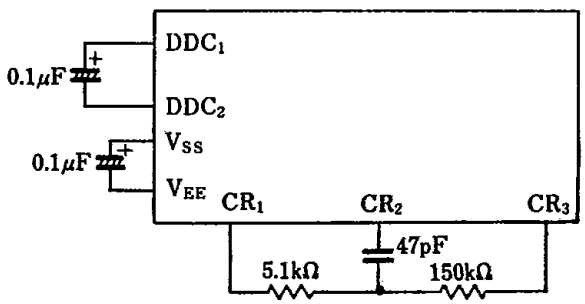
Note 1: Total power consumption at fosc=64kHz
All output pins open
All input pins connected to the Vss pin
V_{DD1} pin connected to V_{DD} pin
Note 2: Applies to all input pins except Vss, V_{DD1}, V_{DD}, V_{EE}, CR_1, CR_2, CR_3 pins
Note 3: The constant values shown in the right figure are used in the oscillation circuit.
Note 4: Applied to segment output pins
Note 5: Applied to common output pins
Note 6: Applied to pins STP and ALM



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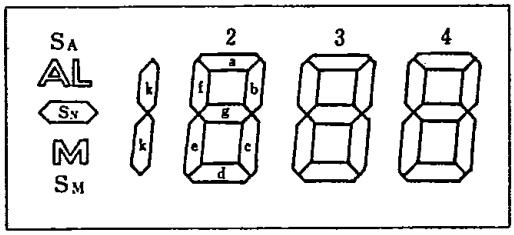
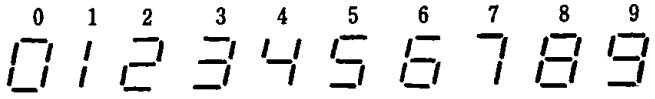
■ Sample Displays and Font





Sample display 1999

−120

−20

0

M30

■ Count Function

(1) Count range

Shown below are the count methods.

Up · count	Down · count
−1999	1999
↓	↓
−1998	1998
↓	↓
⋮	⋮
↓	↓
−2	2
↓	↓
−1	1
↓	↓
0 ←	0 ←
↓	↓
1	−1
↓	↓
2	−2
↓	↓
⋮	⋮
↓	↓
1998	−1998
↓	↓
1999	−1999

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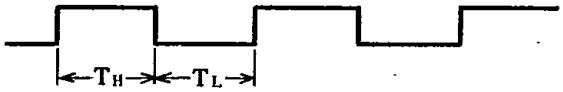
(2) Count input cycle

The count input signal waveform is as follows.



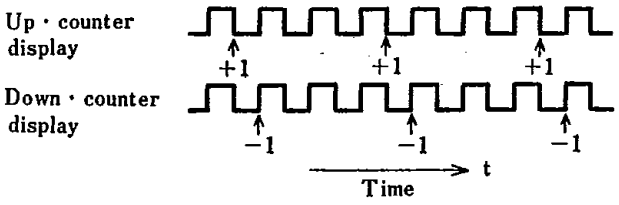
T_H : 5ms (MIN.), T_L : 5ms (MIN.)

(3) The relationship between count input, count content, and display

The LR3617 changes its display output each time 3 pulses get applied to the count input pin.

(4) Count input recognition

The LR3617 recognizes as one count pulse entered a transition that occurs in the up-counter mode when the counter input pin S_{CK} connected to V_{SS} is to be reconnected to V_{DD} (or open) or a transition that occurs in the down-counter mode when the count input pin S_{CK} connected to V_{DD} (or open) is to be reconnected to V_{SS}.



(5) Up/down input

The LR3617 works as a down-counter when the up/down input pin is connected to V_{SS}, and as an up-counter when the up/down input pin S_{DN} is connected to V_{DD} (or open).

With the stop signal output pin STP at V_{SS} level due to the tape end mode (discussed later) or the memory stop mode (discussed later) operation, when the up-down input pin S_{DN} connected to V_{DD} (or open) is to be reconnected to V_{SS}, the state of the stop signal output pin STP will be inverted to produce V_{DD} level output.

(6) Counter reset

Connecting the reset input pin S_R to V_{SS} resets the counter content to 0. Note that the counter does not operate with the reset input pin S_R connected to V_{SS}.

■ Memory Stop Mode

(1) Memory stop mode and its resetting

When the memory input pin S_{MEM} connected to V_{DD} (or open) is to be reconnected to V_{SS}, the memory stop mode will be entered, and M sign be displayed on LCD.

In memory stop mode, when the memory input pin S_{MEM} connected to V_{DD} (or open) is to be recon-

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nected to V_{SS}, the memory stop mode will be reset and the M display on the LCD will disappear. Altering the memory input pin S_{MEM} connection does not affect the counter content.

(2) Memory stop mode operation

When the counter content changes in memory stop mode from the value other than 0 to 0 (when 2 pulses are applied to the count input pin after the display has turned 0, in the case of display changing from 1 to 0, or when the display turns 0 in the case of display changing from −1 to 0), the stop signal output pin STP will produce V_{SS} level output. However, in the case of counter content change from the value other than 0 to 0 due to reset input S_R, the stop signal output pin STP will not go V_{SS} level and stays at V_{DD} level instead.

When the stop signal output pin STP produces V_{SS} level output due to the counter content change from the value other than 0 to 0, the memory stop mode will be reset and with it the M display on the LCD will disappear.

With the counter content at 0, the memory input pin S_{MEM} connected to V_{DD} (or open) is reconnected to V_{SS} to enter the memory stop mode.

And the stop signal output pin does not produce V_{SS} level output but stays at V_{DD} level.

The reset input S_R does not affect the memory stop mode.

The memory input pin S_{MEM} is always in effective operation as long as the LSI is supplied with power. The timing of the reset input S_R and the memory input S_{MEM} is as follows.

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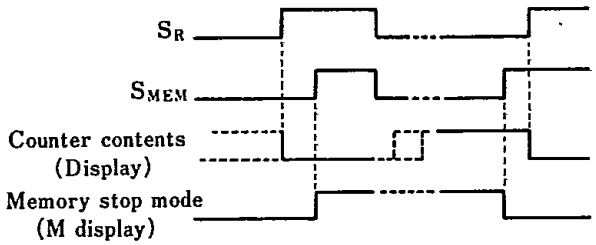


■ Tape End Detection Function

When no pulse has been applied to the counter input pin S_{CK} for 4～8 seconds with V_{SS} level input being applied to both the operation input pin S_{OPR}, and the pause input pin S_{PAU}, it will be decided that it is the tape end to be followed by the operations described below.

(1) Tape end stop mode

The tape end stop mode is a state in which the mode input pin S_{ALM} is connected to V_{DD} (or open). And when it is decided that it is the tape end, the stop signal output pin STP will produce V_{SS} level output. Changing the operation input pin S_{OPR} from V_{DD} to V_{SS} level with the stop signal output pin STP at V_{SS} level in the tape end stop mode, the state of the stop signal output pin will be inverted to produce V_{DD} level output.

(2) Tape end alarm mode

The tape end alarm mode will be entered when the mode input pin S_{ALM} is connected to V_{SS}. And if it is decided that it is the tape end, a 500～1000Hz pulse will be applied to the alarm signal output pin ALM.

When the operation input pin S_{OPR} is turned V_{DD} level with a 500～1000Hz pulse being applied to the alarm output pin ALM in the tape and alarm mode, the alarm signal output pin ALM produces V_{DD} level output. However with the STP at V_{SS} level output, the ALM output is disabled.

(3) Operation input (S_{OPR})

When the tape recorder is in PLAY, RECORD, FF, REW, CUE, REVIEW state, or in operation, V_{SS} level input is applied. And when the tape recorder is out of operation, V_{DD} level input is applied.

(4) Pause input (S_{PAU})

To be connected to V_{SS} when the tape recorder is in normal operation, or to be connected to V_{DD} (or open) when the tape recorder is out of operation or in the pause state.

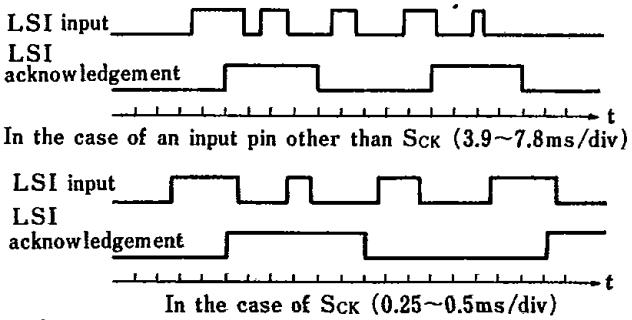
When no pulse has been applied to the count input pin S_{CK} for 4～8 seconds with the pause input pin connected to V_{DD} (or open), nor is it decided that it is the tape end.

(5) Tape end alarm display

Tape end alarm mode allows for the mode indication in LCD static display.

(6) Chatter killer

The LR3617 has its operation input pin S_{OPR}, pause input pin S_{PAU}, mode input pin S_{ALM}, up-down input pin S_{DN}, memory input pin S_{MEM}, reset input pin S_R, and count input pin S_{CK} equipped with built-in chatter killers, the timing of which is shown in the figure below.



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(7) Initial set

By connecting the initial set input pin $\overline{S_{ACL}}$ to V_{DD}, the internal LSI and each output will be initialized as follows.

Counter display 0

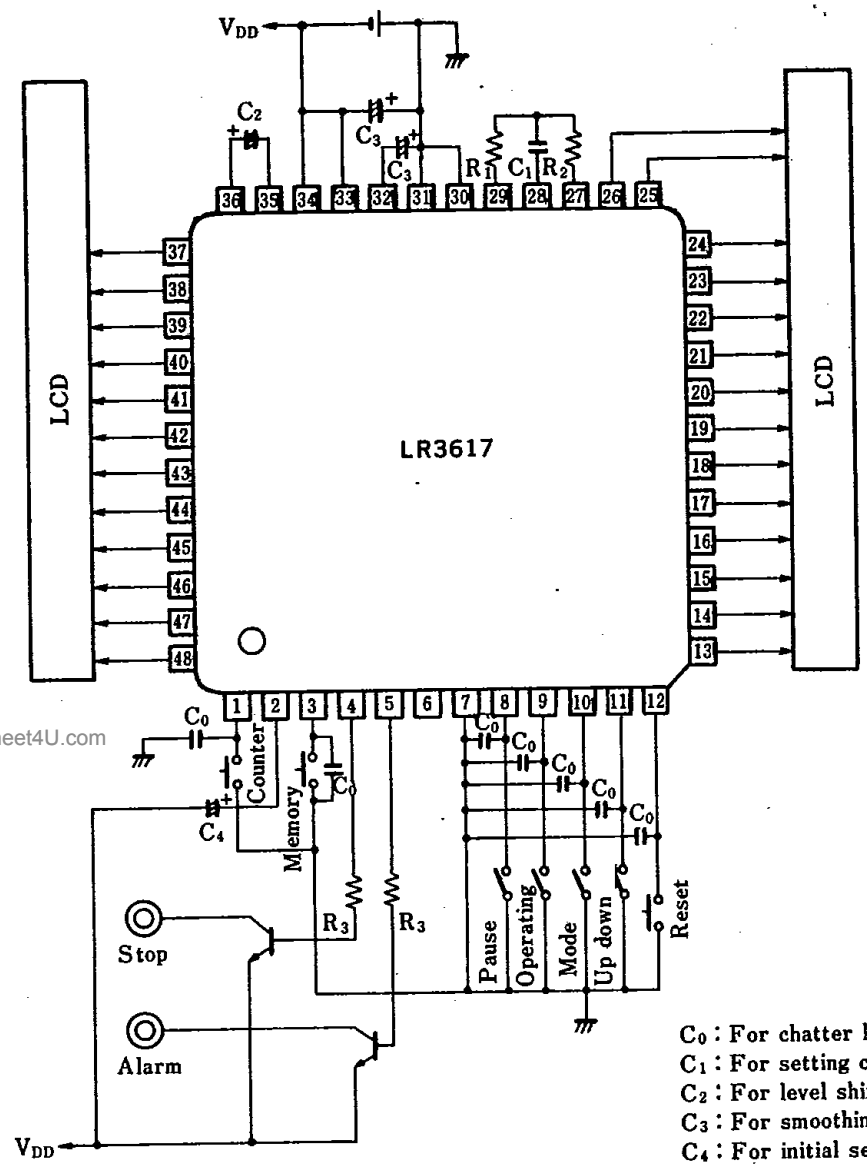
Memory stop function reset (therefore no M display)

Stop signal output pin STP V_{DD} level output

Alarm signal output pin ALM V_{DD} level output

The LSI retains the state as described above with the initial set input pin $\overline{S_{ACL}}$ connected to V_{DD}.

■ System Configuration Example



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C_0 : For chatter killer of input signal
C_1 : For setting clock frequency
C_2 : For level shift coupling
C_3 : For smoothing after level shift
C_4 : For initial set
C_5 : For power supply hold
R_1 : For setting frequency
R_2 : } For regulating current
R_3 : }