SHARP

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To ;

S P E C I F I C A T I O N S

Product Type Signal processing LSI for 270,000-470,000 pixel CCD

Model No. LR36B15

※These specifications contain 36 pages including the cover and appendix.
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DATE:

BY:

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SHARP CORPORATION
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Sep 22 2011
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Table of contents

1. Description

This product is the LSI equipped with the AFE block contain CDS, PGA and ADC, drive timing pulse generator of the 270-thousand to 470-thousand pixels CCD area sensor, each pulse generator for the television signal, the signal processing function for converting to the video signal from the CCD image converted to digital signal and 75ohm video amplifier contains LPF.

・Features

■ AFE for CCD

- 12bit AD convertor with CCD I/F
- CDS of 1Vpp input range
- Input clamping circuit
- PGA of gain range from -3dB to 36dB
- Black level calibration circuit

■ Timing generator for CCD (TG)

- It corresponds to the CCD of 270-thousand and 410-thousand pixels for NTSC, 320-thousand 470-thousand pixels for PAL.

■ Image signal processor (ISP)

- The automatic exposure control function is equipped.
- The automatic white balance control function is equipped.
- The automatic carrier balance equalizer function is equipped.
- The line crawl compensation function is equipped.
- The white blemish compensation function is equipped.
- The gamma correction functions for brightness signal and the color signal are equipped independently.
- Lens shading compensation function is equipped.
- It has the output of the DC IRIS control.
- 50Hz flicker suppression function is equipped.

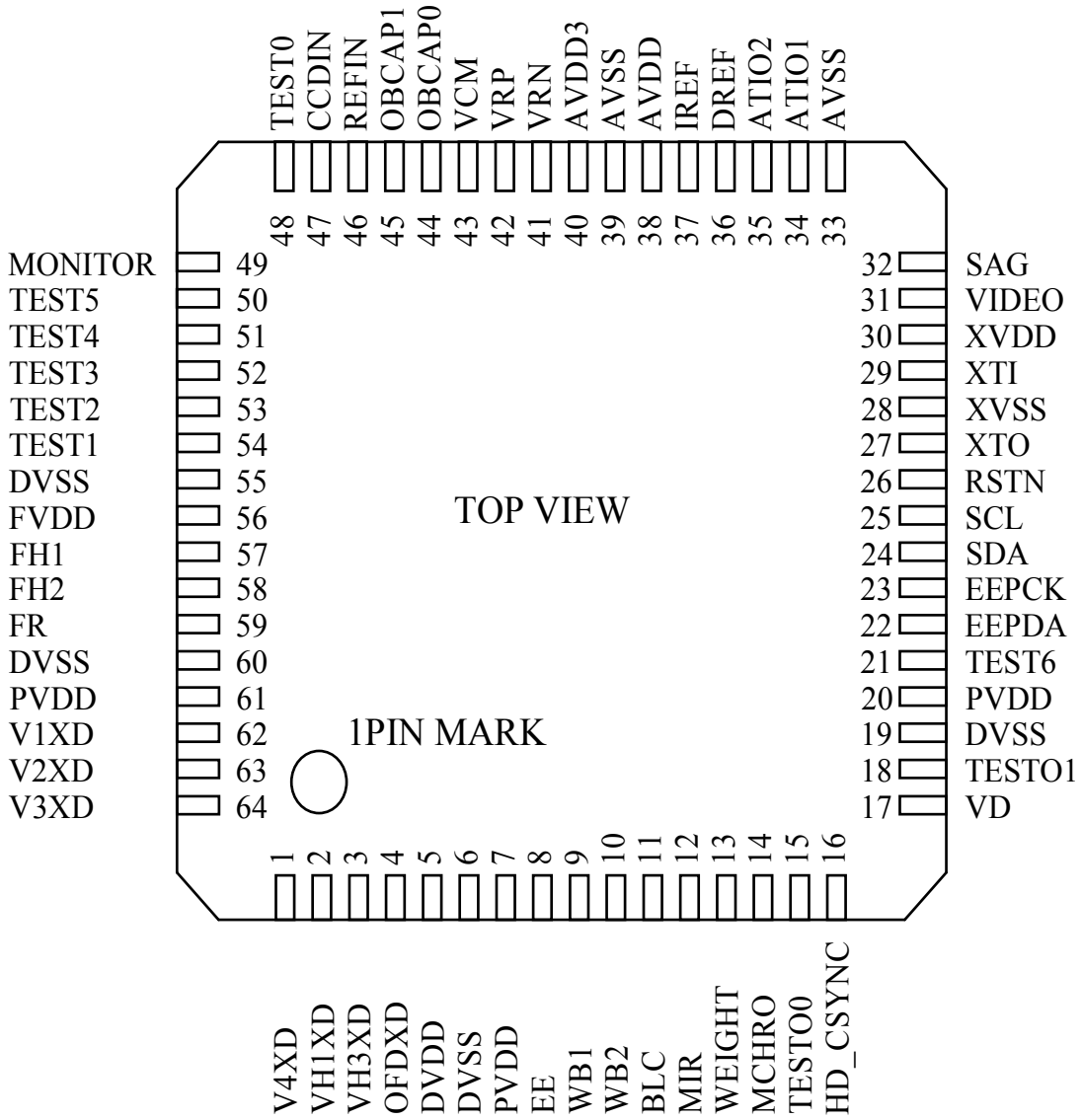
■ Video encoder

- Correspond to NTSC-M, PAL-BDG video format.
- Support standard composite video format.
- 10-bit DA convertor is equipped.
- 75-ohm drive amplifier of 6dB gain with LPF is equipped.
- SAG correction function is equipped.

■ Others

- 4K bit EEPROM Read/Write function for the adjustment parameter storage.
  (LR36B15 needs EEPROM which has 16 or more bytes page access feature).
- Host interface is dedicated 2-wired serial interface.
- 1.8V linear regulator is equipped. (3.3V single power supply)
- NTSC:28.63636MHz / PAL:28.375MHz crystal oscillator is equipped.
- Small QFN package (HQFN64-P-0909-0.5, Pb free, Halogen free)
- Operation temperature : -30 to 85 °C

2. Pin Assignment



3. Pin Description

No.	Name	PS (*1)	I/O type (*2)	Function
1	V4XD	P	O_2	Vertical CCD clocking pulse. Connect to V-driver. Output high at reset.
2	VH1XD	P	O_2	Pixel transfer gate pulse. Connect to V-driver. Output high at reset.
3	VH3XD	P	O_2	Pixel transfer gate pulse. Connect to V-driver. Output high at reset.
4	OFDXD	P	O_2	OFD(Over Flow Drain) pulse. Connect to V-driver. Output high at reset.
5	DVDD	D	—	LDO decoupling terminal for internal digital circuit power supply. Connect 2.2μF capacitor between DVSS.
6	DVSS	P	—	Ground terminal.
7	PVDD	P	—	Power supply for digital I/O buffer. (3.3V)
8	EE	P	IO_2	Fixed speed of an electrical shutter mode selection terminal
9	WB1	P	IO_2	Fixed white balance mode setting terminal 1.
10	WB2	P	IO_2	Fixed white balance mode setting terminal 2.
11	BLC	P	IO_2	Backlight compensation mode selection terminal.
12	MIR	P	IO_2	Mirror mode selection terminal.
13	WEIGHT	P	IO_2	AE weight parameter selection terminal.
14	MCHRO	P	IO_2	Color suppression mode selection terminal.
15	TESTO0	P	O_2	Test terminal. Please do not connect it anywhere.
16	HD_CSYNC	P	IO_2	Horizontal synchronous signal or composite synchronous signal output terminal. Output low at reset.
17	VD	P	IO_2	Vertical synchronous signal output terminal. Output low at reset.
18	TESTO1	P	O_2	Test terminal. Please do not connect it anywhere.
19	DVSS	P	—	Ground terminal.
20	PVDD	P	—	Power supply for digital I/O buffer. (3.3V)
21	TEST6	P	IS	Test mode setting terminal. Connect to DVSS. (Pull-down)
22	EEPDA	P	IOS_3	EEPROM serial data I/O terminal. Connect data terminal of EEPROM with pull-up resister.(*3)
23	EEPCK	P	O_3	EEPROM serial clock output terminal. Connect clock terminal of EEPROM with pull-up resister. (*3)
24	SDA	P	IOS_3	Data input terminal from the external host to adjust camera parameters. (*3)

No.	Name	PS (*1)	I/O type (*2)	Function
25	SCL	P	IS	Clock input terminal from the external host to adjust camera parameters.
26	RSTN	P	IS	Reset signal input terminal. L : Reset / H : Normal operation Hi-Z condition is forbidden for this terminal.
27	XTO	X	OSC_O	Clock oscillator output. CKI and CKO make oscillator circuit.
28	XVSS	X	—	Ground terminal.
29	XTI	X	OSC_I	Clock oscillator input. Crystal oscillator's frequency (NTSC:28.63636MHz PAL:28.375MHz)
30	XVDD	X	-	Power supply for analog circuit. (3.3V)
31	VIDEO	X	O_A	Video signal output terminal. Refer to 7.1 video amplifier frequency characteristics for connection with SAG terminal.
32	SAG	X	O_A	SAG correction control terminal. Refer to 7.1 video amplifier frequency characteristics for connection with VIDEO terminal.
33	AVSS	X	-	Ground terminal.
34	ATIO1	X	O_A	Analog I/O for testing. Connect to AVSS.
35	ATIO2	X	O_A	Analog I/O for testing. Connect to AVSS.
36	DREF	A3	O_A	Reference voltage for DAC decoupling terminal. Connect 1μF capacitor between AVSS. Output low at reset.
37	IREF	A3	O_A	Bias current for internal analog circuit output terminal. Connect 8.2kΩ resister between AVSS. Output Hi-Z at reset.
38	AVDD	A3	—	LDO decoupling terminal for internal analog circuit power supply. Connect 2.2μF capacitor between DVSS.
39	AVSS	A3	—	Ground terminal.
40	AVDD3	A3	—	Power supply for analog circuit. (3.3V)
41	VRN	A3	O_A	Reference voltage for ADC decoupling terminal. Connect 1μF capacitor between VRP and connect 1μF capacitor between AVSS. Output Hi-Z at reset.
42	VRP	A3	O_A	Reference voltage for ADC decoupling terminal. Connect 1μF capacitor between VRN and connect 1μF capacitor between AVSS. Output Hi-Z at reset.
43	VCM	A3	O_A	Common voltage for ADC decoupling terminal. Connect 1μF capacitor between AVSS. Output Hi-Z at reset.
44	OBCAP0	A3	O_A	Black level integrated voltage output terminal. Connect 1μF capacitor between AVSS. Output Hi-Z at reset.
45	OBCAP1	A3	O_A	
46	REFIN	A3	I_A	Reference signal input terminal. Connect 1μF capacitor between AVSS.
47	CCDIN	A3	I_A	CCD signal input terminal.
48	TEST0	A3	I_A	Test mode setting terminal. Connect to AVSS. (Pull-down)

No.	Name	PS (*1)	I/O type (*2)	Function
49	MONITOR	A3	O_A	Monitor signal output terminal for DC IRIS. Output Hi-Z at reset.
50	TEST5	F	I	Test mode setting terminal. Connect to DVSS. (Pull-down)
51	TEST4	F	I	Test mode setting terminal. Connect to DVSS. (Pull-down)
52	TEST3	F	I	Test mode setting terminal. Connect to DVSS. (Pull-down)
53	TEST2	F	I	Test mode setting terminal. Connect to DVSS. (Pull-down)
54	TEST1	F	I	Test mode setting terminal. Connect to DVSS. (Pull-down)
55	DVSS	F	—	Ground terminal.
56	FVDD	F	—	Power supply for CCD horizontal driver. (3.3V)
57	FH1	F	O_16	Horizontal CCD's driving pulse. Connect to CCD. (Several CCD may need level converter) Output Hi-Z at reset.
58	FH2	F	O_16	Horizontal CCD's driving pulse. Connect to CCD. (Several CCD may need level converter) Output Hi-Z at reset.
59	FR	F	O_8	Output gate resetting pulse. Connect to CCD via capacitor. Output Low at reset.
60	DVSS	P	—	Ground terminal.
61	PVDD	P	—	Power supply for digital I/O buffer. (3.3V)
62	V1XD	P	O_2	Vertical CCD clocking pulse. Connect to V-driver. Output high at reset.
63	V2XD	P	O_2	Vertical CCD clocking pulse. Connect to V-driver. Output high at reset.
64	V3XD	P	O_2	Vertical CCD clocking pulse. Connect to V-driver. Output high at reset.

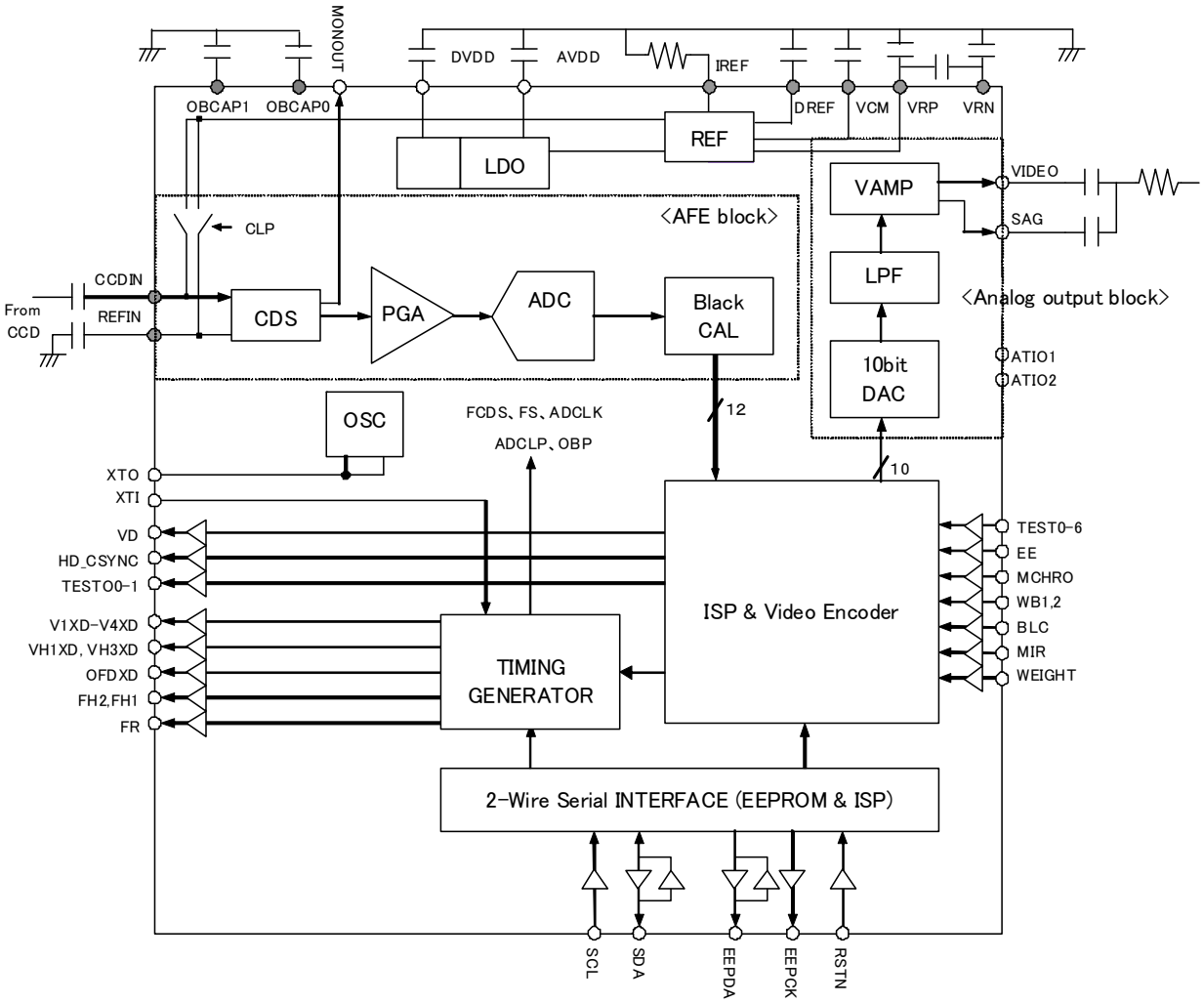
(*1) D means DVDD, A3 means AVDD3, X means XVDD, P means PVDD, F means FVDD

(*2) I/O type is as follows;

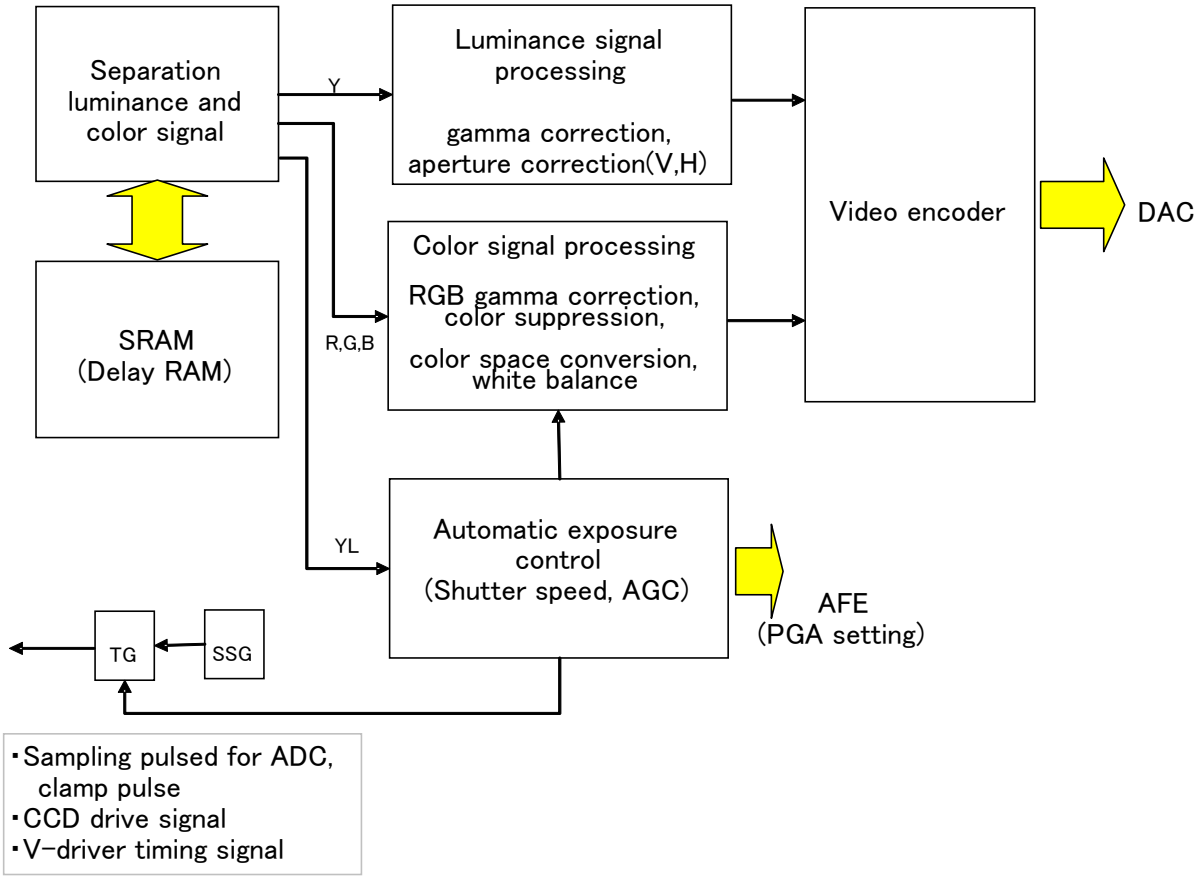
(*3) Decide pull-up resister value to meet the condition that the sink current 3mA at VOL=0.4V.

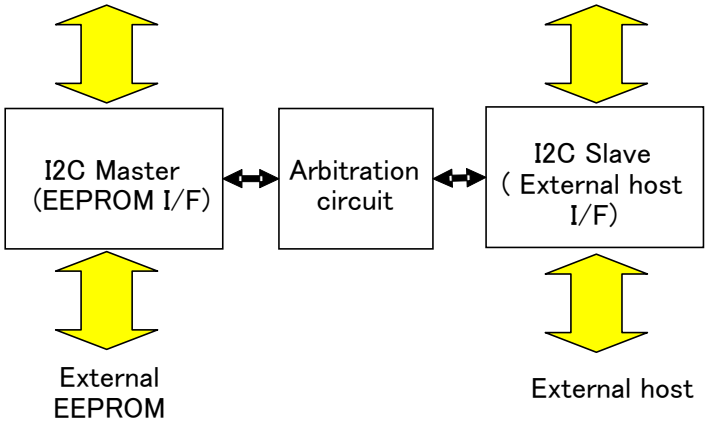
Symbol	I/O type
IS	Schmidt level input terminal
I	CMOS level input terminal
I_D	CMOS level input terminal (pull-down resister contained)
I_A	Analog input terminal
IO_2	Input and output terminals CMOS level input Capable output current is 2mA (when the power is 3.3V)
IO_A	Analog input and output terminal
IOS_3	Input and output terminals schmidt level input Capable output current is 3mA (when the power is 3.3V)
O_2	Output terminals Capable output current is 2mA. (when the power is 3.3V)
O_3	Output terminals Capable output current is 3mA. (when the power is 3.3V)
O_8	Output terminals Capable output current is 8mA. (when the power is 3.3V)
O_16	Output terminals Capable output current is 16mA. (when the power is 3.3V)
O_A	Analog output terminal
OSC_I	Input terminal for the oscillation circuit
OSC_O	Output terminal for the oscillation circuit

4. Block Diagram



Detail block diagram of ISP and video encoder block





5. Electrical characteristics

5.1. Absolute maximum ratings

Parameter	Symbol	Min.	Max.	Units	Notes
Power voltages for digital I/O	PVDD	-0.3	4.3	V	
Power voltages for CCD horizontal driver	FVDD	-0.3	4.3	V	
Power voltages for analog circuit1	AVDD3	-0.3	4.3	V	
Power voltages for analog circuit2	XVDD	-0.3	4.3	V	
External voltages for DVDD terminal (*1)	DVDD	-0.3	2.3	V	
External voltages for AVDD terminal (*1)	AVDD	-0.3	2.3	V	
Input voltages for digital I/O terminals (*2)	VIP	-0.3	PVDD+0.3 or 4.3V	V	
Analog input voltages 1 (*3)	VIA3	-0.3	AVDD3+0.3 or 4.3V	V	
Analog input voltages 2 (*4)	VIX	-0.3	XVDD+0.3 or 4.3	V	
Output voltages for digital I/O terminals (*5)	VOP	-0.3	PVDD+0.3 or 4.3V	V	
Output voltages for CCD horizontal drivers (*6)	VOF	-0.3	FVDD+0.3 or 4.3V	V	
Analog output voltages 1 (*7)	VOA3	-0.3	AVDD3+0.3 or 4.3V	V	
Analog output voltages 2 (*8)	VOX3	-0.3	XVDD+0.3 or 4.3	V	
Storage temperature	TSTG	-65	150	℃	

(Note) Exceeding any of the above limiting values may result in permanent device damage.
Normal function will not be guaranteed after any the above limiting values is exceeded.

(*1) Regulator output terminal.
When the voltage that is higher than maximum value is forced, this LSI will be reset.

(*2) Applied to PVDD power supplied input terminals (I, IS) and I/O terminals (IO_2).

(*3) Applied to AVDD3 power supplied input terminals.

(*4) Applied to XVDD power supplied input terminals.

(*5) Applied to PVDD power supplied output terminals (O_2) and I/O terminals (IO_2).

(*6) Applied to FVDD power supplied output terminals (O_8, O_16).

(*7) Applied to AVDD3 power supplied output terminals.

(*8) Applied to XVDD power supplied output terminals.

5.2. Recommended operating conditions

Parameters	Symbol	Min.	Typ.	Max.	Units	Notes
Digital I/O power supply voltage	PVDD	3.15	3.3	3.6	V	PVDD=FVDD= AVDD3=XVDD
CCD horizontal driver power supply voltage	FVDD	3.15	3.3	3.6	V	
Analog power supply voltage1	AVDD3	3.15	3.3	3.6	V	
Analog power supply voltage2	XVDD	3.15	3.3	3.6	V	
Input clock	CKI	10	28.636 (*1) 28.375 (*2)	30	MHz	(*1) NTSC (*2) PAL
Operating temperature	Ta	-30	25	85	℃	

(Note) Power supply voltages are based on each ground terminal levels.

All of the ground terminals should be same level. (AVSS=DVSS=XVSS=0V).

5.3. DC characteristics

(PVDD=FVDD=3.15~3.6V, DVSS=0V, Ta=-30~85℃)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Hi leval digital input voltage 1 (*1)	VIH1	0.8PVDD			V	
Lo level digital input voltage 1 (*1)	VIL1			0.2PVDD	V	
Hysteresis voltage (*2)	VHIS	0.05PVDD			V	
Digital output Hi voltage 1 (*3)	VOH1	0.8PVDD			V	IOH= -2mA
Digital output Lo voltage 1 (*3)	VOL1			0.2PVDD	V	IOL= 2mA
Digital output Hi voltage 2 (*4)	VOH2	0.8FVDD			V	IOH= -8mA
Digital output Lo voltage 2 (*4)	VOH2			0.2FVDD	V	IOL= 8mA
Digital output Hi voltage 3 (*5)	VOH3	0.8FVDD			V	IOH= -16mA
Digital output Lo voltage 3 (*5)	VOH3			0.2FVDD	V	IOL= 16mA
EEPCK, EEPDA, SDA Lo output voltage	VOLC			0.4	V	IOLC=3mA
Digital input Hi leakage 1 (*1)	IHL1	-10		10	uA	VIN=PVDD
Digital input Lo leakage 1 (*1)	ILL1	-10		10	uA	VIN=0 V

(*1) EE, WB1,2, BLC, MIR, WEIGHT, MCHRO, EEPDA, SCL, SDA, RSTN

(*2) SDA, SCL, EEPDA

(*3) V1XD~V4XD, VH1XD, VH3XD, OFDXD, HD_CSYNC, VD

(*4) FR

(*5) FH1, FH2

5.4. Analog characteristics

5.4.1. AFE block

(Conditions : AVDD3=XVDD=3.3V, AVSS=0V, Ta=25℃)

(Unless otherwise specified: ADC sampling frequency = 15MHz, Input frequency = 1MHz, Input level = 1.0Vpp)

Parameter	Min.	Typ.	Max.	Units	Conditions
Input range (*1)	0.8	1.0		Vpp	Measured downward from clamp voltage. With settings of black level code = 0, PGA gain = 0dB.
Input bandwidth		1		pixel	CCDIN ~ ADC ADC settling time for step input of full scale -2dB. With setting of PGA gain = 0dB.
Clamp voltage	1.3	1.4	1.5	V	CCDIN and REFIN terminal voltage in CLP active.
VRP voltage	1.3	1.4	1.5	V	
VRN voltage	0.4	0.5	0.6	V	
PGA minimum gain PGA maximum gain PGA resolution	-4.1 35.4 0.0	-3.1 36.4 0.05	-2.1 37.4 0.10	dB dB dB	Value relative to 0dB setting.
Black calibration bandwidth (Time Constant) (*2)					At sampling frequency = 15MHz
		547		us	With setting of x1 (default)
		0.13		us	With setting of x4096

(*1) CCDIN input level when ADC output reaches FFFh.

(*2) Black calibration bandwidth can be set from x1 to x4096, 12steps by register setting.

And it will be change according to operation frequency as follows,

τ [sec] ≡ 8200 / (Fs [Hz] x (speed setting))

Parameter	Min.	Typ.	Max.	Units	Conditions
MONITOR output gain (*3)	-2	0	+2	dB	REFIN, CCDIN ~ MONOUT
MONITOR output bandwidth (*4)		-7		dB	WINDOW = L (internal signal), (*6) Amplitude difference between input frequency is 190k and 1MHz
		-1		dB	WINDOW = H (internal signal), Amplitude difference between input frequency is 1M and 4MHz
ADC Resolution			12	bit	(*5)
ADC diff. nonlinearity			+3 / <-2.0	LSB	
ADC Integ. nonlinearity		±1.5	±6	LSB	
AFE total Noise (*6)		0.9 2.2 8.4		LSB rms LSB rms LSB rms	With setting of PGA gain = 0dB With setting of PGA gain = 18dB With setting of PGA gain = 30dB

(*3) Amplitude difference between MONITOR terminal output and CCDIN terminal input sine wave ingredient signal. With load of CL=30pF to MONITOR terminal.

(*4) Monitor terminal output amplitude difference between two input frequencies.
With load of CL=30pF to MONITOR terminal.

(*5) Guarantee no missing code in 11bit precision. Range of from -255 to 4095.

(*6) “WINDOW” is internal signal generated in ISP block.
Set with following registers WIN_PS (01E[7:0]), WIN_PE (083[7:0]), WIN_LS (0A7[7:0]) and WIN_LE(0FD[7:0]). Fixed Lo in Default.

5.4.2. Analog output block

(Conditions : AVDD3=XVDD=3.3V, AVSS=0V, Ta=25℃)

(Unless otherwise specified: DAC sampling frequency = 28MHz)

Parameter	Min.	Typ.	Max.	Units	Conditions
DAC resolution		10		bit	
DAC diff. nonlinearity		±0.6	±2.0	LSB	(*1)
DAC integ. nonlinearity		±0.4	±1.0	LSB	(*1)
Video amplifier output gain	5.0	6.0	7.0	dB	Amplifier input level = 1Vpp (*2)
Video amplifier full scale voltage		2.0	2.6 (*3)	Vpp	
Video amplifier LPF ripple	-1	±0.5	+1	dB	Bandwidth 100kHz ~ 5.5MHz
Video amplifier LPF group delay		6	30	ns	|GD 3MHz – GD 5.5MHz| (*4)
Analog output total S/(N+D)	45	51		dB	Bandwidth 100kHz ~ 5.5MHz (*5)
Analog output total S/N		54		dB	Bandwidth 100kHz ~ 5.5MHz (*5)

(*1) DAC output of ramp wave. (input code : 0 ~ 1023)

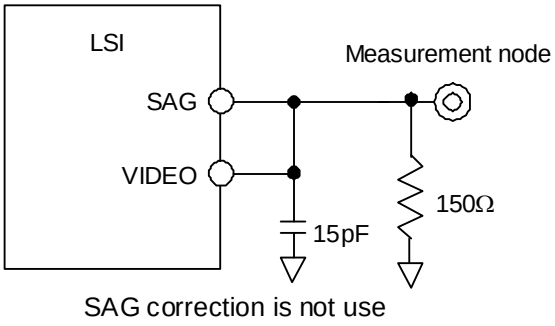
(*2) Amplifier input level 1Vpp correspond to DAC output when input code is from 0 to 800.

(*3) Distortion characteristic is not guaranteed when output over 2.0Vpp.

(*4) Design reference value.

(*5) Video amplifier output when the digital sine wave signal of 1MHz and 1Vpp is input to DAC.
Output load resistance : 150Ω, Output load capacitance : 15pF

[Measurement circuit]



SAG correction is not use

5.4.3. Crystal oscillator

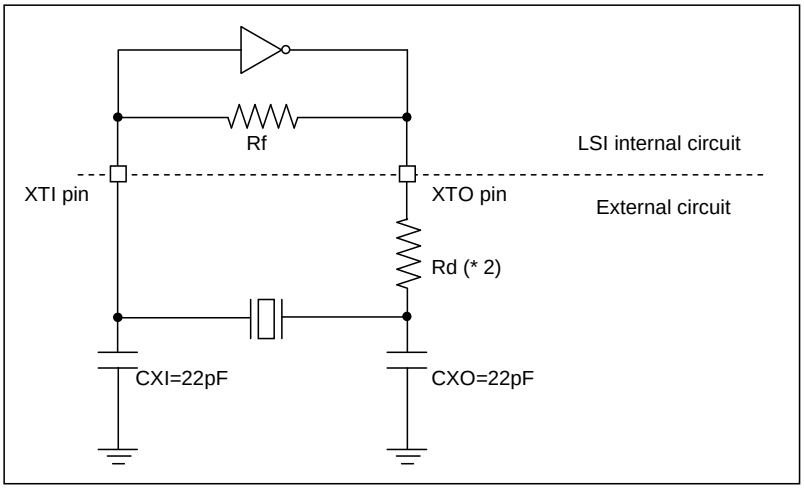
(Conditions : XVDD=3.3V, XVSS=0V, Ta=25℃)

Parameter	Min.	Typ.	Max.	Units	Conditions
Oscillation frequency		28.636		MHz	NTSC
		28.375			PAL
Frequency accuracy		±10	±100	ppm	
Load capacitance CL		13		pF	
Effective equivalent resistance Re			100	Ω	
Crystal parallel capacitance CO		2		pF	(*2)
XTI terminal external connection load capacitance CXI		22		pF	When use CL=13pF crystal
XTO terminal external connection load capacitance CXO		22		pF	When use CL=13pF crystal

Recommended crystal is CA-301 (EPSON TOYOCOM).

(*1) Effective equivalent resistance generally may be taken as $Re = R1 \times (1+C0/CL)^2$, where R1 : Crystal series equivalent resistance, C0: Crystal parallel capacitance, CL: Load capacitance

Example connection



(*2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

5.4.4. Regulator block

(Conditions : AVDD3=PVDD=3.3V, AVSS=DVSS=0V, Ta=25℃)

Parameter	Min.	Typ.	Max.	Units	Conditions
Output Voltage	1.75	1.80	1.85	V	For digital
	1.85	1.90	1.95	V	For analog
Maximum output (Limit current)	67	87	114	mA	For digital and analog
Over voltage detection voltage (*1)	> 2.3	2.4		V	For digital and analog

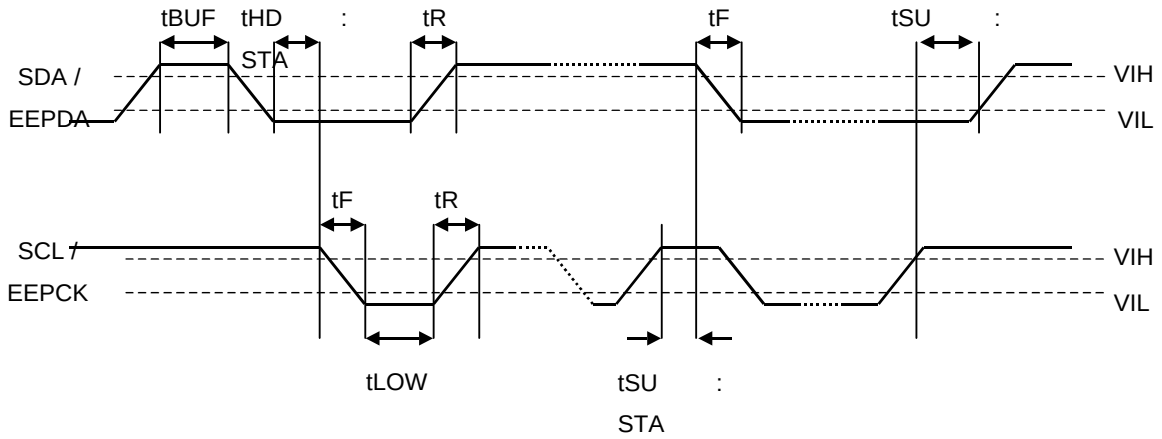
(*1) When over voltage is detected, the LSI will be reset.

5.5. AC timing

5.5.1. 2-wired serial system bus I/O timing

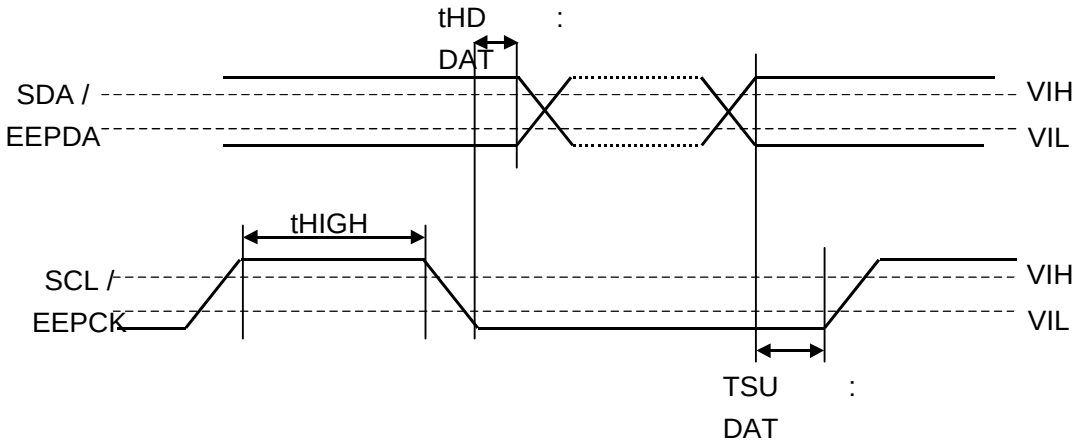
(Typical conditions : PVDD=3.3V, DVSS=0V, Ta=25℃)

(Minimum and maximum conditions : PVDD=3.15 ~ 3.6V, DVSS=0V, Ta=-30 ~ 85℃)



Parameter	Symbol	Min.	Max.	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300*1	nsec
Input Signal Fall Time	tF		300*1	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

*1 Do not inspect in mass production.

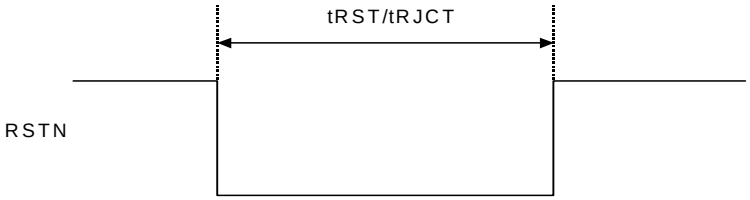


Parameter	Symbol	Min.	Max.	Units
Data Setup Time	tSU:DAT	100		nsec
Data Hold Time	tHD:DAT	0.0(*1)	0.9(*2)	usec
Clock Pulse High Time	tHIGH	0.6		usec

(*1) The device should internally possess the hold time of 300ns or more for the SDA signal, and escape indeterminate condition in SCL falling edge.

(*2) This condition must be met if this LSI used with tLOW=1.3us.

5.5.2. Reset pulse



Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
RSTN pulse width	tRST	500			nsec	
RSTN rejection pulse width	tRJCT			50	nsec	

5.5.3. Power ON/OFF sequences

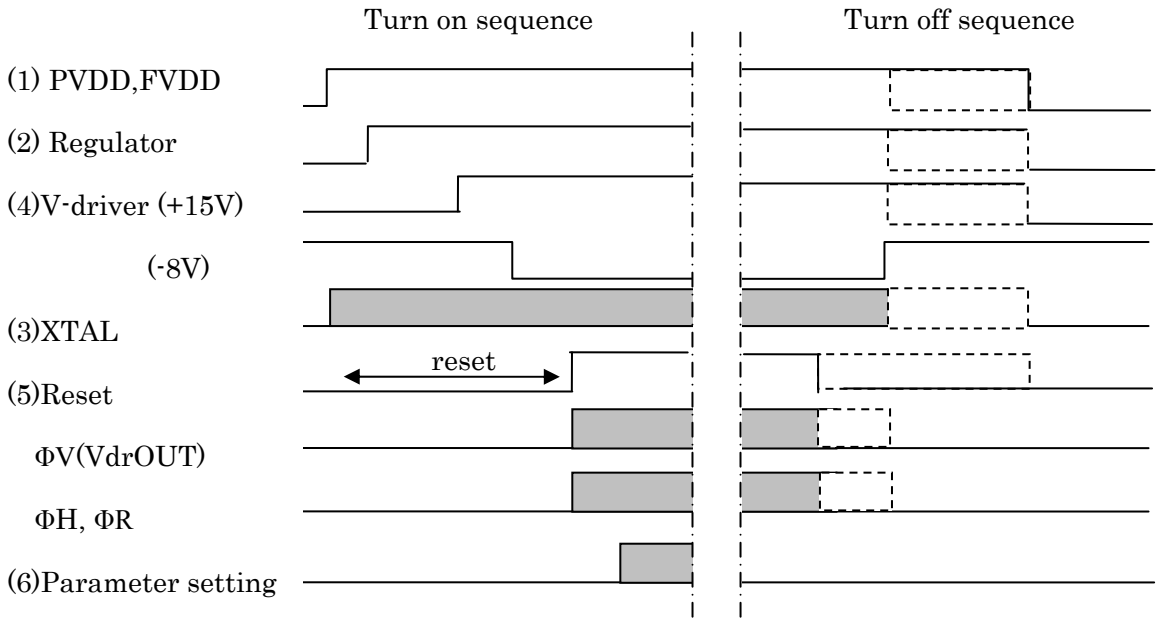
The power supply is turned on according to the following procedures.

Procedure		Power	Regulator	XTAL	Reset	Note
Before turning on the power supply		OFF	OFF	Stop	Low	
①	PVDD,FVDD turning on	ON				
②	Regulator		ON	Rising		
③	XTAL Oscillation			Oscillation		
④	V driver power supply turning on					(*1)
⑤	Reset release				L→High	(*2)
⑥	Parameter setting				High	

(*1) Please turn it on after the low input of V-driver becomes under 0.5V and the high input of it becomes over the VDD (TYP:3.3V) - 0.5V.

(*2) Please do the reset release and turn on ΦV after the clock is steady and the VL (-8V) become under the VL * 0.9.

Note 3) When re-turning on, please wait till the VL become over the VL * 0.1 after the each power supply turn off. And then, please do the above sequence.



6. System Architecture

6.1. CCD Sensor

This LSI has a timing generation circuit and a voltage change circuit, and then this is enable to drive the following CCD sensor. (Some CCD is used with external circuit of Amplifier transmitter of horizontal drive pulse.)

Supported sensor	Register settings (Adrs:001h)	
	TVMD (bit5)	SCCD (bit4)
270-thousand pixels CCD sensor for NTSC	0	0
410-thousand pixels CCD sensor for NTSC	0	1
320-thousand pixels CCD sensor for PAL	1	0
470-thousand pixels CCD sensor for PAL	1	1

6.2. Host I/F

At the host I/F that the following serial bus was connected with, it can set a parameter for the various setting.

Serial bus	Terminal used	Rate (Max)	Reference standard
2-wired system bus	SCL SDA	400kbps	Standard Mode I2C-BUS (I2C-BUS SPECIFICATION Ver2.1: Jan.2000)

Slave address is “1010000Xb” fixed.

6.3. EEPROM

It controls EEPROM which the following serial bus was connected with to save or load of the parameter for the all kind setting in the DSP can be done. Also, each parameter can be automatically read in case of start-up. Incidentally, in case of saving / loading to EEPROM, this DSP accesses EEPROM continuously in 16 bytes, being the longest. Therefore, EEPROM use the one which has the page write feature of equal to or more than 16 bytes.

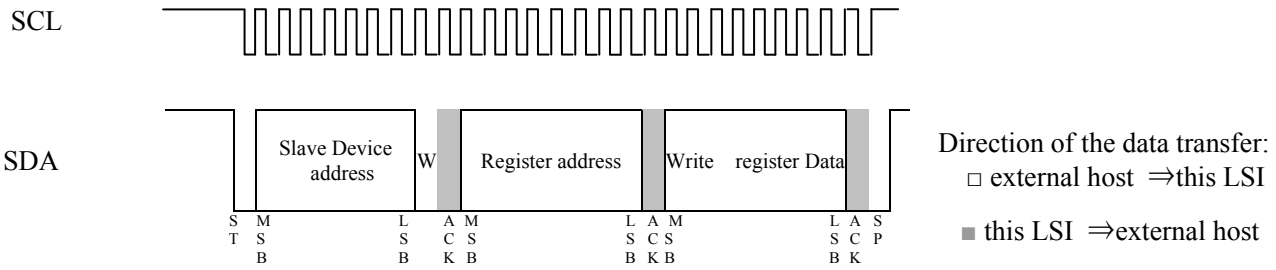
Serial bus	Terminal used	Rate (Max)	Reference devices
2-wired system bus	EEPCK EEPDAI	400kbps	M24C04 (ST-MICRO) 24LC04B (MICROCHIP)

Slave address of EEPROM can be set in DSP adrs 2D3h and 2E3h.

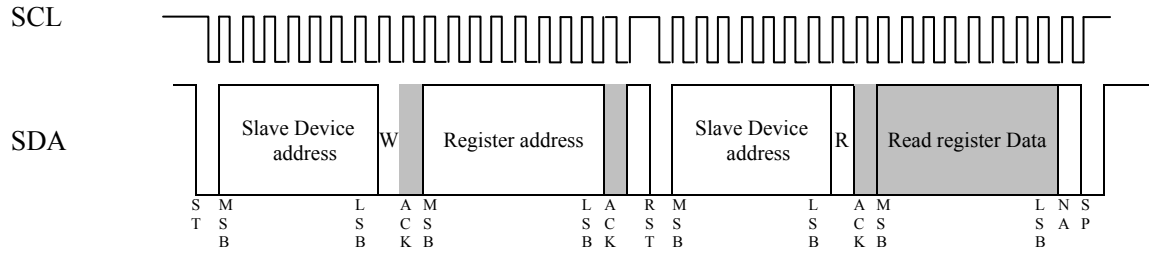
6.4. Host I/F access by 2-wired system bus

Host I/F by the 2-wire system bus of this LSI writes to an outside host according to a logical form, and provides the function to read. Host I/F by the 2-wire system consists of clock line (SCL) for serial communications and serial data line (SDA).

(1) Data writing format to the DSP for byte.



(2) Data reading format from the DSP for 1 byte.



- Start bit (ST) : It is provide for start communication.
- Slave Device address : Slave Device for communication is provide
- ACK bit,NACK bit (NA) : The bit for handshaking in one bit is followed 8 bit data (slave device address, register address, and register data).
- Register address (8bit) : Receive data. It specified the lower 8bit inside of 12bit address.
- Register data (8bit) : Send and receive data. Read/ Write value of register.
- Stop bit (SP) : It is provide for stop communication.
- Resta bit (RST) : It is provide for start reading.

○Start bit (START), Restart bit (RESTA), Stop bit (STOP)

Start bit and Restart bit are defined that the data line (SDA) changes low level from high level with the clock line (SCL) keeping high level. Stop bit is defined that the data line (SDA) changes High level from Low level with the clock line (SCL) keeping high level

○ACK bit, NACK bit

The following one bit of 8 bit data (slave device address, register address, and register data) is a bit for handshaking. When 8 bit data is normally received, the device that receives 8 bit data generates ACK bit (Active Low). At this time, the other device where 8 bit data was transmitted opens the data line. When the host is communicating with other slave devices and 8 bit data cannot be normally received, this device opens the data line and generates NACK bit (Active High) with an external pull-up resistor.

Note) Setting of bank switching is in MSADR register (adrs xFFh).

6.5. EEPROM access by 2-wired system bus

In the setting of the following registers, a set value of each register of DSP is written in EEPROM, the register of DSP can be set from EEPROM.

Register setting value	00h	03h	0Ch
Address 02F9h	No Operation (default)	DSP→EEPROM Batch data writing	EEPROM→DSP Set data reading

This LSI will reload DSP setting data from EEPROM when power up sequence (after reset release).
Relation between EEPROM condition and register access after automatic reload is as follows.

	EEPROM	EEPROM→DSP		DSP→EEPROM	DSP←Host	
		Auto. reload when power up	Read Data		Read Access	Write Access
(1)	Initialized	Enable	Valid	Enable	Enable	Enable
(2)	Not initialized		Invalid data		Disable	

In case of the EEPROM which is not initialized is connected, the DSP may set in condition (2).
Please initialize EEPROM according to following sequence.

[Initialize EEPROM]

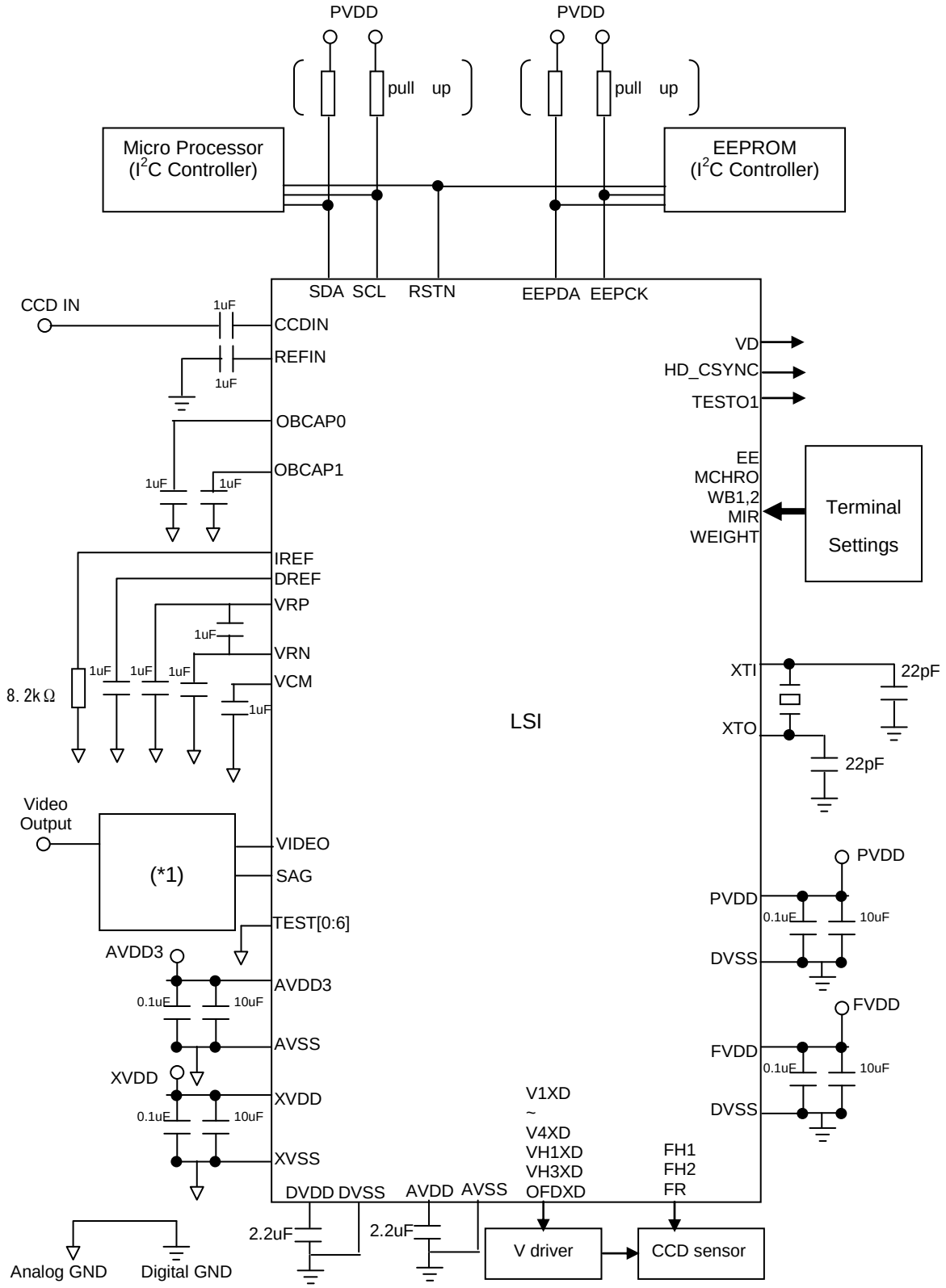
process	Host→DSP operation			Contents
	Adrs	R/W	Value	
1	02F9h	Read	(‘00h’)	Initialize EEPROM (During adrs 02F9h[4]=’1’, DSP accessing to EEPROM. Do not do next sequence until it turn to ‘0’.)
2	02F9h	Write	(‘03h’)	
3	02F9h	Read	(‘00h’)	
4	02F9h	Write	(‘03h’)	
5	02F9h	Read	(‘00h’)	
6	Make reset or turn off the power of LSI once and turn it on again.			
7	02F9h	Read	(‘00h’)	Confirm to finish accessing to EEPROM.
8	any	Write	Any	Write data to EEPROM after the parameter that is wanted to store to EEPROM are set to DSP.
9	02F9h	Write	(‘03h’)	
10	02F9h	Read	(‘00h’)	Confirm to finish EEPROM access.

6.6. Operation mode selection using external terminals

To set register SW_SEL (adrs 018h[0]) =’0’, external terminal witch has function same as corresponded registers will be active.

Operation mode		Priority of terminal setting and register setting. Selected by SW_SEL register (adrs 018h[0])	
Terminal	Mode description	SW_SEL= ”0” (Default)	SW_SEL= “1”
EE	Fixed speed of an electronic shutter 0: Fixed Shutter speed (NTSC: 1/100, PAL: 1/120 correspond to REG_EEMD=0001) 1: Automatic shutter speed control	EE terminal is active	REG_EEMD (adrs 019h[7:4]) is active
WB1,2	Fixed white balance mode 00: Fixed mode WB1 01: Fixed mode WB2 10: Fixed mode WB3 11: Automatic control	WB1,2 terminals are active	REG_WBSEL (adrs 0x19[3:2]) is active
BLC	Backlight compensation mode 0: Normal 1: Backlight	BLC terminal is active	REG_BLC (adrs 019h[1]) is active
MIR	Mirror mode 0: Normal 1: Mirror	MIR terminal is active	REG_MIR (adrs 019h[0]) is active
WEIGHT	Weight parameter selecion 0: A 1: B A: set in adrs 111h~117h B: set in adrs 0EBh~0F1h	WEIGHT terminal is active	REG_WEIGHT (adrs 0EB[5]) is active
MCHRO	White and black video output 0: Normal (color) 1: White and black video output	MCHRO terminal is active	REG_MCHRO (adrs 0x21[7]) is active

6.7. System connection example

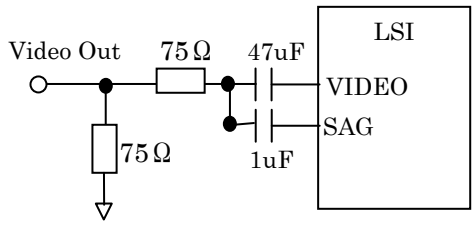


(*1) Refer to figure of video amplifier frequency characteristics for connection between VIDEO and SAG terminal.

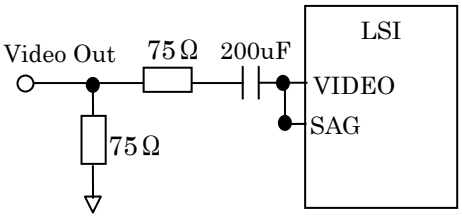
7. Additions

7.1. Figure of video amplifier frequency characteristics

(a) SAG compensation is used : 47uF + 1uF

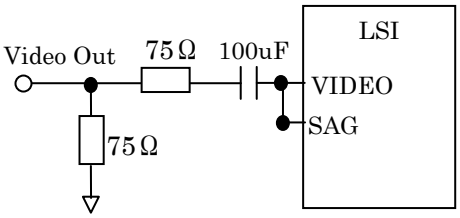


(b) SAG compensation is not used : 200uF

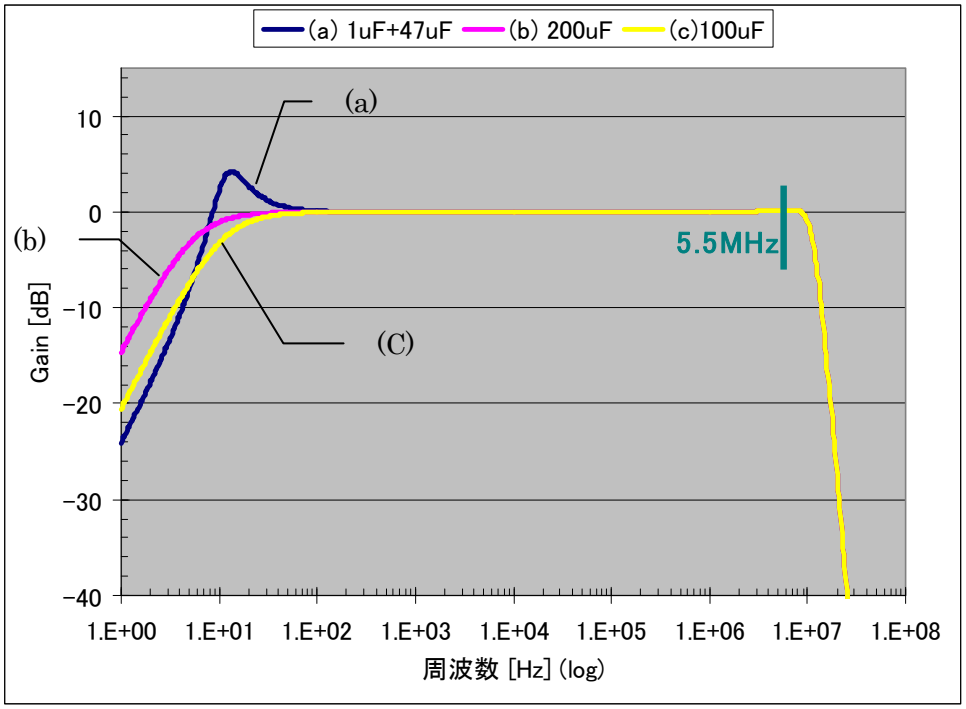


Measurement point is Video Out

(c) SAG compensation is not used : 100uF



(Unless otherwise Ta=25℃, AVDD3=3.3V, Design reference value)



8 Package and packing specification

[Applicability]

This specification applies to an IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% (Relative humidity) max.
- Storage period：One year max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

（1） Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

2. Baking Condition.

（1） Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2

（2） Recommended baking conditions.

- Baking temperature and period :
  125℃ for 25 hours.
- The above baking conditions apply since the trays are heat-resistant.

（3） Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

3. Surface mount conditions.

The following soldering conditions are recommended to ensure device quality.

3-1.Soldering.

（1） Convection reflow or IR/Convection reflow. (one-time soldering or two-time soldering in air or nitrogen environment)

・Temperature and period :

A) Peak temperature. 250℃ max.

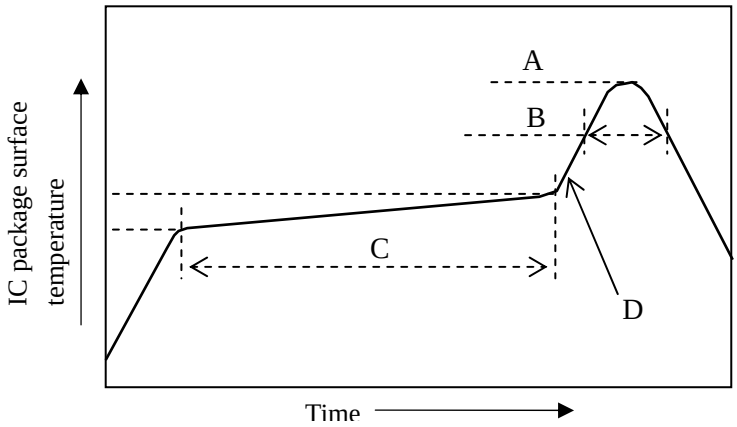
B) Heating temperature. 45 to 65 seconds as 220℃

C) Preheat temperature. It is 150 to 180℃, and is 105±15 seconds

D) Temperature increase rate. It is 1 to 3℃/seconds

・Measuring point : IC package surface.

・Temperature profile :



4. Condition for removal of residual flux.

（1） Ultrasonic washing power : 25 watts / liter max.

（2） Washing time : Total 1 minute max.

（3） Solvent temperature : 15～40℃

5. Package outline specification.

5-1. Package outline.

Refer to the attached drawing.

(Plastic body dimensions do include burr of resin.)

5-2. Package weight.

0.2g/pcs. About.

6. Markings.

6-1.Marking details. (The information on the package should be given as follows.)

（1） Product name : LR36B15

（2） Company name : SHARP

（3） Date code : （Example）YYWWXXX

YY → Denotes the production year. (Last two digits of the year.)

WW → Denotes the production week.（01・02・～・52・53）

XXX → Denotes the production ref. code.

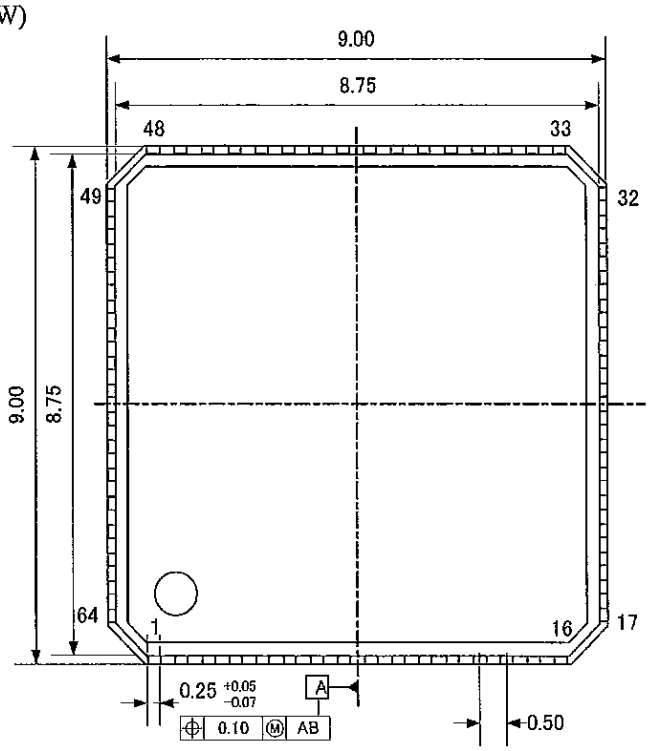
6-2.Marking layout.

The layout is shown in the attached drawing.

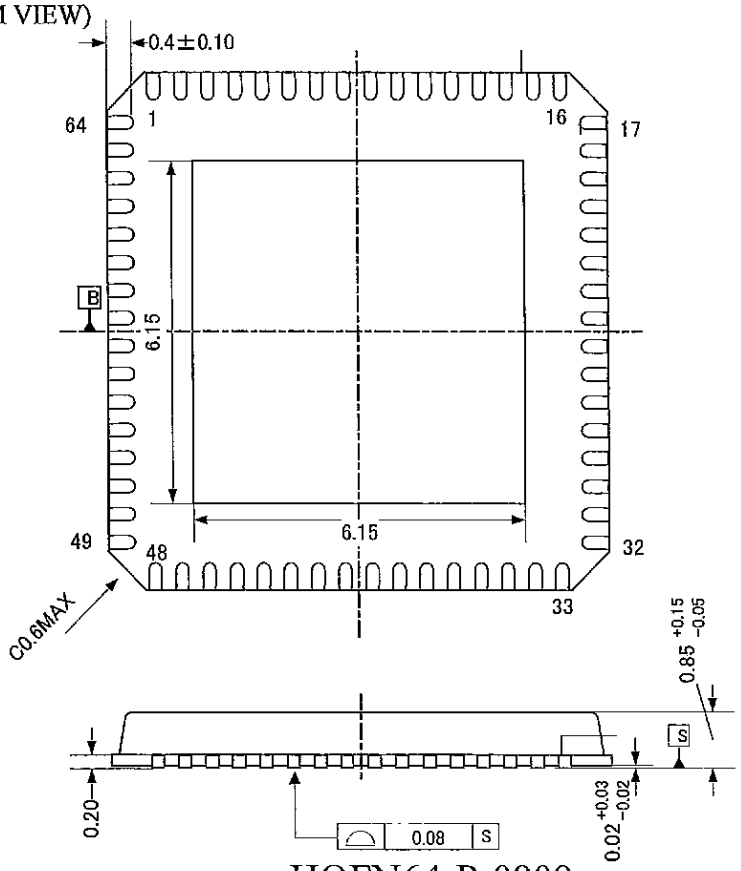
(However, this layout does not specify the size of the marking character and marking position.)

(Note)It is those with an underline printing in a date code because of a LEAD FREE type.

(TOP VIEW)



(BOTTOM VIEW)



HQFN64-P-0909

パッケージ PKG	HQFN064-P-0909	単位 UNIT	mm	NOTE

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard （2600 devices / inner carton max.）	Packing the devices. （10 trays / inner carton）
Tray	Conductive plastic（260 devices / tray）	Securing the devices.
Upper cover tray	Conductive plastic（1 tray / inner carton）	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene （3 pcs. / inner carton ）	Securing the devices.
Outer carton	Cardboard （10400 devices / outer carton max.）	Outer packing.

（ Devices must be placed on the tray in the same direction.）

7-2.Outline dimension of tray.

Refer to the attached drawing.

8. Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

(3) The devices should be mounted within one year of the date of delivery.

9. Chemical substance information in the product

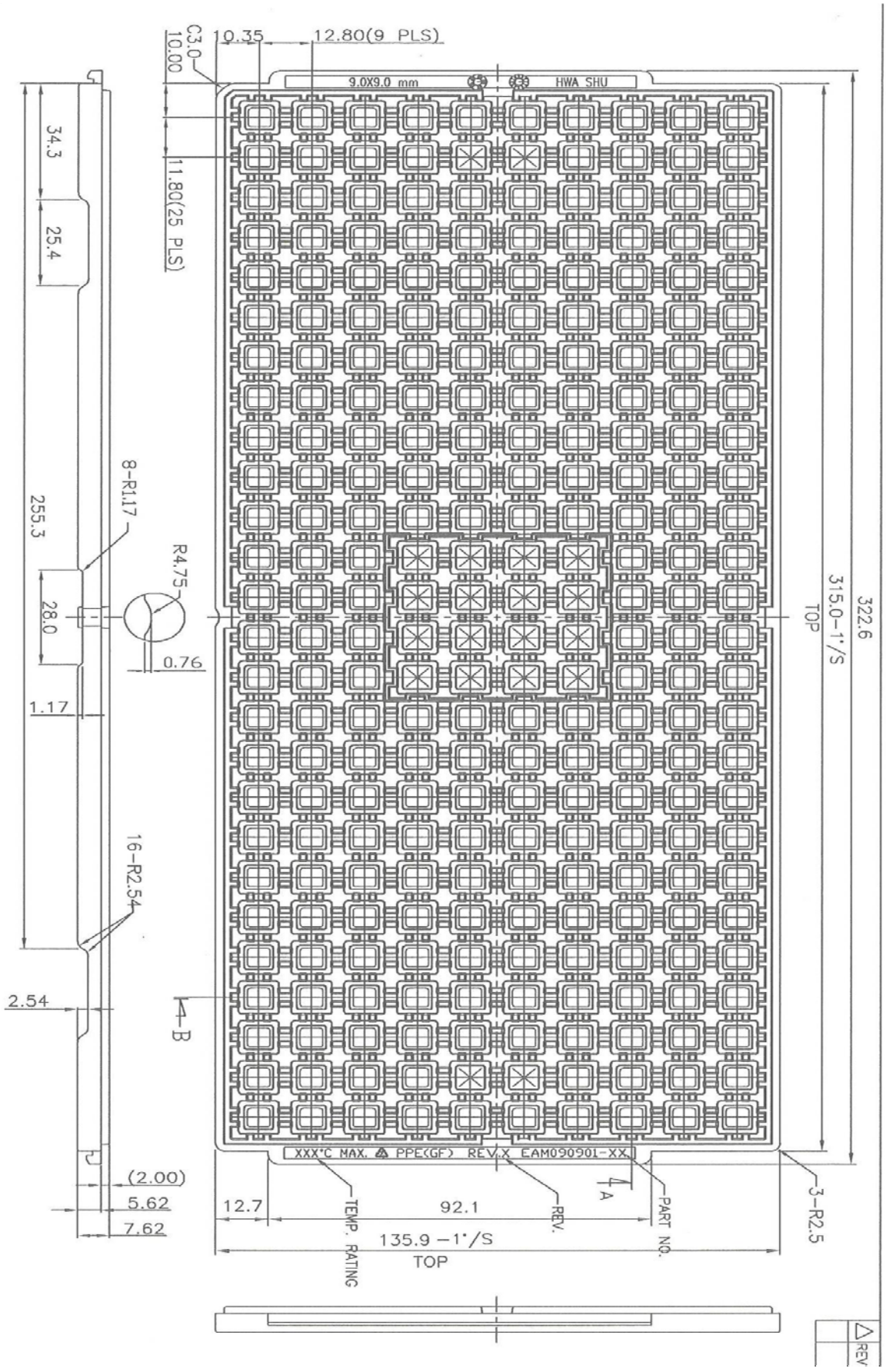
Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

Names and Contents of the Toxic and Hazardous Substances or Elements in the Product

Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
○	○	○	○	○	○

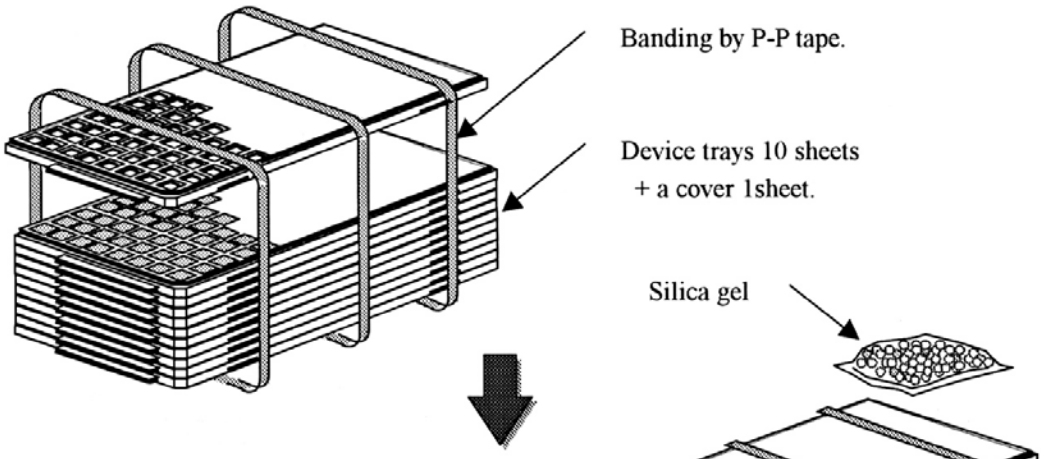
○：indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.

×：indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006 standard.

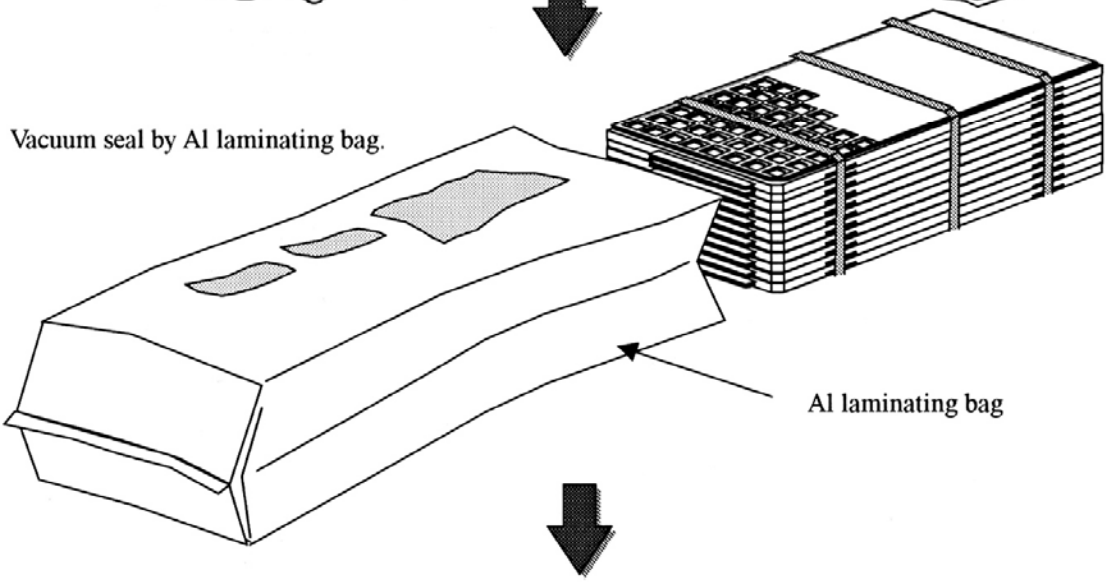


単位 UNIT	mm	NOTE

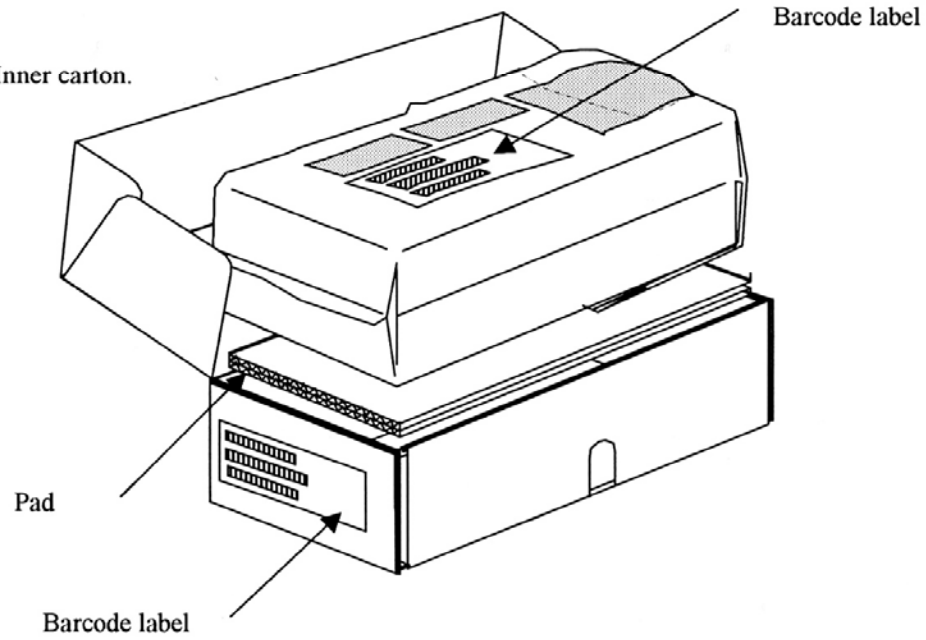
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.

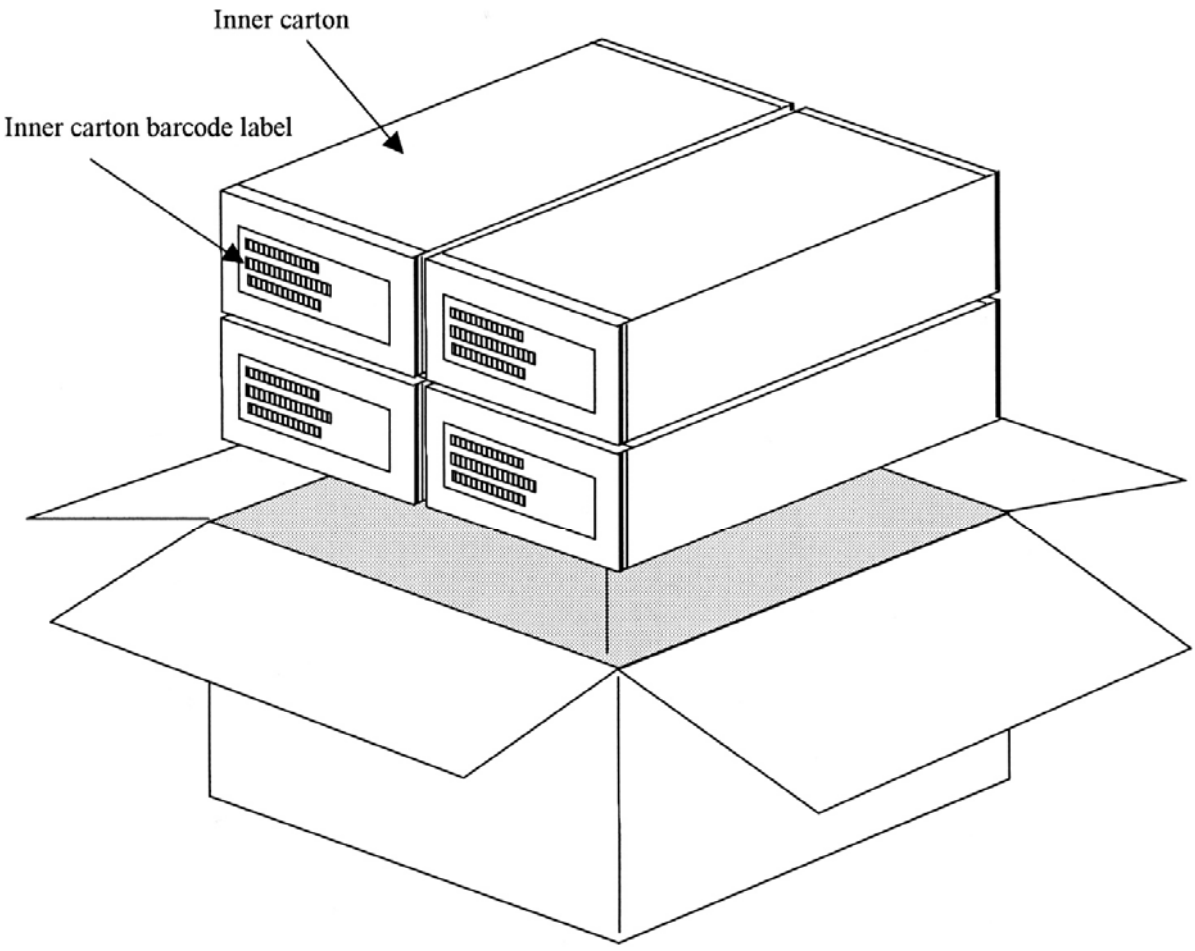


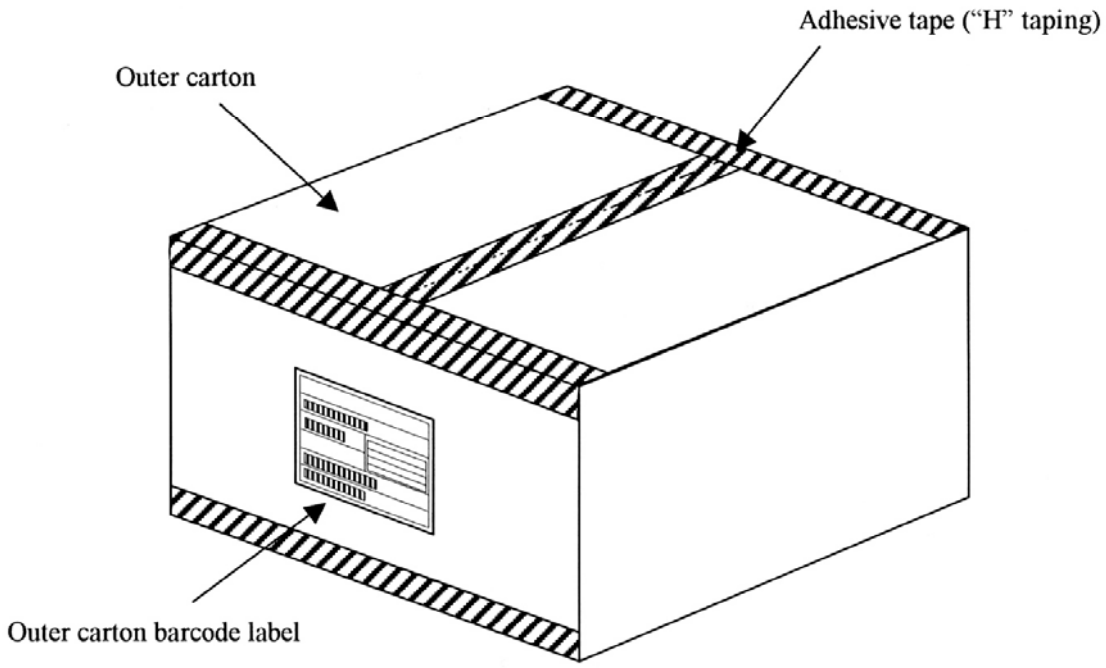
(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.





L × W× H

Inner carton - Outer dimensions : 360×150×95

Outer carton - Outer dimensions : 390×335×230

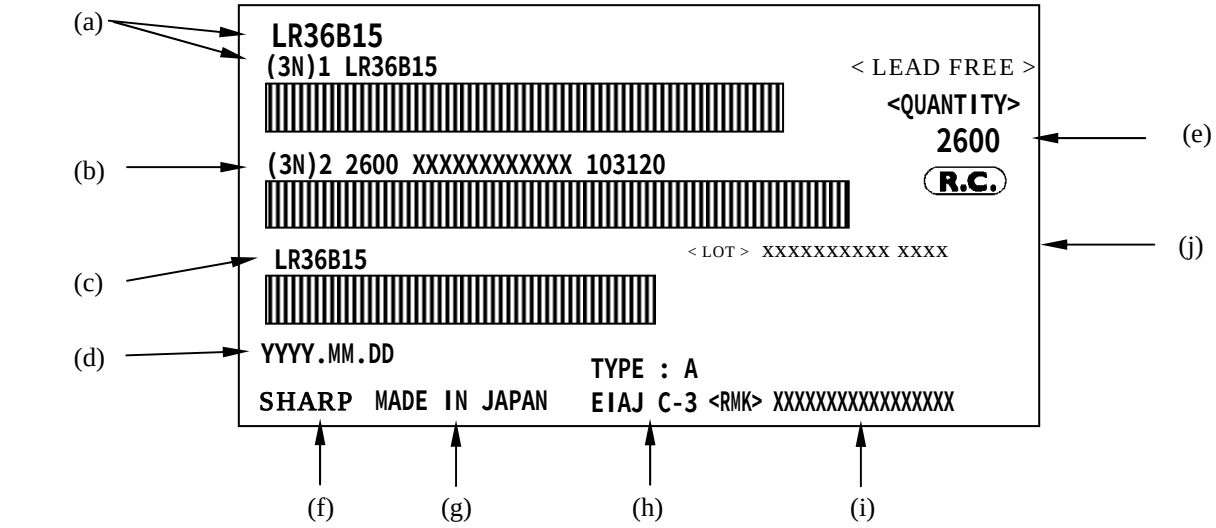
NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

20110727

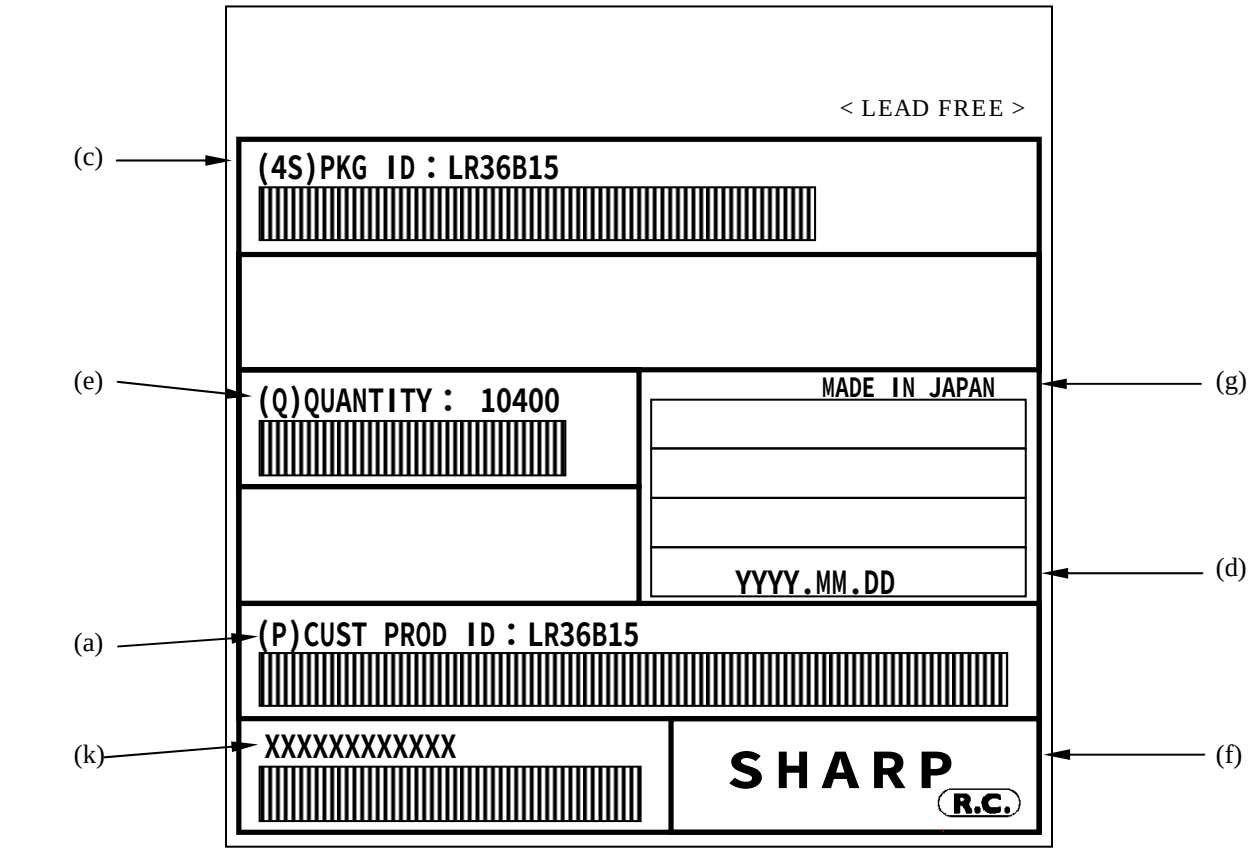
(Note) The << LEAD FREE >> display shows a lead free article.
"R.C." is Sharp's corporate logo indicating that the product is RoHS compliant.

Inner carton label



Outer carton label

(Former) EIAJ B Standard conforming



(a) Product name
(b) Quantity PD lot Company code
(c) Part No. (SHARP)
(d) Packed date
(e) Quantity
(f) "SHARP" Logo
(g) The country of origin
(h) Type name (Conformity standard)
(i) Sharp management No.
(j) Sharp control No.
(k) Shipment lot