LR38575

Timing Generator IC for 1 310 k-pixel CCD

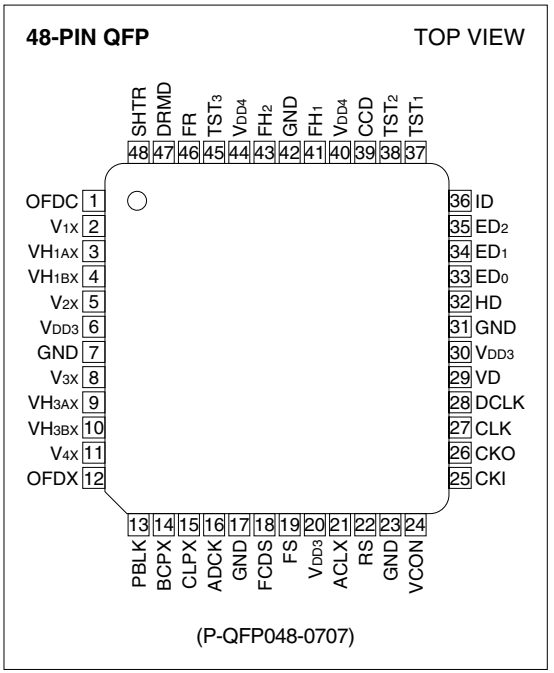
DESCRIPTION

The LR38575 is a CMOS timing generator IC which generates timing pulses for driving 1 310 k-pixel CCD area sensor and processing pulses.

FEATURES

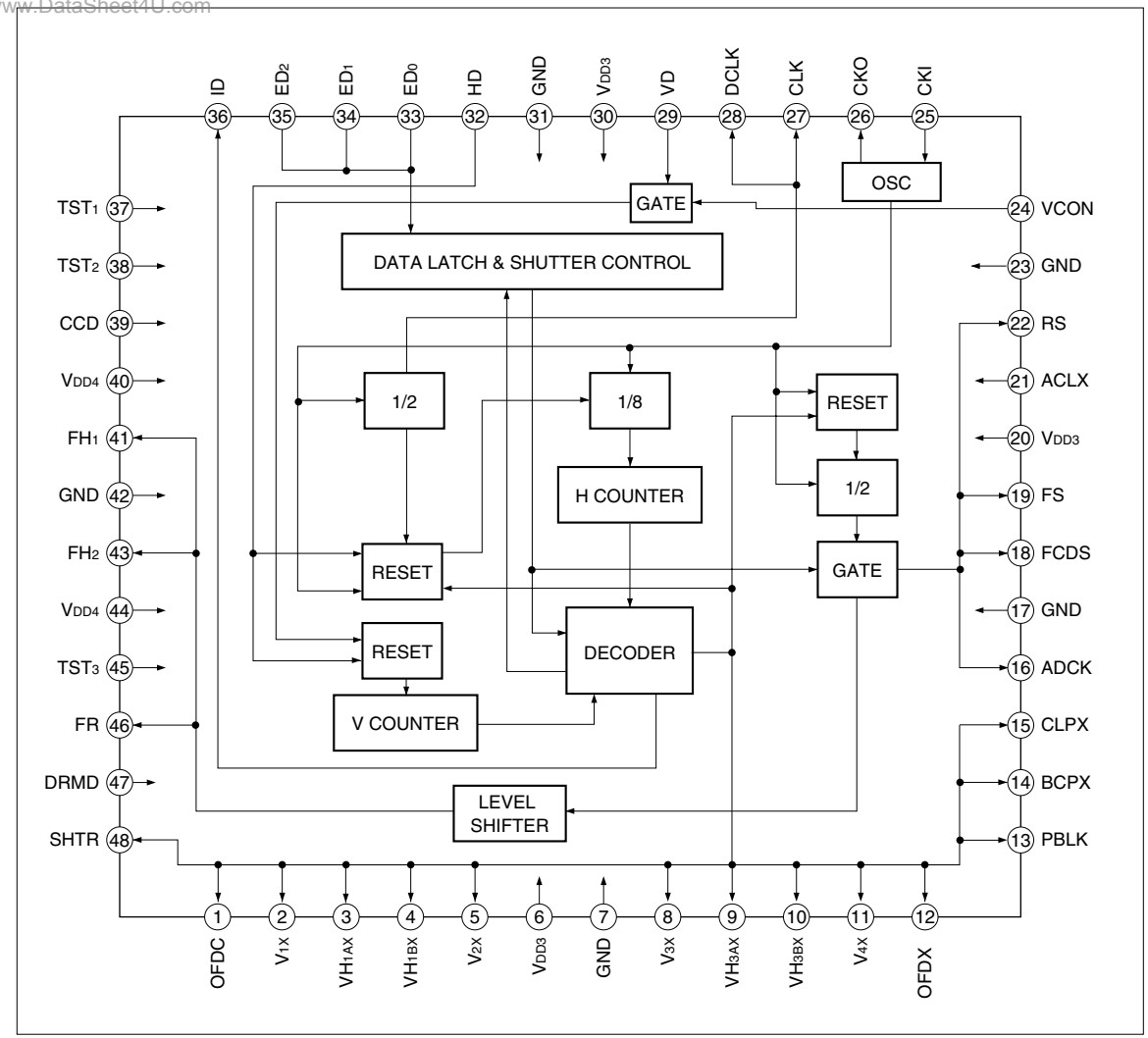
- Designed for 1/3.2-type 1 310 k-pixel CCD area sensor
- Frequency of driving horizontal CCD : 12.272725 MHz
- In monitoring mode, it can be obtained 30 fields/s
- Two still mode types :
  3 fields period and 4 fields period
- External shutter control function with serial data input is possible
- +3.3 V and +4.5 V power supplies
- Package :
  48-pin QFP (P-QFP048-0707) 0.5 mm pin-pitch

PIN CONNECTIONS



(P-QFP048-0707)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
1	OFDC	O3	⎍	Control pulse output for OFD voltage	A pulse to control OFD voltage.
2	V_{1X}	O3	⎍	Vertical transfer pulse output 1	A vertical transfer pulse for the CCD. Connect to V_{1X} pin of vertical driver IC.
3	VH_{1AX}	O3	⎎	Readout pulse output 1A	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH_{1AX} pin of vertical driver IC.
4	VH_{1BX}	O3	⎎	Readout pulse output 1B	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH_{1BX} pin of vertical driver IC.
5	V_{2X}	O3	⎍	Vertical transfer pulse output 2	A vertical transfer pulse for the CCD. Connect to V_{2X} pin of vertical driver IC.
6	V_{DD3}	–	–	Power supply	Supply of +3.3 V power.
7	GND	–	–	Ground	A grounding pin.
8	V_{3X}	O3	⎎	Vertical transfer pulse output 3	A vertical transfer pulse for the CCD. Connect to V_{3X} pin of vertical driver IC.
9	VH_{3AX}	O3	⎎	Readout pulse output 3A	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH_{3AX} pin of vertical driver IC.
10	VH_{3BX}	O3	⎎	Readout pulse output 3B	A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH_{3BX} pin of vertical driver IC.
11	V_{4X}	O3	⎎	Vertical transfer pulse output 4	A vertical transfer pulse for the CCD. Connect to V_{4X} pin of vertical driver IC.
12	OFDX	O3	⎎	OFD pulse output	A pulse that sweeps the charge of the photo-diode for the electronic shutter. Connect to OFD pin of the CCD through the vertical driver IC and DC offset circuit. Held at H level in normal mode.
13	PBLK	O3	⎎	Pre-blanking pulse output	A pulse for pre-blanking. This pulse is controlled by serial data BLKCNT. BLKCNT = H; This pulse stays low during the absence of effective pixels within the vertical blanking or during the sweepout signal. BLKCNT = L; This pulse stays high during the sweepout signal. The output phase of PBLK is selected by serial data.

PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
14	BCPX	O3		Optical black clamp pulse output	A pulse to clamp the optical black signal. This pulse is controlled by serial data BCPCNT; BCPCNT = H; This pulse stays high during the absence of effective pixels within the vertical blanking or during the sweepout signal. BCPCNT = L; This pulse stays high during the sweepout signal.
15	CLPX	O3		Clamp pulse output	A pulse to clamp the dummy outputs of the CCD signal. This pulse stays high during the sweepout period.
16	ADCK	O6MA3		AD clock output	An output pin for AD converter. The output phase of ADCK is selected by serial data in 90˚ steps.
17	GND	–	–	Ground	A grounding pin.
18	FCDS	O6MA3		CDS pulse output 1	A pulse to clamp the feed-through level for the CCD. The output phase and output polarity of FCDS are selected by serial data.
19	FS	O6MA3		CDS pulse output 2	A pulse to sample-hold the signal for the CCD. The output phase and output polarity of FS are selected by serial data.
20	V_{DD3}	–	–	Power supply	Supply of +3.3 V power.
21	ACLX	ICU3	–	All clear input	An input pin for resetting all internal circuits at power-on. Connect to V_{DD} through the diode and GND through the capacitor.
22	RS	O6MA3		S/H pulse output	A pulse to sample-hold the signal for the CDS circuit. The output polarity of RS is selected by serial data.
23	GND	–	–	Ground	A grounding pin.
24	VCON	ICU3	–	VD control input	An input pin to control internal vertical clock for long shutter speed. H level or open : VD L level : VD is masked by the pulse which is latched at the rising edge of VD. It's necessary to be set SMD = high and number of the fields data n ≥ 2 in serial data control at VCON operation.
25	CKI	OSCI3	–	Clock input	An input pin for reference clock oscillation. The frequency is 24.54545 MHz.
26	CKO	OSCO3	–	Clock output	An output pin for reference clock oscillation. The output is the inverse of CKI (pin 25).
27	CLK	O6MA3		Clock output	An output pin to generate HD and VD pulses. The frequency is 12.272725 MHz.

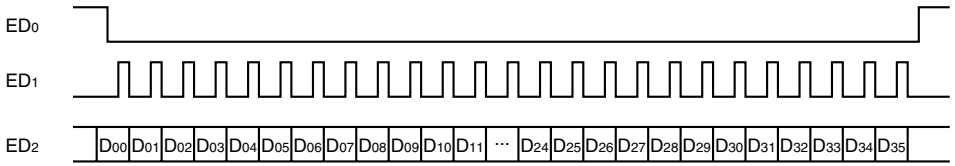
PIN NO.	SYMBOL	IO SYMBOL	POLARITY	PIN NAME	DESCRIPTION
28	DCLK	O6MA3		Clock output	An output pin for DSP IC. The frequency is 12.272725 MHz. The output phase of DCLK is selected by serial data in 90˚ steps.
29	VD	IC3		Vertical reference pulse input	An input pin for reference of vertical pulse. Connect to VD pin of DSP IC.
30	V_{DD3}	–	–	Power supply	Supply of +3.3 V power.
31	GND	–	–	Ground	A grounding pin.
32	HD	IC3		Horizontal drive pulse input	An input pin for reference of horizontal pulse. Connect to HD pin of DSP IC.
33	ED_0	ICSU3	–	Strobe pulse input	An input pin for the strobe pulse, to control the functions of LR38575. For details, see "**Serial Data Control**".
34	ED_1	ICSU3	–	Shift register clock input	An input pin for the clock of the shift register, to control the functions of LR38575. For details, see "**Serial Data Control**".
35	ED_2	ICSU3	–	Shift register data input	An input pin for the data of the shift register, to control the functions of LR38575. For details, see "**Serial Data Control**".
36	ID	O3		Line index pulse output	The pulse is used in color separator. The signal switches between high and low at every line.
37	TST_1	ICD4	–	Test pin 1	A test pin. Set open or to L level in normal mode.
38	TST_2	ICD4	–	Test pin 2	A test pin. Set open or to L level in normal mode.
39	CCD	ICU4	–	CCD selection input	An input pin to select CCD. It should be used with MODE input which is in the serial data. Fix to H level or open.
40	V_{DD4}	–	–	Power supply	Supply of +3.3 to +4.5 V power.
41	FH_1	O6MA43		Horizontal transfer pulse output 1	A horizontal transfer pulse for the CCD. Connect to ϕ_{H1} pin of the CCD.
42	GND	–	–	Ground	A grounding pin.
43	FH_2	O6MA43		Horizontal transfer pulse output 2	A horizontal transfer pulse for the CCD. Connect to ϕ_{H2} pin of the CCD.
44	V_{DD4}	–	–	Power supply	Supply of +3.3 to +4.5 V power.
45	TST_3	ICD4	–	Test pin 3	A test pin. Set open or to L level in normal mode.
46	FR	O6MA43		Reset pulse output	A pulse to reset the charge of output circuit. The output phase of FR is selected by serial data.
47	DRMD	ICU3	–	Drive mode selection input	An input pin to select the period of still mode. L level : 3 fields period H level or open : 4 fields period
48	SHTR	O3		Trigger output	A trigger pulse for effective signal period.

IC3 : Input pin (CMOS level)
ICU3 : Input pin (CMOS level with pull-up resistor)
ICSU3 : Input pin (CMOS schmitt-trigger level with pull-up resistor)
ICU4 : Input pin (CMOS level with pull-up resistor)
ICD4 : Input pin (CMOS level with pull-down resistor)

O3 : Output pin (output high level is V_{DD3}.)
O6MA3 : Output pin (output high level is V_{DD3}.)
O6MA43 : Output pin (output high level is V_{DD4}.)
OSCI3 : Input pin for oscillation
OSCO3 : Output pin for oscillation

Serial Data Control

SERIAL DATA INPUT TIMING



ED_2 is shifted at the rising edge of ED_1, and is latched at the rising edge of ED_0.

PWSA is effective at the rising edge of ED_0, but others are effective at the horizontal line in which VH_{1AX} to VH_{3BX} are active.

ED_0 should be at low level during data inputs of ED_1 and ED_2.

Since all internal data are set to low level by ACLX, ED_0 to ED_2 should be input for proper operations.

Since all internal data except PWSA are set to low level by PWSA, ED_0 to ED_2 should be input for proper operations.

SERIAL DATA INPUTS

DATA	NAME	FUNCTION	DATA = L	DATA = H	AT ACLX = L
D_{00}-D_{06}	SD_0-SD_6	Step of high speed shutter	–		All L
D_{07}	SD_7	Number of exposed fields	–		All L
D_{08}	SD_8				
D_{09}	SD_9				
D_{10}	SMD	Electronic shutter mode control	–		L
D_{11}	INMD	Integration mode control	Monitoring	Still	L
D_{12}	PWSA	Power save control	Normal	Power save	–
D_{13}	PLCH	Polarity control of FCDS, FS and RS pulses	Negative	Positive	L
D_{14}	MODE	Monitoring mode selection with CCD (pin 39)	No use	RJ24J3XX	L
D_{15}	BCPCNT	BCP control	Discontinuous	Continuous	L
D_{16}	ML_1	Phase control	–		All L
D_{17}	ML_2				
D_{18}	MR_1		–		All L
D_{19}	MR_2				
D_{20}	MR_3				
D_{21}	MC_1		–		All L
D_{22}	MC_2				
D_{23}	MC_3				
D_{24}	MS_1		–		All L
D_{25}	MS_2				
D_{26}	MS_3				
D_{27}	MD_1		–		All L
D_{28}	MD_2				
D_{29}	MD_3				
D_{30}	MA_1		–		All L
D_{31}	MA_2				
D_{32}	MP_1		–		All L
D_{33}	MP_2				
D_{34}	BLKCNT	PBLK control	Discontinuous	Continuous	L
D_{35}	VHCONT	VH_{1AX} to VH_{3BX} control	Normal	Stay H	L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{DD3}, V_{DD4}	−0.3 to +6.0	V
Input voltage	V_{I3}	−0.3 to V_{DD3} + 0.3	V
	V_{I4}	−0.3 to V_{DD4} + 0.3	V
Output voltage	V_{O3}	−0.3 to V_{DD3} + 0.3	V
	V_{O4}	−0.3 to V_{DD4} + 0.3	V
Operating temperature	T_{OPR}	−20 to +70	°C
Storage temperature	T_{STG}	−55 to +150	°C

ELECTRICAL CHARACTERISTICS

DC Characteristics (V_{DD3} = 3.0 V to V_{DD4}, V_{DD4} = V_{DD3} to 5.5 V, $V_{DD4} \geq V_{DD3}$, T_{OPR} = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL3-1}				$0.2V_{DD3}$	V	1, 2
Input "High" voltage	V_{IH3-1}		$0.8V_{DD3}$			V	
Input "Low" voltage	V_{IL3-2}	Schmitt-buffer	$0.2V_{DD3}$			V	3
Input "High" voltage	V_{IH3-2}				$0.75V_{DD3}$	V	
Hysteresis voltage	$V_{T+} - V_{T-}$		$0.08V_{DD3}$			V	
Input "Low" voltage	V_{IL4}				$0.2V_{DD4}$	V	4, 5
Input "High" voltage	V_{IH4}		$0.8V_{DD4}$			V	
Input "Low" current	$\lvert I_{IL3-1} \rvert$	V_I = 0 V			1.0	µA	1
Input "High" current	$\lvert I_{IH3-1} \rvert$	$V_I = V_{DD3}$			1.0	µA	
Input "Low" current	$\lvert I_{IL3-2} \rvert$	V_I = 0 V	2.0		60	µA	2, 3
Input "High" current	$\lvert I_{IH3-2} \rvert$	$V_I = V_{DD3}$			2.0	µA	
Input "Low" current	$\lvert I_{IL4-1} \rvert$	V_I = 0 V	2.0		60	µA	4
Input "High" current	$\lvert I_{IH4-1} \rvert$	$V_I = V_{DD4}$			2.0	µA	
Input "Low" current	$\lvert I_{IL4-2} \rvert$	V_I = 0 V			2.0	µA	5
Input "High" current	$\lvert I_{IH4-2} \rvert$	$V_I = V_{DD4}$	2.0		60	µA	
Output "Low" voltage	V_{OL3-1}	I_{OL} = 2 mA			0.4	V	6
Output "High" voltage	V_{OH3-1}	I_{OH} = −1 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-2}	I_{OL} = 2 mA			0.4	V	7
Output "High" voltage	V_{OH3-2}	I_{OH} = −2 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL3-3}	I_{OL} = 3 mA			0.4	V	8
Output "High" voltage	V_{OH3-3}	I_{OH} = −3 mA	V_{DD3} − 0.5			V	
Output "Low" voltage	V_{OL4}	I_{OL} = 9 mA			0.4	V	9
Output "High" voltage	V_{OH4}	I_{OH} = −9 mA	V_{DD4} − 0.5			V	

NOTES :

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICU3).
3. Applied to input (ICSU3).
4. Applied to input (ICU4).
5. Applied to input (ICD4).
6. Applied to output (O3).
7. Applied to output (OSCO3). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or V_{DD3}.)
8. Applied to output (O6MA3).
9. Applied to output (O6MA43).

PACKAGE OUTLINES

48 QFP (P-QFP048-0707)

(Unit : mm)