**SHARP**

# LR38620

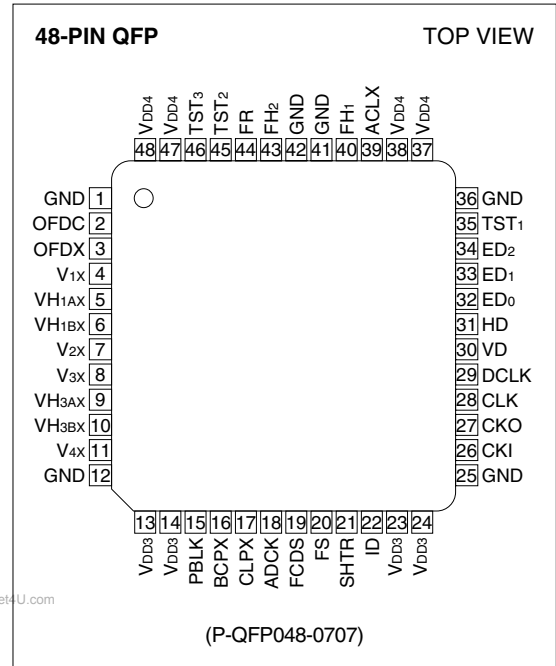## Timing Generator IC for 4 200 k-pixel CCD

## DESCRIPTION

The LR38620 is a CMOS timing generator IC which generates timing pulses for driving 4 200 k-pixel CCD area sensor and processing pulses.
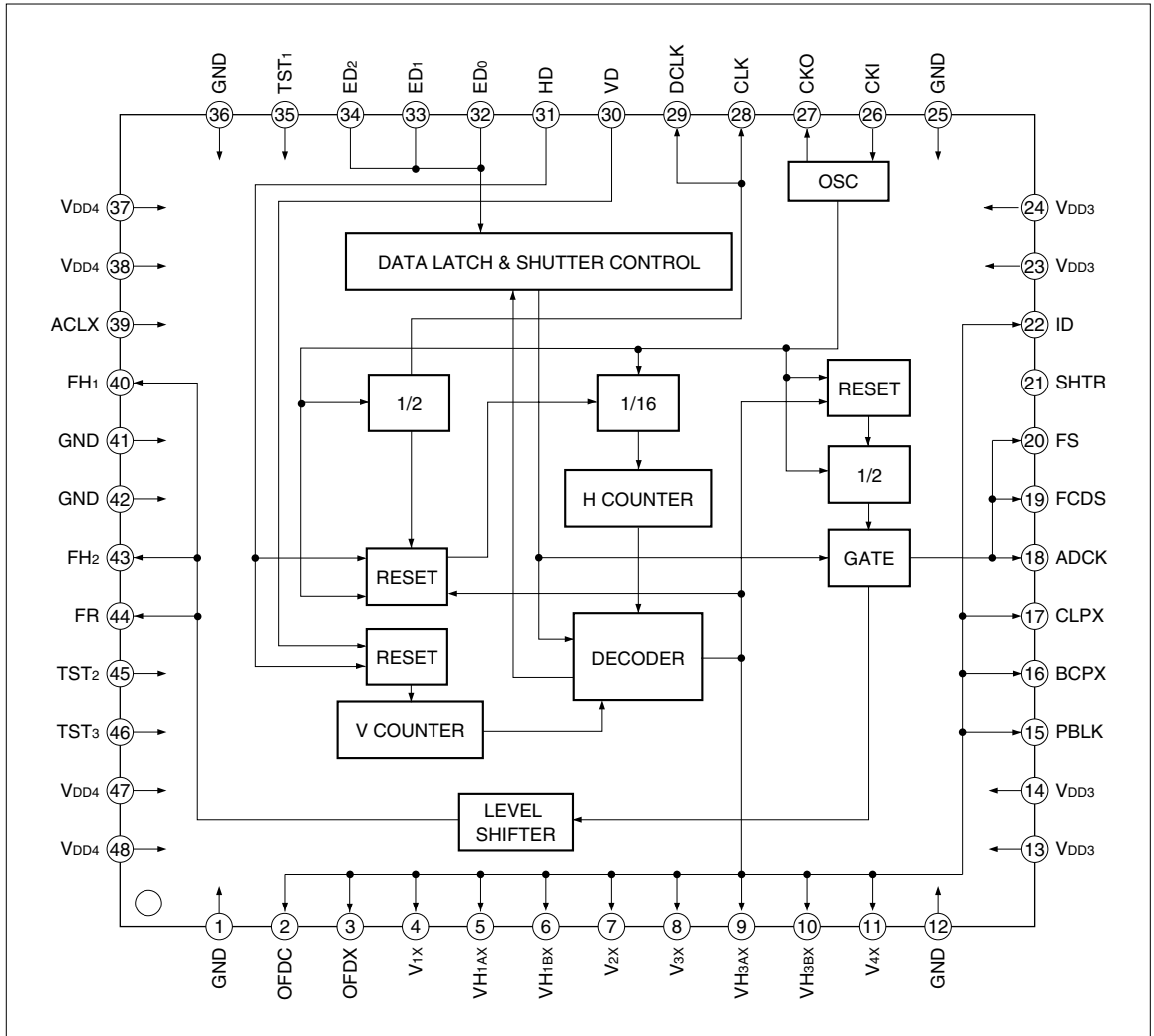
## FEATURES

- Designed for 1/1.8-type 4 200 k-pixel CCD area sensor
- Frequency of driving horizontal CCD : 24.54545 MHz
- In monitoring mode, it can be obtained 30 fields/s
- External shutter control function with serial data input is possible
- +3.3 V and +4.5 V power supplies
- Package :
  48-pin QFP (P-QFP048-0707) 0.5 mm pin-pitch

## PIN CONNECTIONS

**48-PIN QFP**                TOP VIEW

Top pins (48–37): $V_{DD4}$, $V_{DD4}$, $TST_3$, $TST_2$, FR, $FH_2$, GND, GND, $FH_1$, ACLX, $V_{DD4}$, $V_{DD4}$

Left pins (1–12):
1 GND
2 OFDC
3 OFDX
4 $V_{1X}$
5 $VH_{1AX}$
6 $VH_{1BX}$
7 $V_{2X}$
8 $V_{3X}$
9 $VH_{3AX}$
10 $VH_{3BX}$
11 $V_{4X}$
12 GND

Right pins (36–25):
36 GND
35 $TST_1$
34 $ED_2$
33 $ED_1$
32 $ED_0$
31 HD
30 VD
29 DCLK
28 CLK
27 CKO
26 CKI
25 GND

Bottom pins (13–24): $V_{DD3}$, $V_{DD3}$, PBLK, BCPX, CLPX, ADCK, FCDS, FS, SHTR, ID, $V_{DD3}$, $V_{DD3}$

(P-QFP048-0707)

## BLOCK DIAGRAM

## PIN DESCRIPTION

| PIN NO. | SYMBOL | IO SYMBOL | POLARITY | PIN NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | GND | – | – | Ground | A grounding pin. |
| 2 | OFDC | O3MR1 | ⎍ | Control pulse output for OFD voltage | A pulse to control OFD voltage. |
| 3 | OFDX | O3MR1 | ⎎ | OFD pulse output | A pulse that sweeps the charge of the photo-diode for the electronic shutter. Connect to OFD pin of the CCD through the vertical driver IC and DC offset circuit. Held at H level in normal mode. |
| 4 | V$_{1X}$ | O3MR1 | ⎍ | Vertical transfer pulse output 1 | A vertical transfer pulse for the CCD. Connect to V$_{1X}$ pin of vertical driver IC. |
| 5 | VH$_{1AX}$ | O3MR1 | ⎎ | Readout pulse output 1A | A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH$_{1AX}$ pin of vertical driver IC. |
| 6 | VH$_{1BX}$ | O3MR1 | ⎎ | Readout pulse output 1B | A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH$_{1BX}$ pin of vertical driver IC. |
| 7 | V$_{2X}$ | O3MR1 | ⎍ | Vertical transfer pulse output 2 | A vertical transfer pulse for the CCD. Connect to V$_{2X}$ pin of vertical driver IC. |
| 8 | V$_{3X}$ | O3MR1 | ⎎ | Vertical transfer pulse output 3 | A vertical transfer pulse for the CCD. Connect to V$_{3X}$ pin of vertical driver IC. |
| 9 | VH$_{3AX}$ | O3MR1 | ⎎ | Readout pulse output 3A | A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH$_{3AX}$ pin of vertical driver IC. |
| 10 | VH$_{3BX}$ | O3MR1 | ⎎ | Readout pulse output 3B | A pulse that transfers the charge of the photo-diode to the vertical shift register. Connect to VH$_{3BX}$ pin of vertical driver IC. |
| 11 | V$_{4X}$ | O3MR1 | ⎎ | Vertical transfer pulse output 4 | A vertical transfer pulse for the CCD. Connect to V$_{4X}$ pin of vertical driver IC. |
| 12 | GND | – | – | Ground | A grounding pin. |
| 13 | V$_{DD3}$ | – | – | Power supply | Supply of +3.3 V power. |
| 14 | V$_{DD3}$ | – | – | Power supply | Supply of +3.3 V power. |
| 15 | PBLK | O3MR1 | ⎎ | Pre-blanking pulse output | A pulse for pre-blanking. This pulse is controlled by serial data  BLKCNT.<br>    BLKCNT = H; This pulse stays low during the absence of effective pixels within the vertical blanking or during the sweepout signal.<br>    BLKCNT = L; Continuous pulse<br>The output phase of PBLK is selected by serial data. |

| PIN NO. | SYMBOL | IO SYMBOL | POLARITY | PIN NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 16 | BCPX | O3MR1 | ⎍ | Optical black clamp pulse output | A pulse to clamp the optical black signal.<br>This pulse is controlled by serial data BCPCNT.<br>BCPCNT = H; This pulse stays high during the absence of effective pixels within the vertical blanking or during the sweepout signal.<br>BCPCNT = L; This pulse stays high during the sweepout signal. |
| 17 | CLPX | O3MR1 | ⎍ | Clamp pulse output | A pulse to clamp the dummy outputs of the CCD signal.<br>This pulse stays high during the sweepout period. |
| 18 | ADCK | O6M32 | ⎍⎍ | AD clock output | An output pin for AD converter. The output phase of ADCK is selected by serial data in 90° steps. |
| 19 | FCDS | O6M32 | ⊔ / ⊓ | CDS pulse output 1 | A pulse to clamp the feed-through level for the CCD.<br>The output phase and output polarity of FCDS are selected by serial data. |
| 20 | FS | O6M32 | ⊔ / ⊓ | CDS pulse output 2 | A pulse to sample-hold the signal for the CCD.<br>The output phase and output polarity of FS are selected by serial data. |
| 21 | SHTR | O3MR1 | ⊓ | Trigger output | A trigger pulse for effective signal period. |
| 22 | ID | O3MR1 | ⊓⊓ | Line index pulse output | The pulse is used in the color separator.<br>The signal switches between high and low at every line. |
| 23 | VDD3 | – | – | Power supply | Supply of +3.3 V power. |
| 24 | VDD3 | – | – | Power supply | Supply of +3.3 V power. |
| 25 | GND | – | – | Ground | A grounding pin. |
| 26 | CKI | OSCI3 | – | Clock input | An input pin for reference clock oscillation.<br>The frequency is 49.0909 MHz. |
| 27 | CKO | OSCO3 | – | Clock output | An output pin for reference oscillation.<br>The output is the inverse of CKI (pin 26). |
| 28 | CLK | O6M32 | ⎍⎍ | Clock output | An output pin to generate HD and VD pulses.<br>The frequency is 24.54545 MHz. |
| 29 | DCLK | O6M32 | ⎍⎍ | Clock output | An output pin for DSP IC. The frequency is 24.54545 MHz.<br>The output phase of DCLK is selected by serial data in 90° steps. |
| 30 | VD | IC3 | ⎍ | Vertical reference pulse input | An input pin for reference of vertical pulse.<br>Connect to VD pin of DSP IC. |
| 31 | HD | IC3 | ⎍ | Horizontal drive pulse input | An input pin for reference of horizontal pulse.<br>Connect to HD pin of DSP IC. |
| 32 | ED0 | ICSD3 | – | Strobe pulse input | An input pin for the strobe pulse, to control the functions of LR38620. For details, see "**Serial Data Control**". |
| 33 | ED1 | ICSD3 | – | Shift register clock input | An input pin for the clock of the shift register, to control the functions of LR38620. For details, see "**Serial Data Control**". |

| PIN NO. | SYMBOL | IO SYMBOL | POLARITY | PIN NAME | DESCRIPTION |
|---------|--------|-----------|----------|----------|-------------|
| 34 | ED$_2$ | ICSD3 | – | Shift register data input | An input pin for the data of the shift register, to control the functions of LR38620. For details, see **"Serial Data Control"**. |
| 35 | TST$_1$ | ICD3 | – | Test pin 1 | A test pin. Set open or to L level in normal mode. |
| 36 | GND | – | – | Ground | A grounding pin. |
| 37 | V$_{DD4}$ | – | – | Power supply | Supply of +4.5 V power. |
| 38 | V$_{DD4}$ | – | – | Power supply | Supply of +4.5 V power. |
| 39 | ACLX | ICU4 | – | All clear input | An input pin for resetting all internal circuit at power-on. Connect to V$_{DD3}$ through the diode and GND through the capacitor. |
| 40 | FH$_1$ | O8M43 | ⊓ | Horizontal transfer pulse output 1 | A horizontal transfer pulse for the CCD. Connect to $\phi$H1 pin of the CCD. |
| 41 | GND | – | – | Ground | A grounding pin. |
| 42 | GND | – | – | Ground | A grounding pin. |
| 43 | FH$_2$ | O8M43 | ⊔ | Horizontal transfer pulse output 2 | A horizontal transfer pulse for the CCD. Connect to $\phi$H2 pin of the CCD. |
| 44 | FR | O8M43 | ⊔ | Reset pulse output | A pulse to reset the charge of output circuit. The output phase of FR is selected by serial data. |
| 45 | TST$_2$ | ICD4 | – | Test pin 2 | A test pin. Set open or to L level in normal mode. |
| 46 | TST$_3$ | ICD4 | – | Test pin 3 | A test pin. Set open or to L level in normal mode. |
| 47 | V$_{DD4}$ | – | – | Power supply | Supply of +4.5 V power. |
| 48 | V$_{DD4}$ | – | – | Power supply | Supply of +4.5 V power. |

IC3     : Input pin (CMOS level)

ICD3   : Input pin (CMOS level with pull-down resistor)

ICSD3 : Input pin (CMOS schmitt-trigger level with pull-down resistor)

ICD4   : Input pin (CMOS level with pull-down resistor)

ICU4   : Input pin (CMOS level with pull-up resistor)

O3MR1  : Output pin (output high level is V$_{DD3}$.)

O6M32  : Output pin (output high level is V$_{DD3}$.)

O8M43  : Output pin (output high level is V$_{DD4}$.)

OSCI3  : Input pin for oscillation

OSCO3  : Output pin for oscillation

# Serial Data Control
## SERIAL DATA INPUT TIMING
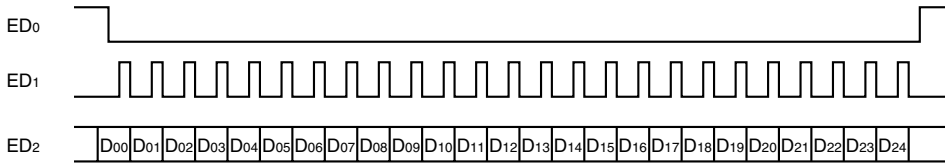


ED2 is shifted by the rising edge of ED1, and is latched by the pulse #1 which is generated after 122 to 162 ns delay from the rising edge of ED0. (See **Fig. 2**.)

The latched serial data are divided into two types by the data of $D_{00}$, and are relatched by the pulse #2 which is generated after 203 to 243 ns delay from the rising edge of ED0. (See **Fig. 1**.)

INMD is effective at the start of #3 horizontal line, and shutter control data are effective at the start of #11 horizontal line in monitoring mode and #93 horizontal line in still mode, and other data are effective at pulse #2.

ED0 should be at low level during data inputs of ED1 and ED2 or while ACLX is at low level.



**Fig. 1   Data Latch Timing**



**Fig. 2   Input Pulse Timing of ED0, ED1 and ED2**

## SERIAL DATA INPUTS

$D_{00} = L$

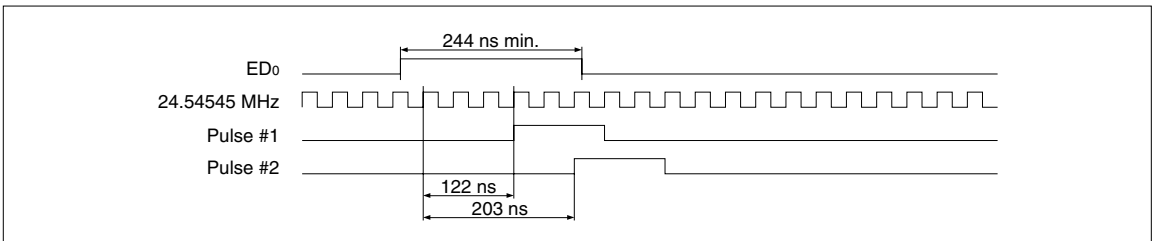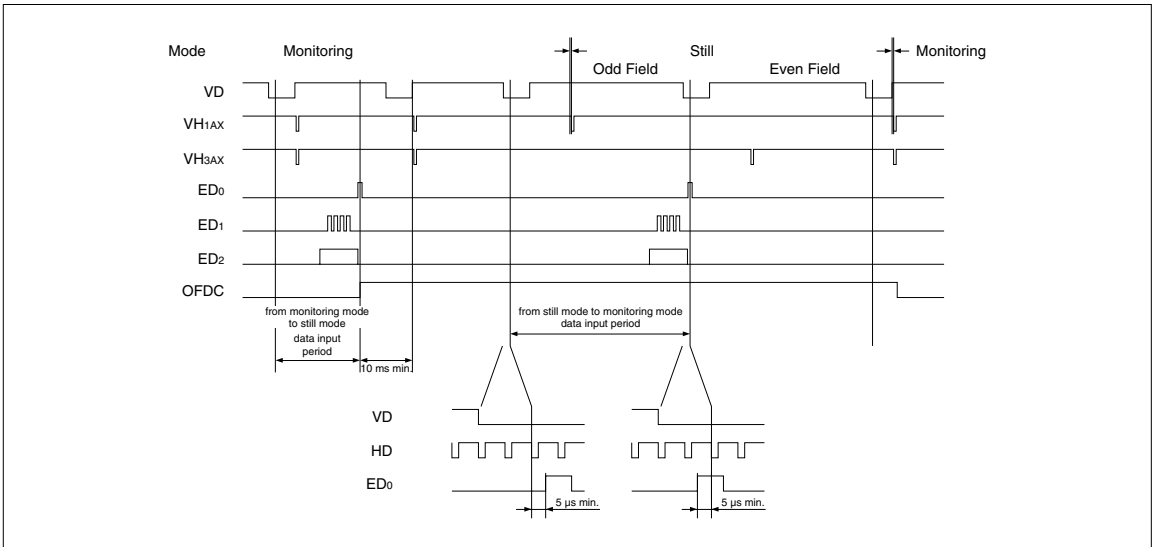| DATA | NAME | FUNCTION | DATA = L | DATA = H | AT ACLX = L |
|------|------|----------|----------|----------|-------------|
| $D_{01}$-$D_{09}$ | SDV0-SDV8 | Integration time control in field period step by horizontal period. | – | | All L |
| $D_{10}$-$D_{15}$ | SDH0-SDH5 | Dummy | Fix to L level | | All L |
| $D_{16}$ | SDF0 | Integration time control by field period. | – | | All L |
| $D_{17}$ | SDF1 | | | | |
| $D_{18}$ | SDF2 | | | | |
| $D_{19}$ | SMD | Electronic shutter mode control | – | | L |
| $D_{20}$ | PWSA | Power save control | Normal | Power save | L |
| $D_{21}$ | INMD | Integration mode control | Monitoring | Still | L |
| $D_{22}$ | Dummy | Dummy | Fix to L level | | L |
| $D_{23}$ | Dummy | Dummy | Fix to L level | | L |
| $D_{24}$ | VHCNT | VH1AX to VH3BX control | Output | Held at H level | L |

$D_{00} = H$

| DATA | NAME | FUNCTION | DATA = L | DATA = H | AT ACLX = L |
|------|------|----------|----------|----------|-------------|
| $D_{01}$ | ML1 | Phase control | – | | All L |
| $D_{02}$ | ML2 | | | | |
| $D_{03}$ | MR1 | | – | | All L |
| $D_{04}$ | MR2 | | | | |
| $D_{05}$ | MR3 | | | | |
| $D_{06}$ | MC1 | | – | | All L |
| $D_{07}$ | MC2 | | | | |
| $D_{08}$ | MC3 | | | | |
| $D_{09}$ | MS1 | | – | | All L |
| $D_{10}$ | MS2 | | | | |
| $D_{11}$ | MS3 | | | | |
| $D_{12}$ | MD1 | | – | | All L |
| $D_{13}$ | MD2 | | | | |
| $D_{14}$ | MD3 | | | | |
| $D_{15}$ | MA1 | | – | | All L |
| $D_{16}$ | MA2 | | | | |
| $D_{17}$ | Dummy | Dummy | Fix to L level | | All L |
| $D_{18}$ | Dummy | | | | |
| $D_{19}$ | Dummy | | | | |
| $D_{20}$ | MP1 | Phase control | – | | All L |
| $D_{21}$ | MP2 | | | | |
| $D_{22}$ | PLCH | Polarity control of FCDS and FS pulses | Negative | Positive | L |
| $D_{23}$ | BLKCNT | PBLK control | Continuous | Discontinuous | L |
| $D_{24}$ | BCPCNT | BCPX control | Continuous | Discontinuous | L |

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply voltage | $V_{DD3}$, $V_{DD4}$ | −0.3 to +5.5 | V |
| Input voltage | $V_{I3}$ | −0.3 to $V_{DD3}$ + 0.3 | V |
| | $V_{I4}$ | −0.3 to $V_{DD4}$ + 0.3 | V |
| Output voltage | $V_{O3}$ | −0.3 to $V_{DD3}$ + 0.3 | V |
| | $V_{O4}$ | −0.3 to $V_{DD4}$ + 0.3 | V |
| Operating temperature | $T_{OPR}$ | −20 to +70 | °C |
| Storage temperature | $T_{STG}$ | −55 to +150 | °C |

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

($V_{DD3}$ = 3.3±10%, $V_{DD4}$ = 4.5±10%, $T_{OPR}$ = −20 to +70°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Input "Low" voltage | $V_{IL3-1}$ | | | | $0.2V_{DD3}$ | V | 1, 2 |
| Input "High" voltage | $V_{IH3-1}$ | | $0.8V_{DD3}$ | | | V | |
| Input "Low" voltage | $V_{IL3-2}$ | | | | $0.2V_{DD3}$ | V | 3 |
| Input "High" voltage | $V_{IH3-2}$ | Schmitt-buffer | | | $0.75V_{DD3}$ | V | |
| Hysteresis voltage | $V_{T+} - V_{T-}$ | | $0.14V_{DD3}$ | | | V | |
| Input "Low" voltage | $V_{IL4}$ | | | | $0.2V_{DD4}$ | V | 4, 5 |
| Input "High" voltage | $V_{IH4}$ | | $0.8V_{DD4}$ | | | V | |
| Input "Low" current | $\mid I_{IL3-1} \mid$ | $V_I$ = 0 V | | | 1.0 | μA | 1 |
| Input "High" current | $\mid I_{IH3-1} \mid$ | $V_I$ = $V_{DD3}$ | | | 1.0 | μA | |
| Input "Low" current | $\mid I_{IL3-2} \mid$ | $V_I$ = 0 V | | | 3.0 | μA | 2, 3 |
| Input "High" current | $\mid I_{IH3-2} \mid$ | $V_I$ = $V_{DD3}$ | 8.0 | | 100 | μA | |
| Input "Low" current | $\mid I_{IL4-1} \mid$ | $V_I$ = 0 V | 20 | | 300 | μA | 4 |
| Input "High" current | $\mid I_{IH4-1} \mid$ | $V_I$ = $V_{DD4}$ | | | 5.0 | μA | |
| Input "Low" current | $\mid I_{IL4-2} \mid$ | $V_I$ = 0 V | | | 5.0 | μA | 5 |
| Input "High" current | $\mid I_{IH4-2} \mid$ | $V_I$ = $V_{DD4}$ | 20 | | 300 | μA | |
| Output "Low" voltage | $V_{OL3-1}$ | $I_{OL}$ = 3 mA | | | 0.4 | V | 6 |
| Output "High" voltage | $V_{OH3-1}$ | $I_{OH}$ = −2.5 mA | $V_{DD3} - 0.5$ | | | V | |
| Output "Low" voltage | $V_{OL3-2}$ | $I_{OL}$ = 12 mA | | | 0.4 | V | 7 |
| Output "High" voltage | $V_{OH3-2}$ | $I_{OH}$ = −10 mA | $V_{DD3} - 0.5$ | | | V | |
| Output "Low" voltage | $V_{OL4}$ | $I_{OL}$ = 20 mA | | | 0.4 | V | 8 |
| Output "High" voltage | $V_{OH4}$ | $I_{OH}$ = −20 mA | $V_{DD4} - 0.5$ | | | V | |

**NOTES :**

1. Applied to inputs (IC3, OSCI3).
2. Applied to input (ICD3).
3. Applied to input (ICSD3).
4. Applied to input (ICU4).
5. Applied to input (ICD4).

6. Applied to outputs (OSCO3, O3MR1). (Output (OSCO3) measures on condition that input (OSCI3) level is 0 V or $V_{DD3}$.)
7. Applied to output (O6M32).
8. Applied to output (O8M43).

## PACKAGE OUTLINES

### 48 QFP (P-QFP048-0707)

(Unit : mm)