LR38637

Digital Signal Processor For VGA/CIF CMOS Image Sensors

DESCRIPTION

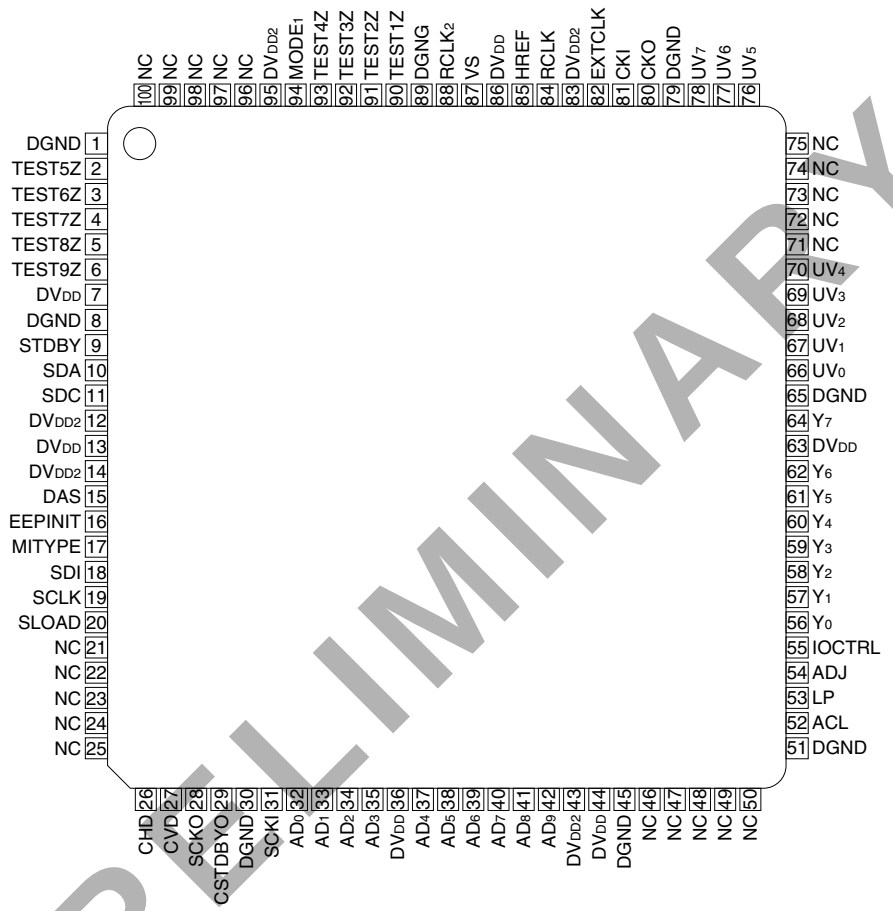
The LR38637 is a CMOS digital signal processor for color digital video camera systems of 110 k-pixel (CIF)/350 k-pixel (VGA) CMOS image sensors with primary color mosaic filters.

FEATURES

- Supported CMOS image sensors
  - Image size : 110 k pixels (CIF)/350 k pixels (VGA)
  - R, G and B primary color mosaic filters : Bayer matrix, 10 bits per color
- Built-in synchronous signal generation circuit for CMOS image sensors
- Built-in parallel digital output function
  - 16-bit outputs : YUV, RGB format
  - 8-bit outputs : UYVY format
- Output image sizes for VGA CMOS image sensors : VGA, QVGA, QQVGA, CIF, QCIF, QQCIF
- Output image sizes for CIF CMOS image sensors : QVGA, QQVGA, CIF, QCIF, QQCIF
- Used for video cameras by combining with CMOS image sensor
- Parameters required for image signal processing can be changed
- Built-in auto exposure control
- Built-in auto carrier balance control
- Built-in auto white balance control
- Built-in drive circuit for 2k-bit EEPROM
- Built-in auto white detect correction
- Built-in shading correction control
- Power supplies
  - +2.5 V±10% for internal digital circuits
  - +2.7 to +3.6 V for digital circuits
- Package :
  100-pin LQFP (P-LQFP100-1414) 0.5 mm pin-pitch

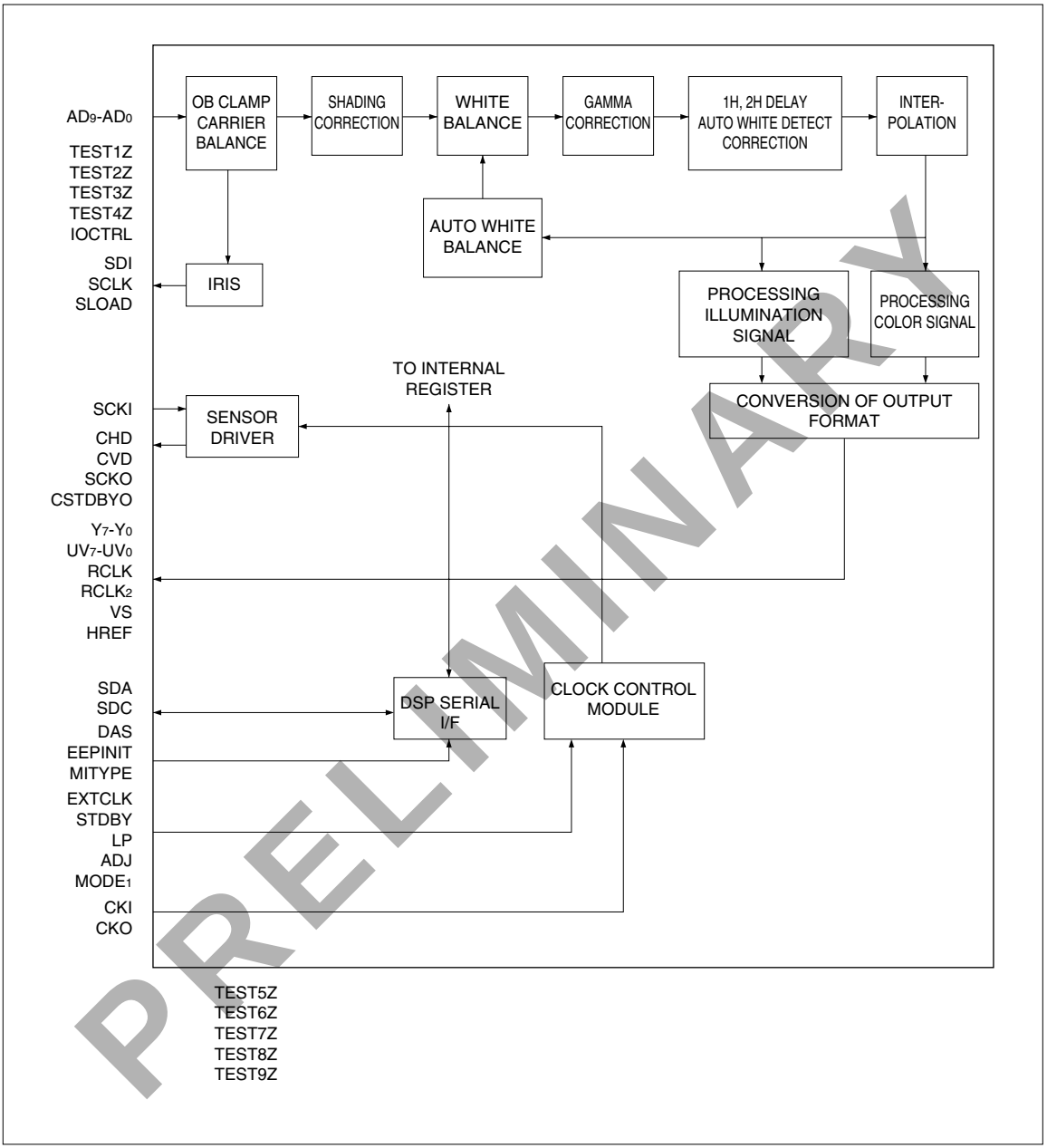
PIN CONNECTIONS

100-PIN LQFP TOP VIEW



(P-LQFP100-1414)

BLOCK DIAGRAM



PIN DESCRIPTION

PIN NO.	SYMBOL	IO SYMBOL	DESCRIPTION
1	DGND	–	Ground
2	TEST5Z	–	Test input (Must be open.) (NOTE 4)
3	TEST6Z	–	Test input (Must be open.) (NOTE 4)
4	TEST7Z	–	Test input (Must be open.) (NOTE 4)
5	TEST8Z	–	Test input (Must be open.) (NOTE 4)
6	TEST9Z	–	Test input (Must be open.) (NOTE 4)
7	DV_{DD}	–	Internal power supply (+2.5 V)
8	DGND	–	Ground
9	STDBY	IL	Standby mode control Low level input : The LR38637 and CMOS image sensor are in normal mode. High level input : The LR38637 and CMOS image sensor are in standby mode.
10	SDA	IOL4	DSP serial data input/output (NOTE 5, 6)
11	SDC	IOL4	DSP serial clock input/output (NOTE 5, 6)
12	DV_{DD2}	–	I/O power supply (+3.0 V)
13	DV_{DD}	–	Internal power supply (+2.5 V)
14	DV_{DD2}	–	I/O power supply (+3.0 V)
15	DAS	I	DSP DAS device address input
16	EEPINIT	I	Control of auto reading from EEPROM. Low level input : The LR38637 does NOT read automatically from EEPROM. High level input : The LR38637 reads automatically from EEPROM.
17	MITYPE	I	Connect to High level (+3.0 V).
18	SDI	O4	Serial data output for CMOS image sensor
19	SCLK	O4	Serial clock output for CMOS image sensor
20	SLOAD	O4	Serial load output for CMOS image sensor
21	NC	–	Must be open.
22	NC	–	Must be open.
23	NC	–	Must be open.
24	NC	–	Must be open.
25	NC	–	Must be open.
26	CHD	O4	Horizontal drive pulse output for CMOS image sensor
27	CVD	O4	Vertical drive pulse output for CMOS image sensor
28	SCKO	O4	Clock output for CMOS image sensor
29	CSTDBYO	O12	Standby control output to CMOS image sensor Low level output : CMOS image sensor is in normal mode. High level output : CMOS image sensor is in standby mode.
30	DGND	–	Ground
31	SCKI	I	Clock input from CMOS image sensor
32	AD_0	I	Digital input bit 0
33	AD_1	I	Digital input bit 1
34	AD_2	I	Digital input bit 2
35	AD_3	I	Digital input bit 3

PIN NO.	SYMBOL	IO SYMBOL	DESCRIPTION
36	DV_{DD}	–	Internal power supply (+2.5 V)
37	AD_4	I	Digital input bit 4
38	AD_5	I	Digital input bit 5
39	AD_6	I	Digital input bit 6
40	AD_7	I	Digital input bit 7
41	AD_8	I	Digital input bit 8
42	AD_9	I	Digital input bit 9
43	DV_{DD2}	–	I/O power supply (+3.0 V)
44	DV_{DD}	–	Internal power supply (+2.5 V)
45	DGND	–	Ground
46	NC	–	Must be open.
47	NC	–	Must be open.
48	NC	–	Must be open.
49	NC	–	Must be open.
50	NC	–	Must be open.
51	DGND	–	Ground
52	ACL	IS	Reset input (low active)
53	LP	I	Lower power mode control Low level input : The LR38637 and CMOS image sensor are in normal mode. High level input : The LR38637 and CMOS image sensor are in low power mode.
54	ADJ	I	Connect to Low level (+0.0 V)
55	IOCTRL	I	Switch input/output of parallel video output. (NOTE 7)
56	Y_0	IO4	Digital video output (NOTE 8)
57	Y_1	IO4	Digital video output (NOTE 8)
58	Y_2	IO4	Digital video output (NOTE 8)
59	Y_3	IO4	Digital video output (NOTE 8)
60	Y_4	IO4	Digital video output (NOTE 8)
61	Y_5	IO4	Digital video output (NOTE 8)
62	Y_6	IO4	Digital video output (NOTE 8)
63	DV_{DD}	–	Internal power supply (+2.5 V)
64	Y_7	IO4	Digital video output (NOTE 8)
65	DGND	–	Ground
66	UV_0	IO4	Digital video output (NOTE 8)
67	UV_1	IO4	Digital video output (NOTE 8)
68	UV_2	IO4	Digital video output (NOTE 8)
69	UV_3	IO4	Digital video output (NOTE 8)
70	UV_4	IO4	Digital video output (NOTE 8)
71	NC	–	Must be open.
72	NC	–	Must be open.
73	NC	–	Must be open.

PIN NO.	SYMBOL	IO SYMBOL	DESCRIPTION
74	NC	–	Must be open.
75	NC	–	Must be open.
76	UV_5	IO4	Digital video output. (NOTE 8)
77	UV_6	IO4	Digital video output. (NOTE 8)
78	UV_7	IO4	Digital video output. (NOTE 8)
79	DGND	–	Ground
80	CKO	OSC	System clock oscillator output
81	CKI	IA	System clock oscillator input
82	EXTCLK	IAC	Connect to High level (+3.0 V) .
83	DV_{DD2}	–	I/O power supply (+3.0 V)
84	RCLK	O4	Clock output synchronized with digital video output
85	HREF	O4	Horizontal blank pulse of digital video output
86	DV_{DD}	–	Internal power supply (+2.5 V)
87	VS	O4	Vertical blank pulse of digital video output
88	$RCLK_2$	O4	Separated video output
89	DGND	–	Ground
90	TEST1Z	IU	Test input (Must be open.) (NOTE 3)
91	TEST2Z	IU	Test input (Must be open.) (NOTE 3)
92	TEST3Z	IU	Test input (Must be open.) (NOTE 3)
93	TEST4Z	IU	Test input (Must be open.) (NOTE 3)
94	$MODE_1$	I	Connect to Low level (+0.0 V).
95	DV_{DD2}	–	I/O power supply (+3.0 V)
96	NC	–	Must be open.
97	NC	–	Must be open.
98	NC	–	Must be open.
99	NC	–	Must be open.
100	NC	–	Must be open.

I : Input pin
IL : Input pin
IS : Schmidt input pin
IU : Input pin with pull-up resistor
O4 : Output pin
O12 : Output pin
IO4 : Input/output pin
IOL4 : Schmidt input/output pin (Nch open drain)
IA : Input pin for oscillation
OSC : Output pin for oscillation
IAC : Input pin for external clock

REMARKS :

PIN TYPE (MAX. OUTPUT CURRENT)	APPLICABLE PINS
+3.0 V output pin (10 m A)	CSTDBYO
+3.0 V I/O pin (3 mA) or output pin (3 mA)	SDA, SDC, SDI, SCLK, SLOAD, CHD, CVD, SCKO, Y_0 to Y_7, UV_0 to UV_7, RCLK, HREF, VS, $RCLK_2$

NOTES :

1. Be careful that an input pin doesn't have a floating potential.
2. Be careful not to have a floating potential when an I/O pin is set to input.
3. Keep test pins TEST1Z to TEST4Z normally open or "High level".
4. Keep test pins TEST5Z to TEST9Z normally open.
5. SDA and SDC are input pins at resetting (ACL is Low level).
6. SDA and SDC are N-ch open-drain outputs, so use them with external pulled-up resistor.
7. When an IOCTRL pin is at High condition, the image output pins (Y_0 to Y_7, UV_0 to UV_7) are input pins.
8. The output form of the image output pins (Y_0 to Y_7, UV_0 to UV_7) can be changed by parameter setting.

FUNCTIONAL DESCRIPTION

Oscillation Circuit

Oscillation circuit leads the same frequency of the quartz crystal connected to I/O pins and provides the same frequency to the internal logic circuits as shown in **Fig. 1** and **Fig. 2**.

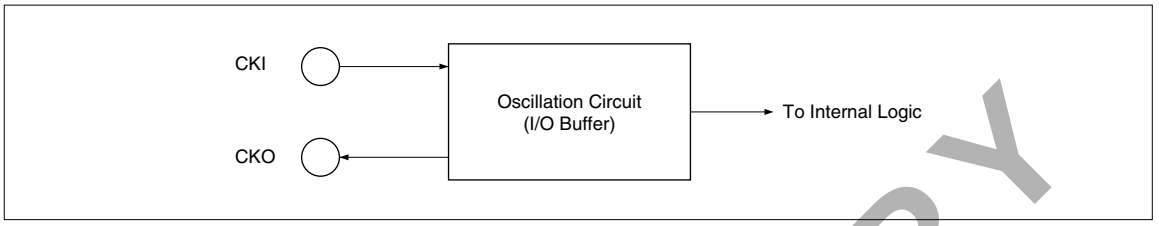


Fig. 1 Block Diagram of Oscillation Circuit

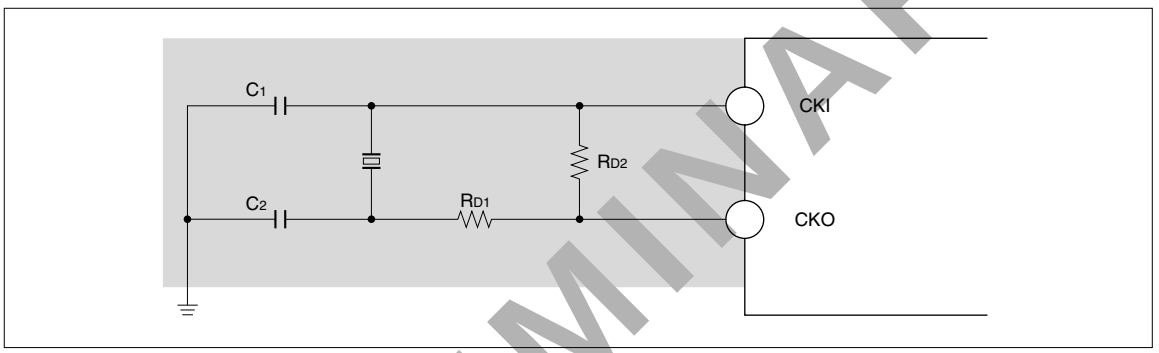


Fig. 2 Clock Input to Oscillation Circuit

Connection of Quartz Crystal (T_A = −20 to +70°C, DV_{DD2} = 2.7 to 3.6 V, DV_{DD} = 2.25 to 2.75 V) : Example of Oscillation under Fundamental Frequencies

APPLICABLE PINS	FUNDAMENTAL FREQUENCY [MHz]	RECOMMENDED COEFFICIENT			
		C_1 [pF]	C_2 [pF]	R_{D1} [Ω]	R_{D2} [Ω]
CKI, CKO	24.5454 or 9.0000	10	10	220	1 M

NOTES :

1. The oscillation circuit should be located as close to CKI, CKO as possible.
2. Do not install other signal lines in the shaded area.
3. Perform due evaluation on the match between the LR38637 and the quartz crystal.

Clock

Input clock from the CKI pin is supplied to CMOS image sensor through the SCKO pin after dividing according to inside parameter of the LR38637.
Set the EXTCLK pin to open or "High level".
The clock frequency which can be inputted to the CKI input pin is 24.5454 MHz or 9 MHz.

Power ON/OFF Sequence

Two power supplies are used with the LR38637. One (DV_{DD2}) is used for I/O buffer and the other (DV_{DD}) is used for the core logic circuits.

Power ON : Be sure to turn ON the internal power of DV_{DD} first.

Power OFF : Be sure to turn OFF the I/O buffer of DV_{DD2} first.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
I/O power supply voltage	DV_{DD2}	−0.3 to +4.3	V
Internal power supply voltage	DV_{DD}	−0.3 to +3.3	V
Input voltage	V_{I2}	−0.3 to DV_{DD2} + 0.3	V
Output voltage	V_{O2}	−0.3 to DV_{DD2} + 0.3	V
Storage temperature	T_{STG}	−65 to +150	˚C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply voltage	DV_{DD2}	I/O digital power supply	2.7	3.0	3.6	V
	DV_{DD}	Internal digital power supply	2.25	2.50	2.75	V
Operating temperature	T_{OPR}		−20	+25	+70	˚C
Operating frequency	f_{OPR}	Internal logic		12.27		MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(DV_{DD2} = 3.0 V, DV_{DD} = 2.5 V, T_A = −20 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage 1	V_{IL1}				$0.3DV_{DD2}$	V	1
Input "High" voltage 1	V_{IH1}		$0.7DV_{DD2}$			V	
Input "Low" voltage 2	V_{IL2}				$0.2DV_{DD2}$	V	2
Input "High" voltage 2	V_{IH2}		$0.8DV_{DD2}$			V	
Positive trigger voltage	V_{T^+}		1.24			V	3
Negative trigger voltage	V_{T^-}				1.21	V	
Hysteresis voltage	$V_{T^+} - V_{T^-}$		0.17			V	
Hysteresis voltage	V_{HYS}		$0.1DV_{DD2}$			V	4
Input leakage current	I_{I2}	V_{IN} = 0V to DV_{DD2}	−1.0		+1.0	µA	5
		V_{IN} = DV_{DD2} [with pull-up 98 kΩ]	−5.0		+5.0	µA	6
Input "Low" current	I_{IL}	V_{IN} = 0 V		−30		µA	
Output "Low" voltage 1	V_{OL1}	I_{OL} = 3 mA			$0.2DV_{DD2}$	V	7
Output "Low" voltage 2	V_{OL2}	I_{OL} = 3 mA			0.5	V	8
Output "High" voltage 2	V_{OH2}	I_{OH} = −3 mA	DV_{DD2} − 0.5			V	
Output "Low" voltage 3	V_{OL3}	I_{OL} = 10 mA			0.5	V	9
Output "High" voltage 3	V_{OH3}	I_{OH} = −7 mA	DV_{DD2} − 0.5			V	
Oscillation frequency	F_{OSC}			24.5454		MHz	10

(DV_{DD2} = 3.0 V, DV_{DD} = 2.5 V, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply current	I_{DD}	Input : VGA sensor Output : 15 fps, parallel output • This value is reference value with our evaluation environment.		TBD		mA	11
Standby current	P_{SB}	• This value is reference value with our evaluation environment.		TBD		µA	12

NOTES :

1. Applicable to IO symbols IL, IOL4.
2. Applicable to IO symbol I, IU, IO4.
3. Applicable to IO symbol IS.
4. Applicable to IO symbol IOL4.
5. Applicable to IO symbols I, IO4, IS, IL, IOL4.
6. Applicable to IO symbol IU.
7. Applicable to IO symbol IOL4.
8. Applicable to IO symbols O4, IO4.
9. Applicable to IO symbol O12.
10. Applicable to IO symbols IA (CKI), OSC (CKO).
11. Test conditions
    Connected 8-bit CMOS image sensor :
    VGA image sensor/VGA mode
    External clock :
    MODE1 = "Low", EXTCLK = "High", CKI = 24.5454 MHz
    Output frame rate : CLK_MODE = "001" (15 frames/s)
    Parallel output :
    Operation (IOCTRL = "Low", Y_0 to Y_7, UV_0 to UV_7 = "Open"
    Output format : YUV (OUT_SEL = "00")
    Output frame size : VGA (640 x 480)
12. Test conditions
    STDBY, EXTCLK, SDA, SDC, MODE1 = "High",
    CKI, IOCTRL, DAS, EEPINIT, MITYPE, SCKI, AD_0 to AD_9, ACL, LP, ADJ = "Low",
    CKO, Y_0 to Y_7, UV_0 to UV_7, TEST1Z to TEST9Z, SDI, SCLK, SLOAD, CHD, CVD, SCKO, CSTDBYO, RCLK, HREF, VS, $RCLK_2$ = "Open"

AC Characteristics

CMOS IMAGE SENSOR INTERFACE TIMING

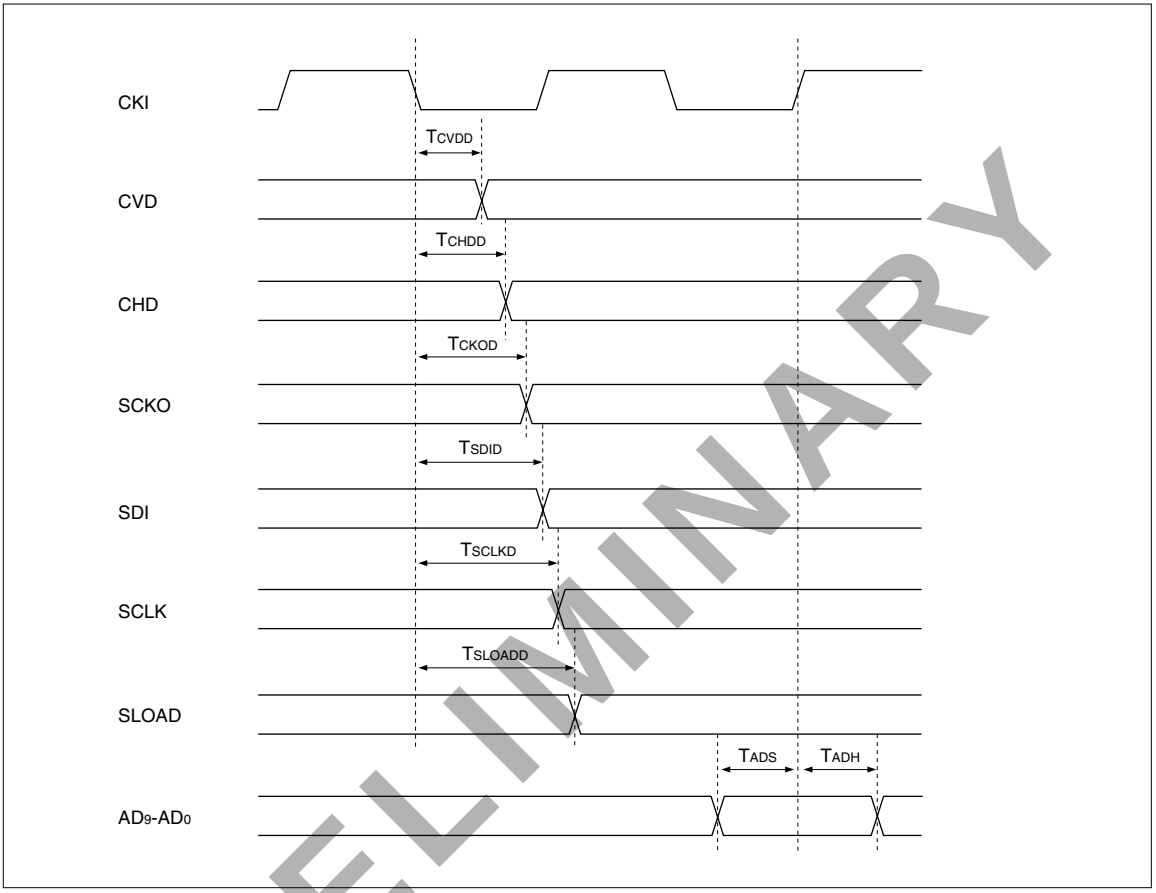


Fig. 3 CMOS Image Sensor Interface Timing

(DV_{DD2} = 3.0 V, DV_{DD} = 2.5 V, T_A = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
CVD output delay	T_{CVDD}		15	ns	1
CHD output delay	T_{CHDD}		15	ns	1
SCKO output delay	T_{SCKOD}		15	ns	1
SDI output delay	T_{SDID}		15	ns	1
SCLK output delay	T_{SCLKD}		15	ns	1
SLOAD output delay	T_{SLOADD}		15	ns	1
Setup time of AD_9-AD_0 input data	T_{ADS}	10		ns	1
Hold time of AD_9-AD_0 input data	T_{ADH}	10		ns	1

NOTE :

1. Output load capacitance C_L = 15 pF

DIGITAL PARALLEL OUTPUT TIMING

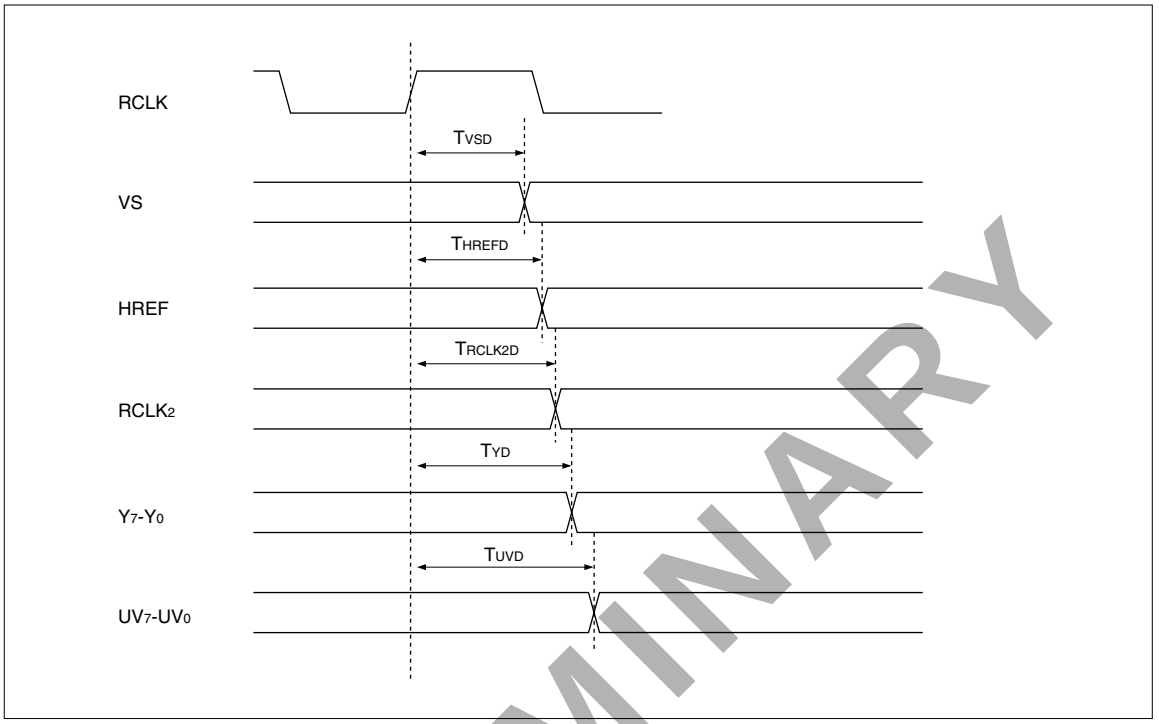


Fig. 4 Digital Parallel Output Timing

(DV_{DD2} = 3.0 V, DV_{DD} = 2.5 V, T_A = −20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
VS output delay	T_{VSD}	−15	+15	ns	1
HREF output delay	T_{HREFD}	−15	+15	ns	1
$RCLK_2$ output delay	T_{RCLK2D}	−15	+15	ns	1
Y_7 to Y_0 output delay	T_{YD}	−15	+15	ns	1
UV_7 to UV_0 output delay	T_{UVS}	−15	+15	ns	1

NOTE :

1. Output load capacitance C_L = 15 pF

DSP SERIAL INTERFACE TIMING

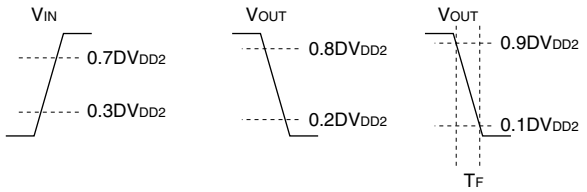


Fig. 5 I/O Level and Rising Time

HOST I/F TIMING

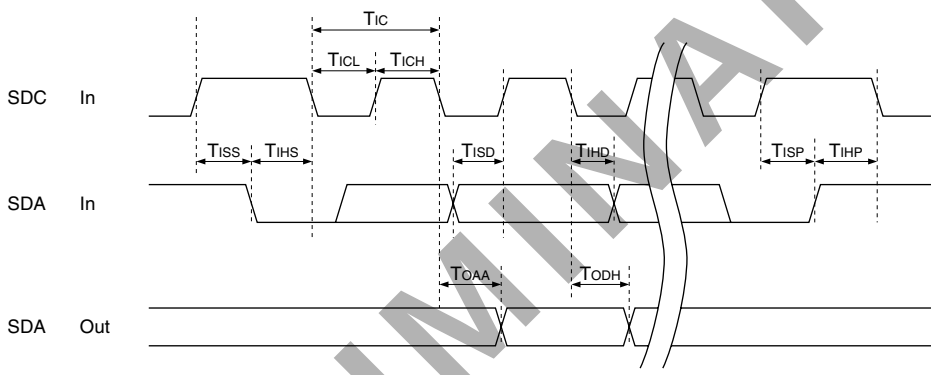


Fig. 6 Host I/F Timing

(DVDD2 = 3.0 V, DVDD = 2.5 V, TA = –20 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Operating clock frequency	TIC		400	kHz	
High clock period	TICH	0.1		µs	
Low clock period	TICL	0.2		µs	
Setup time of start condition	TISS	0.1		µs	
Hold time of start condition	TIHS	0.1		µs	
Setup time of input data	TISD	0.1		µs	
Hold time of input data	TIHD	0		µs	
Output delay	TOAA	0		µs	1
Hold time of output data	TODH	0		µs	1
Setup time of stop condition	TISP	0.1		µs	
Hold time of stop condition	TIHP	0.1		µs	
Falling period	TF		300	ns	1

NOTE :

1. Output load capacitance CL = 15 pF

EEPROM I/F TIMING

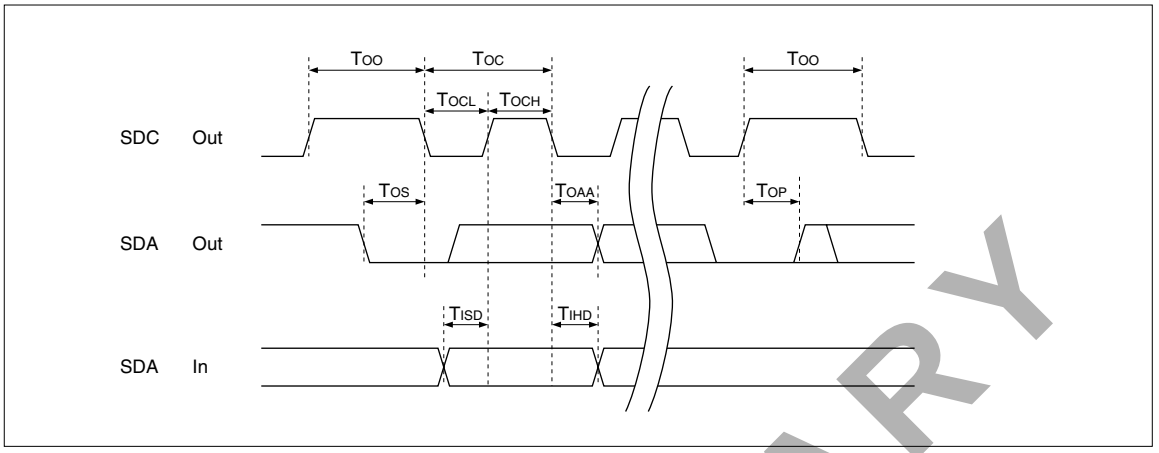


Fig. 7 EEPROM I/F Timing

(DV_{DD2} = 3.0 V, DV_{DD} = 2.5 V, T_A = −20 to +70˚C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Operating clock frequency	T_{OC}	0	56.93	kHz	1, 2
High clock period	T_{OCH}	8.78		µs	1, 2
Low clock period	T_{OCL}	8.78		µs	1, 2
Start condition output delay	T_{OS}	17.56		µs	1, 2
Setup time of input data	T_{ISD}	1		µs	
Hold time of input data	T_{IHD}	0		µs	
Output delay	T_{OAA}	4.39		µs	1, 2
Stop condition output delay	T_{OP}	26.34		µs	1, 2
SDC bus release time	T_{OO}	70.24		µs	1, 2

NOTES :

1. Output load capacitance C_L = 15 pF
2. Available maximum clock frequency is 24.5454 MHZ (CKI).

PACKAGE OUTLINES

100 LQFP (P-LQFP100-1414)

(Unit : mm)