SHARP

To

SPEC No.	CCD3-062-PD00
ISSUE:	Feb.28, 2006

SPECIFICATION
(Preliminary)

Product Type: **Signal processing LSI for 270,000-470,000 pixel CCD**

Model No.: **LR38653**

*This document contains 28 pages including the cover page and the appendix.

If you have any objections, please contact us before issuing your purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: K. Misawa

Dept. General Manager

REVIEWED BY:	PREPARED BY:
M. Fukuda	Y. Nakade

Product Development Dept.III
Imaging and Sensing Module Division
Large-Scale IC Group
SHARP CORPORATION

■ Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.

■ When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment, which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communication equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three paragraphs to a sales representative of the company.

■ Please direct all queries regarding the products covered herein to the sales representative of the company.

Table of Contents

1. OUTLINE 2

2. TERMINAL ASSIGNMENT 3

3. TERMINAL EXPLANATION 6

4. BLOCK DIAGRAM 10

5. ELECTRICAL CHARACTERISTICS 11

6. APPEARANCE AND PACKING SPECIFICATION 18

1. Outline

This product is the LSI which has the signal processing part which has the signal process function which converts the timing pulse which drives 270 - 470-thousand pixels CCD, pulse generating with all kinds for the television signal and the CCD image information which was changed into the digital signal into the video signal, and the driver part of the vertical transfer pulse for CCD and the AFE part which accumulated the CDS, the PGA, and the AD converter.

1.1. Functions

- The power source voltage: 4 powers of 15 V, -8 V, 3.3 V and 1.8V.
- It corresponds to the CCD area sensor of 270-thousand and 410-thousand pixels for NTSC, and 320-thousand and 470-thousand pixels for PAL.
- It corresponds to an NTSC standard, PAL standard.
- CCD input gain (Analog level) variable range:-8-36dB
- 18MHz and 9bit AD converter are contained.
- Generating circuit for the CCD drive signal and various pulses for television signals is contained.
  For the output with 2 level values for vertical CCD drive: Built-in 2 circuits.
  For the output with 3 level values for vertical CCD drive: Built-in 2 circuits.
  For the output with 2 level values for electronic shutter: Built-in 1 circuit.
- The parameter with all kinds which is necessary to process a camera signal is possible variably.
- 4K bit EEPROM Read/Write function for the adjustment parameter storage.
  (EEPROM uses the one which has the Page-write function of equal to or more than 16 bytes).
- The automatic exposure control function is equipped.
- The automatic white balance control function is equipped.
- The automatic carrier balance equalizer function is equipped.
- The line crawling correction function is equipped.
- The white blemish correction function is equipped.
- The luminance signal, the color signal independence gamma correction circuit.
- Lens shading compensation.
- The strong glare (Blackout) correction function.
- The analog composite video is outputted. (10bit DA converter)
- YUV digital output (8bit x 2) is selectable.
- The video output of the mirror image function is equipped.
- The package material is plastic.
- The package is 171 pin CSP (the pin pitch of 0.5 mm).
- Lead free compatible.
- CMOS is used in circuit design and construction.

* Not designed or rated as radiation hardened
* Please refer to a technical manual about the directions of each function, and the details of restrictions. However, priority is given to this paper about specification.

* SHARP takes no responsibility for any problems related to any intellectual property right of a third party resulting from the use of SHARP devices.

2. Terminal assignment

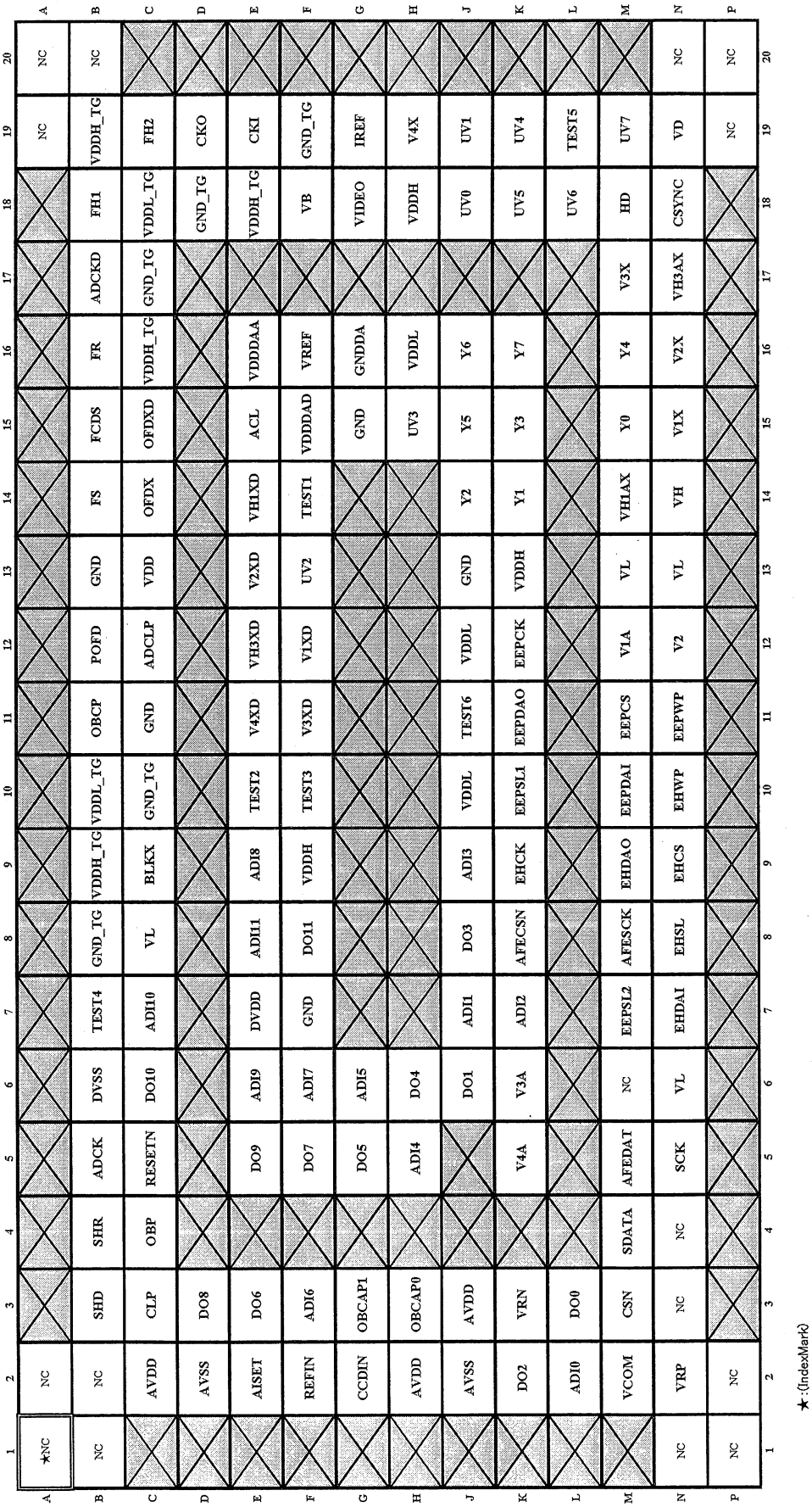
2.1. Terminal assignment table

No.	SIGNAL	I/O	Power	No.	SIGNAL	I/O	Power	No.	SIGNAL	I/O	Power
B3	SHD	I	B	E16	VDDDAA	VDDDAA	J	K5	V4A	O_20	D,E
B4	SHR	I	B	E18	VDDH_TG	VDDH_TG	H	K6	V3A	O_20	D,E
B5	ADCK	I	B	E19	CKI	OSC_I	H	K7	ADI2	IS	G
B6	DVSS	GND		F2	REFIN	I_A	A	K8	AFECSN	O_4	G
B7	TEST4	I_D	G	F3	ADI6	IS	G	K9	EHCK	IOS_4	G
B8	GND_TG	GND		F5	DO7	O_1	B	K10	EEPSL1	IS_D	G
B9	VDDH_TG	VDDH_TG	H	F6	ADI7	IS	G	K11	EEPDAO	IOS_4	G
B10	VDDL_TG	VDDL	F	F7	GND	GND		K12	EEPCK	IOS_4	G
B11	OBCP	O_4	H	F8	DO11	O_1	B	K13	VDDH	VDDH	G
B12	POFD	O_20	D,E	F9	VDDH	VDDH	G	K14	Y1	IO_4	G
B13	GND	GND		F10	TEST3	I_D	H	K15	Y3	IO_4	G
B14	FS	O_4	H	F11	V3XD	O_4	H	K16	Y7	IO_4	G
B15	FCDS	O_4	H	F12	V1XD	O_4	H	K18	UV5	IO_4	G
B16	FR	O_4	H	F13	UV2	IO_4	G	K19	UV4	IO_4	G
B17	ADCKD	O_4	H	F14	TEST1	I_D	H	L2	ADI0	IS	G
B18	FH1	O_16	H	F15	VDDDAD	VDDDAD	K	L3	DO0	O_1	B
B19	VDDH_TG	VDDH_TG	H	F16	VREF	I_A	J	L18	UV6	IO_4	G
C2	AVDD	AVDD	A	F18	VB	O_A	J	L19	TEST5	I_D	G
C3	CLP	I	B	F19	GND_TG	GND		M2	VCOM	O_A	A
C4	OBP	I	B	G2	CCDIN	I_A	A	M3	CSN	I	B
C5	RESETN	I	B	G3	OBCAP1	O_A	A	M4	SDATA	I	B
C6	DO10	O_1	B	G5	DO5	O_1	B	M5	AFEDAT	O_4	G
C7	ADI10	IS	G	G6	ADI5	IS	G	M7	EEPSL2	IS_D	G
C8	VL	VL	E	G15	GND	GND		M8	AFESCK	O_4	G
C9	BLKX	O_4	H	G16	GNDDA	GND		M9	EHDAO	IOS_4	G
C10	GND_TG	GND		G18	VIDEO	O_A	J	M10	EEPDAI	IOS_4	G
C11	GND	GND		G19	IREF	O_A	J	M11	EEPCS	O_4	G
C12	ADCLP	O_4	H	H2	AVDD	AVDD	A	M12	V1A	O_20	D,E
C13	VDD	VDD	C	H3	OBCAP0	O_A	A	M13	VL	VL	E
C14	OFDX	I_U	C	H5	ADI4	IS	G	M14	VH1AX	I_U	C
C15	OFDXD	O_4	H	H6	DO4	O_1	B	M15	Y0	IO_4	G
C16	VDDH_TG	VDDH_TG	H	H15	UV3	IO_4	G	M16	Y4	IO_4	G
C17	GND_TG	GND		H16	VDDL	VDDL	F	M17	V3X	I_U	C
C18	VDDL_TG	VDDL	F	H18	VDDH	VDDH	G	M18	HD	O_4	G
C19	FH2	O_16	H	H19	V4X	I_U	C	M19	UV7	IO_4	G
D2	AVSS	GND		J2	AVSS	GND		N2	VRP	O_A	A
D3	DO8	O_1	B	J3	AVDD	AVDD	A	N5	SCK	I	B
D18	GND_TG	GND		J6	DO1	O_1	B	N6	VL	VL	E
D19	CKO	OSC_O	H	J7	ADI1	IS	G	N7	EHDAI	IOS_4	G
E2	AISET	I_A	A	J8	DO3	O_1	B	N8	EHSL	IS_D	G
E3	DO6	O_1	B	J9	ADI3	IS	G	N9	EHCS	IS	G
E5	DO9	O_1	B	J10	VDDL	VDDL	F	N10	EHWP	IS	G
E6	ADI9	IS	G	J11	TEST6	I_D	G	N11	EEPWP	O_4	G
E7	DVDD	DVDD	B	J12	VDDL	VDDL	F	N12	V2	O_20	E
E8	ADI11	IS	G	J13	GND	GND		N13	VL	VL	E
E9	ADI8	IS	G	J14	Y2	IO_4	G	N14	VH	VH	D
E10	TEST2	I_D	H	J15	Y5	IO_4	G	N15	V1X	I_U	C
E11	V4XD	O_4	H	J16	Y6	IO_4	G	N16	V2X	I_U	C
E12	VH3XD	O_4	H	J18	UV0	IO_4	G	N17	VH3AX	I_U	C
E13	V2XD	O_4	H	J19	UV1	IO_4	G	N18	CSYNC	O_4	G
E14	VH1XD	O_4	H	K2	DO2	O_1	B	N19	VD	O_4	G
E15	ACL	IS_U	H	K3	VRN	O_A	A	others	NC	—	

The symbols "A"-"K" of the power column shows the power sorting-out of the buffer output.

I/O Symbol	I/O Type
I	CMOS level input terminal
IS	Schmidt level input terminal
I_D	CMOS level input terminal (pull-down resistance 84 kΩ contained)
I_U	CMOS level input terminal (pull-up resistance 100 kΩ contained)
IS_D	Schmidt level input terminal (pull-down resistance 84 kΩ contained)
IS_U	Schmidt level input terminal (pull-up resistance 96kΩ contained)
I_A	Analog input terminal
IO_4	Input and output terminals CMOS level input Capable output current is 4mA.
IOS_4	Input and output terminals schmidt level input Capable output current is 4mA.
O_1	Output terminals Capable output current is 1mA. (when the power is 3V)
O_4	Output terminals Capable output current is 4mA. (when the power is 3.3V)
O_16	Output terminals Capable output current is 16mA. (when the power is 3.3V)
O_20	Output terminals Capable output current is 20mA. (when the power VDD is 3V, VH=15V, VL=-8V)
O_A	Analog output terminal
OSC_I	Input terminal for the oscillation circuit
OSC_O	Output terminal for the oscillation circuit
GND	Ground
AVDD	Power source A: Analog power source (3.0V~3.6V)
DVDD	Power source B: Digital power source (3.0V~3.6V)
VDD	Power source C: IO power source. (3.0V~3.6V)
VH	Power source D: Power source for V-Driver. (10V~20V)
VL	Power source E: Power source for V-Driver. (-10V~-5V)
VDDL	Power source F: Internal core power source. (1.62V~1.98V)
VDDH	Power source G: IO power source. (3.0V~3.6V)
VDDH_TG	Power source H: IO power source. (3.0V~3.6V)
VDDDAA	Power source J: Analog power source for DA converter. (3.0V~3.6V)
VDDDAD	Power source K: Digital power source for DA converter. (3.0V~3.6V)

2.2. CSP terminal arrangement (TOP view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	★NC	NC																	NC	NC
B	NC	NC	SHD	SHR	ADCK	DVSS	TEST4	GND_TG	VDDH_TG	VDDL_TG	OBCP	POFD	GND	FS	FCDS	FR	ADCKD	FH1	VDDH_TG	NC
C		AVDD	CLP	OBP	RESETN	DO10	ADI10	VL	BLKX	GND_TG	GND	ADCLP	VDD	OFDX	OFDXD	VDDH_TG	GND_TG	VDDL_TG	FH2	
D		AVSS	DO8		DO9	ADI9	DVDD	ADI11	ADI8	TEST2	V4XD	VH3XD	V2XD	VH1XD	ACL	VDDDAA		GND_TG	CKO	
E		AISET	DO6		DO7	ADI7	GND	DO11	VDDH	TEST3	V3XD	V1XD	UV2	TEST1	VDDDAD	VREF		VB	GND_TG	
F		REFIN	ADI6		DO5	ADI5									GND	GNDDA		VIDEO	IREF	
G		CCDIN	OBCAP1		ADI4	DO4									UV3	VDDL		VDDH	V4X	
H		AVDD	OBCAP0												Y5	Y6		UV0	UV1	
J		AVSS	AVDD		V4A	DO1	ADI1	DO3	ADI3	VDDL	TEST6	VDDL	GND	Y2	Y3	Y7		UV5	UV4	
K		DO2	VRN		V3A	ADI2	AFECSN	EHCK	EEPSL1	EEPDAO	EEPCK	VDDH	Y1	Y1	Y0	VH1AX	V3X	HD	UV7	
L		ADI0	DO0												V1X	VH		UV6	TEST5	
M		VCOM	CSN	SDATA	AFEDAT	NC	EEPSL2	AFESCK	EHDAO	EEPDAI	EEPCS	V1A	VL	VH1AX	Y0	Y4	V2X	VH3AX	CSYNC	VD
N		NC	VRP	NC	SCK	VL	EHDAI	EHSL	EHCS	EHWP	EEPWP	V2	VL	VH	V1X	V2X	VH3AX	CSYNC	VD	NC
P		NC	NC																NC	NC

★:(IndexMark)

3. Terminal explanation

Pin No.	Signal	I/O	Function
A1	NC	-	Make open. (It connect with A2 and B1 inside)
A2	NC	-	Make open. (It connect with A1 and B1 inside)
A19	NC	-	Make open. (It connect with A20 and B20 inside)
A20	NC	-	Make open. (It connect with A19 and B20 inside)
B1	NC	-	Make open. (It connect with A1 and A2 inside)
B2	NC	-	Make open.
B3	SHD	I	Data sampling pulse input. (Connect to B14.)
B4	SHR	I	Reference sampling pulse input. (Connect to B15.)
B5	ADCK	I	AD Converter sampling clock input. (Connect to B17.)
B6	DVSS	GND	Digital output driver ground terminal.
B7	TEST4	I_D	Test terminal. Make open or ground (Note.1)
B8	GND_TG	GND	Ground terminal.
B9	VDDH_TG	VDDH_TG	Power source terminal for I/O. (3.3V)
B10	VDDL_TG	VDDL	Power source terminal for internal core. (1.8V)
B11	OBCP	O_4	OB pixel clamp pulse output terminal. (Connect to C4.)
B12	POFD	O_20	Electronic shutter pulse output Connect to the appropriate terminal of CCD via the capacitor.
B13	GND	GND	Ground terminal.
B14	FS	O_4	Output terminal of sample hold pulse. (Connect to B3.)
B15	FCDS	O_4	Output terminal of sample hold pulse. (Connect to B4.)
B16	FR	O_4	Reset transistor gate clock pulse output Connect to the appropriate terminal of CCD via the capacitor.
B17	ADCKD	O_4	AD converter sampling clock output. (Connect to the B5.)
B18	FH1	O_16	Horizontal shift register gate clock pulse output. Connect to the appropriate terminal of CCD.
B19	VDDH_TG	VDDH_TG	Power source terminal for I/O. (3.3V)
B20	NC	-	Make open. (It connect with A19 and A20 inside)
C2	AVDD	AVDD	Analog power source terminal. (3.3V)
C3	CLP	I	Clamp control signal input. (Connect to C12.)
C4	OBP	I	Pulse input for the black level detection. (Connect to B11.)
C5	RESETN	I	AFE reset input terminal. (Active Low)
C6	DO10	O_1	AD converter output terminal bit10. (Connect to C7.)
C7	ADI10	IS	Video input terminal bit10. (Connect to C6.)
C8	VL	VL	Power source terminal. (-8V)
C9	BLKX	O_4	Blanking output terminal. (Make OPEN.)
C10	GND_TG	GND	Ground terminal.
C11	GND	GND	Ground terminal.
C12	ADCLP	O_4	AD input clamp pulse output terminal. (Connect toC3)
C13	VDD	VDD	Power source terminal. (3.3V)
C14	OFDX	I_U	Overflow drain shutter pulse input. (Connect to C15.)
C15	OFDXD	O_4	Overflow drain shutter pulse output. (Connect to C14.)
C16	VDDH_TG	VDDH_TG	Power source terminal for I/O. (3.3V)
C17	GND_TG	GND	Ground terminal.
C18	VDDL_TG	VDDL	Power source terminal for internal core. (1.8V)
C19	FH2	O_16	Horizontal shift register gate clock pulse output. Connect to the appropriate terminal of CCD.
D2	AVSS	GND	Analog ground terminal.
D3	DO8	O_1	AD converter output terminal1 bit8. (Connect to E9.)
D18	GND_TG	GND	Ground terminal.
D19	CKO	OSC_O	Clock generation output terminal. Oscillation circuit of crystal oscillator is structured with the adjacent CKI (E19).

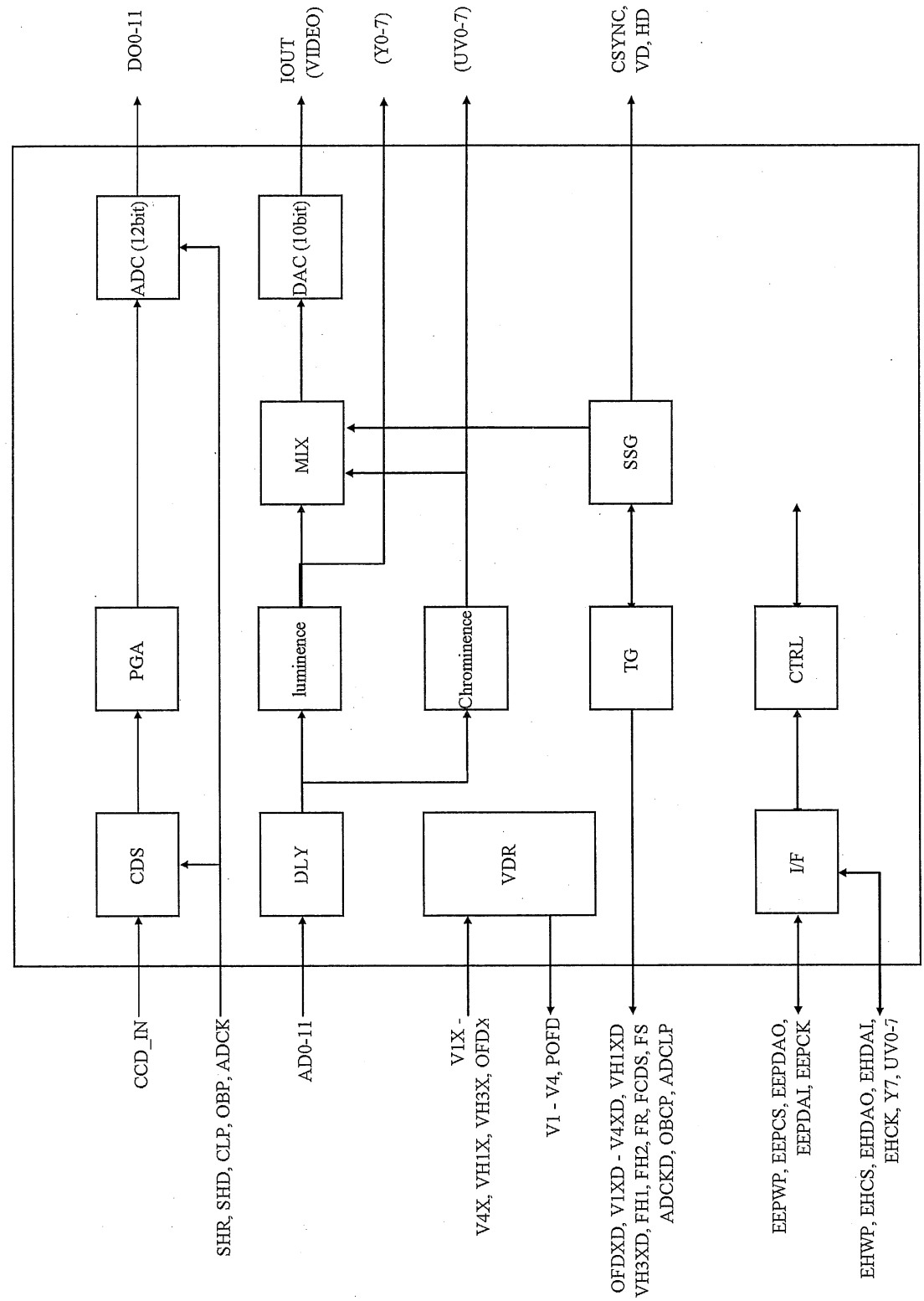
Pin No.	Signal	I/O	Function
E2	AISET	I_A	Internal analog circuit bias power input. (It connects 8.2 kΩ resistance with the between of AVSS (D2).)
E3	DO6	O_1	AD converter output terminal1 bit6. (Connect to F3.)
E5	DO9	O_1	AD converter output terminal1 bit9. (Connect to E6.)
E6	ADI9	IS	Video input terminal bit9. (Connect to E5.)
E7	DVDD	DVDD	Digital output driver power source terminal. (3.3V)
E8	ADI11	IS	Video input terminal bit11(MSB). (Connect to F8.)
E9	ADI8	IS	Video input terminal bit8. (Connect to D3.)
E10	TEST2	I_D	Test terminal. Make open or ground (Note 1) When YUV terminal used as input for control, input high level.
E11	V4XD	O_4	Vertical shift register gate clock pulse output. (Connect to H19.)
E12	VH3XD	O_4	Electric charge read-in pulse output. (Connect to N17.)
E13	V2XD	O_4	Vertical shift register gate clock pulse output. (Connect to N16.)
E14	VH1XD	O_4	Electric charge read-in pulse output. (Connect to M14.)
E15	ACL	IS_U	DSP reset input terminal.
E16	VDDDAA	VDDDAA	Power source terminal for DA converter. (Analog)
E18	VDDH_TG	VDDH_TG	Power source terminal. for I/O. (3.3V)
E19	CKI	OSC_I	Clock generation input terminal. Oscillation circuit of crystal oscillator is structured with the adjacent CKO (D19). Crystal oscillator frequency used as NTSC: 28.63636MHz PAL: 28.375MHz)
F2	REFIN	I_A	Reference input terminal in CDS circuit. (It connects 0.1uF capacitor with the between of AVSS.)
F3	ADI6	IS	Video input terminal bit6. (Connect to E3.)
F5	DO7	O_1	AD converter output terminal1 bit7. (Connect to F6.)
F6	ADI7	IS	Video input terminal bit7. (Connect to F5.)
F7	GND	GND	Ground terminal.
F8	DO11	O_1	AD converter output terminal bitl1 (MSB). (Connect to E8.)
F9	VDDH	VDDH	Power source terminal. for I/O. (3.3V)
F10	TEST3	I_D	Test termina3. Make open or ground (Note 1) When YUV terminal used as input for control, input high level.
F11	V3XD	O_4	Vertical shift register gate clock pulse output. (Connect to M17.)
F12	V1XD	O_4	Vertical shift register gate clock pulse output. (Connect to N15.)
F13	UV2	IO_4	Digital video chrominance difference output terminal bit2. When TEST2=TEST3=High, input terminal for WB control.
F14	TEST1	I_D	Test terminal 1. Make open or ground
F15	VDDDAD	VDDDAD	Power source terminal for DA converter. (Digital)
F16	VREF	O_A	Input terminal for DA converter. Supply DC1.2V.
F18	VB	I_A	Output terminal for DA converter. Ground via the capacitor.
F19	GND_TG	GND	Ground terminal.
G2	CCDIN	I_A	CCD signal input terminal.
G3	OBCAP1	O_A	Black level integral output voltage. (It connects 0.1uF capacitor with the between of AVSS and OBCAP0 (H3).)
G5	DO5	O_1	AD converter output terminal1 bit5. (Connect to G6.)
G6	ADI5	IS	Video input terminal bit 5. (Connect to G5.)
G15	GND	GND	Ground terminal.
G16	GNDDA	GND	Ground terminal for DA converter.
G18	VIDEO	O_A	DA converter video output terminal. Ground via the resistor.
G19	IREF	O_A	Output terminal for DA converter. Ground via the resistor.
H2	AVDD	AVDD	Analog power source terminal. (3.3V)
H3	OBCAP0	O_A	Black level integral output voltage. (It connects 0.1uF capacitor with the between of AVSS and OBCAP1 (G3).)

Pin No.	Signal	I/O	Function
H5	ADI4	IS	Video input terminal bit4. (Connect to H6.)
H6	DO4	O_1	AD converter output terminal bit4. (Connect to H5.)
H15	UV3	IO_4	Digital video chrominance difference output terminal bit3. When TEST2=TEST3=High, input terminal for WB control
H16	VDDL	VDDL	Power source terminal for internal core. (1.8V)
H18	VDDH	VDDH	Power source terminal for I/O. (3.3V)
H19	V4X	I_U	Vertical shift register gate clock pulse input. (Connect to E11.)
J2	AVSS	GND	Analog ground terminal.
J3	AVDD	AVDD	Analog power source terminal. (3.3V)
J6	DO1	O_1	AD converter output terminal bit1. (Connect to J7.)
J7	ADI1	IS	Video input terminal bit1. (Connect to J6.)
J8	DO3	O_1	AD converter output terminal bit3. (Connect to J9.)
J9	ADI3	IS	Video input terminal bit3. (Connect to J8.)
J10	VDDL	VDDL	Power source terminal for internal core. (1.8V)
J11	TEST6	I_D	Test terminal 6. Make open or ground. (Note1)
J12	VDDL	VDDL	Power source terminal for internal core. (1.8V)
J13	GND	GND	Ground terminal.
J14	Y2	IO_4	Digital video output terminal bit2.
J15	Y5	IO_4	Digital video output terminal bit5. When TEST2=TEST3=High, used as test input, make ground.
J16	Y6	IO_4	Digital video output terminal bit6. When TEST2=TEST3=High, used as test input, make ground.
J18	UV0	IO_4	Digital video chrominance difference output terminal bit0 (LSB). When TEST2=TEST3=High, input terminal for MIR control.
J19	UV1	IO_4	Digital video chrominance difference output terminal bit1. When TEST2=TEST3=High, input terminal for BLC control.
K2	DO2	O_1	AD converter input terminal bit2. (Connect to K7.)
K3	VRN	O_A	AD converter internal negative reference voltage. (It connects 0.1uF capacitor with the between of AVSS and VRP (N2)) (Note 2)
K5	V4A	O_20	Vertical CCD drive pulse with three-values output. Connect to the appropriate terminal of CCD.
K6	V3A	O_20	Vertical CCD drive pulse with three-values output. Connect to the appropriate terminal of CCD.
K7	ADI2	IS	Video input terminal bit2. (Connect to K2.)
K8	AFECSN	O_4	Chip select output terminal for serial port (Active Low). (Connect to M3.)
K9	EHCK	IOS_4	Clock input terminal from the external host for communication. Connect to the external clock output terminal.
K10	EEPSL1	IS_D	Make open or ground.
K11	EEPDAO	IOS_4	Make open.
K12	EEPCK	IOS_4	Clock output terminal to the EEPROM. Connect to the clock input terminal of the EEPROM.
K13	VDDH	VDDH	Power source for I/O. (3.3V)
K14	Y1	IO_4	Digital video output terminal bit1.
K15	Y3	IO_4	Digital video output terminal bit3.
K16	Y7	IO_4	Digital video output terminal bit7 (MSB). When TEST2=TEST3=High , input terminal for the AGC control. 0: Normal, 1: AGC fix.
K18	UV5	IO_4	Digital video chrominance difference output terminal bit5. When TEST2=TEST3=High, input terminal for EEMD control.
K19	UV4	IO_4	Digital video chrominance difference output terminal bit4. When TEST2=TEST3=High, input terminal for EEMD control.
L2	ADI0	IS	Video input terminal bit0. (Connect to L3.)
L3	DO0	O_1	AD converter output terminal bit0 (LSB). (Connect to L2.)
L18	UV6	IO_4	Digital video chrominance difference output terminal bit6. When TEST2=TEST3=High, input terminal for EEMD control.

Pin No.	Signal	I/O	Function
L19	TEST5	I_D	Test terminal 5. Make open or ground. (Note1)
M2	VCOM	O_A	AD converter internal common voltage. Connect to the AVSS via the capacitor.
M3	CSN	I	Chip select input terminal for serial port. (Active Low) (Connect to K8.)
M4	SDATA	I	Chip select input terminal for serial port. (Connect to M5.)
M5	AFEDAT	O_4	Chip select input terminal for serial port. (Connect to M4.)
M6	NC	-	Make open.
M7	EEPSL2	IS_D	Control terminal to choose EEPROM. When initial reading from EEPROM, it uses by the Low level. (0: Initial automatic reading enable, 1: No Read)
M8	AFESCK	O_4	Clock output terminal for serial port. (Connect to N5.)
M9	EHDAO	IOS_4	Make open.
M10	EEPDAI	IOS_4	Data input/output terminal from the EEPROM. Connect to the data terminal of EEPROM.
M11	EEPCS	O_4	Make open.
M12	V1A	O_20	Vertical CCD drive pulse with three-values output. Connect to the appropriate terminal of CCD.
M13	VL	VL	Power source terminal. (-8V)
M14	VH1AX	I_U	Electric charge read-in pulse input. (Connect to E14.)
M15	Y0	IO_4	Digital video output terminal bit0 (LSB).
M16	Y4	IO_4	Digital video output terminal bit4.
M17	V3X	I_U	Vertical shift register gate clock pulse input. (Connect to F11.)
M18	HD	O_4	Horizontal drive output terminal.
M19	UV7	IO_4	Digital video chrominance difference output terminal bit7 (MSB). When TEST2=TEST3=High, input terminal for EEMD control.
N1	NC	-	Make open. (It connect with P1 and P2 inside)
N2	VRP	O_A	AD converter internal positive reference voltage. Connect to the AVSS and the VRN (K3) via the capacitor valued 0.47μF.
N3	NC	-	Make open.
N4	NC	-	Make open.
N5	SCK	I	Clock terminal for serial port. (Connect to M8.)
N6	VL	VL	Power source terminal. (-8V)
N7	EHDAI	IOS_4	Data input/output terminal from the external host for communication. Connect to the external data output (input/output) terminal.
N8	EHSL	IS_D	Make open or ground.
N9	EHCS	IS	Control terminal for the DSP register access. Select the slave device address (0: "1010000Xb", 1: "1100000Xb")
N10	EHWP	IS	Control terminal for the DSP register write protect. (Low Enable)
N11	EEPWP	O_4	Control terminal for the EEPROM write protect. (Low Enable)
N12	V2	O_20	Vertical CCD drive two values pulse output. Connect to the appropriate terminal of CCD.
N13	VL	VL	Power source terminal. (-8V)
N14	VH	VH	Power source terminal. (15V)
N15	V1X	I_U	Vertical shift register gate clock pulse input. (Connect to F12.)
N16	V2X	I_U	Vertical shift register gate clock pulse input. (Connect to E13.)
N17	VH3AX	I_U	Electric charge read-in pulse output (Connect to E12.)
N18	CSYNC	O_4	Composite SYNC pulse or pixel clock (RCLK) output terminal
N19	VD	O_4	Vertical drive output terminal.
N20	NC	-	Make open. (It connect with P19 and P20 inside)
P1	NC	-	Make open. (It connect with N1 and P2 inside)
P2	NC	-	Make open. (It connect with N1 and P1 inside)
P19	NC	-	Make open. (It connect with N20 and P20 inside)
P20	NC	-	Make open. (It connect with N20 and P19 inside)

(Note1) There is possibility that the individual setting is necessary to the EEPROM access.
Being under, give us contact to the details.

4. Block diagram



5. Electrical characteristics

5.1. Absolute Maximum rate

Items	Symbol	Rated value	Unit	Note
Power source voltage	AVDD, DVDD	-0.3 ~ 4.5	V	Power source A,B
	VDD	-0.3 ~ 7.0	V	Power source C
	VH−VL	33.0	V	Power source D,E
	VDDL	-0.3 ~ 2.2	V	Power source F
	VDDH, VDDH_TG, VDDDAA, VDDDAD	-0.3 ~ 4.3	V	Power source G,H,J,K
Input voltage	V_{Ia}	-0.3 ~ AVDD+0.3	V	Power source A
	V_{Ib}	-0.3 ~ DVDD+0.3	V	Power source B
	V_{Ic}	-0.3 ~ VDD+0.3	V	Power source C
	V_{If}	-0.3 ~ VDDL+0.3	V	Power source F
	V_{Ig}	-0.3 ~ VDDH+0.3	V	Power source G
	V_{Ih}	-0.3 ~ VDDH_TG+0.3	V	Power source H
	V_{Ij}	-0.3 ~ VDDDAA+0.3	V	Power source J
	V_{Ik}	-0.3 ~ VDDDAD+0.3	V	Power source K
Output voltage	V_{Og}	-0.3 ~ VDDH+0.3	V	Power source G
	V_{Oh}	-0.3 ~ VDDH_TG+0.3	V	Power source H
	V_{Oj}	-0.3 ~ VDDDAA+0.3	V	Power source J
	V_{Ok}	-0.3 ~ VDDDAD+0.3	V	Power source K
Storage temperature	T_{stg}	-55 ~ 150	°C	

There is a problem to cause the permanent destruction of the device in the operation over the limit shown in the above. The operation under an extreme situation isn't guaranteed

5.2. Operating conditions

Items	Symbol	Min.	Typ.	Max.	Unit
Power source voltage	AVDD, DVDD, VDD, VDDH, VDDH_TG, VDDDAA, VDDDAD	3.0	3.3	3.6	V
	VH	10	15	20	V
	VL	-10	-8	-5	V
	VH-VL	15	23	30	V
	VDDL	1.62	1.8	1.98	V
Operating temperature	Ta	-30	25	85	°C
Input clock	CKI	10	NTSC:28.63636 PAL:28.375	30	MHz

5.3. Electrical characteristics 1

An electric characteristic about Power sources A and B is shown below.

5.3.1. CDS, Clamp part

(Power source A(AVDD), B(DVDD)=3.0V,T_a=25°C, Sampling frequency=25MHz)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Input range	V_{ICDS}	When setting to Black level code = 0, PGA gain = 0db (It is the lower direction than the clamp voltage)	0.8	1.1		V	1
Input capacity	C_{IN}	CCDIN		10		pF	
Input bandwidth(BW)	C_{bw}	CCDIN ~ ADC When setting to PGA gain = 0db		1		pixel	2
Clamp voltage	V_{CLP}		1.55	1.7	1.86	V	3

Note.1: The CCDIN input level when the AD converter output reaches [FFFh].

Note.2: It defines as the settling time of ADC to the step input by $0.8V_{p-p}$.

Note.3: It is the level that the CCDIN, REFIN terminal is clamped.

5.3.2. PGA part

(Power source A(AVDD), B(DVDD)=3.0V,T_a=25°C, Sampling frequency=25MHz)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
PGA Minimum gain	GMin	Relative value with the 0db to the input of CCDIN~ADC.	-9	-8	-7	db	
PGA Maximum gain	GMax		35	36	37	db	
PGA gain step width	GSta	Monotony guarantee	0	0.043	0.086	db	

5.3.3. AD comverter part

(Power source A(AVDD), B(DVDD)=3.0V,T_a=25°C, Sampling frequency=25MHz)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Resolution	RES				12	bit	
Differential non-linearity	DNL	Guarantee of no missing code		TBD	TBD	LSB	
Integral non-linearity	INL	Guarantee of no missing code		TBD		LSB	
Common voltage	VCom		1.05	1.2	1.35	V	
Positive side reference voltage	VRP		1.55	1.7	1.85	V	
Negative side reference voltage	VRN		0.55	0.7	0.85	V	

5.3.4. Black calibration

(Power source A(AVDD), B(DVDD)=3.0V,T_a=25°C, Sampling frequency=25MHz)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Band pass (Time constant)	T_{BLKCAL}	1 time setting (default)		180		us	1
		128 time setting		1.4		us	1

Note1: Time constant τ at 1 time of the setting becomes as in the following equation.

τ =C0*600 [us]

C0 = (external capacity between OBCAP0 and OBCAP1) *2

+ (external capacity between OBCAP0 (OBCAP1) and AVSS)

External capacity between OBCAP0, OBCAP1~AVSS = 0.1uF

External capacity between OBCAP0 and OBCAP1 =0.1uF

5.3.5. Noise

(Power source A(AVDD), B(DVDD)=3.0V,T_a=25°C, Sampling frequency=25MHz)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Noise	N_T	PGA gain = 0db setting		TBD		LSBmrs	1
		PGA gain = 30db setting		TBD		LSBmrs	1

Note1: It defines as AD Converter output cord looseness σ about the time without input.

5.4. Electrical characteristics 2

An electric characteristic about Power sources C, D and E is shown below.

5.4.1. DC characteristic

(Power source C(VDD)=3.0V, D(VH)=15V, E(VL)= -8V,Ta= -30~75°C)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
H level input voltage	VIH		0.8VDD		VDD	V	
L level input voltage	VIL		0		0.2VDD	V	
H level input current	| I IH|	VIN=VDD			±1	uA	
L level input voltage	| I IL|	VIN=0V, VDD=3.0V		33	100	uA	
H level output voltage	VOH1	IOH = -20mA	VH-0.40	VH-0.23	VH-0.13	V	2
	VOH2	IOH = -20mA	VH-0.58	VH-0.36	VH-0.20	V	3
L level output voltage	VOL1	IOL = 20mA	VL+0.13	VL+0.23	VL+0.40	V	1,2
	VOL2	IL = 20mA	VL+0.16	VL+0.28	VL+0.48	V	3
Middle level output voltage	VOM1	IOM = 20mA	0.13	0.25	0.47	V	1,2
	VOM2	IOM = -20mA	-0.47	-0.25	-0.13	V	1,2

(Power source C(VDD)=3.0V, D(VH)=10~20V, E(VL)= -10~ -8V,Ta= -30~75°C)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
H level output voltage	VOH1	IOH = -20mA	VH-0.60		VH-0.10	V	2
	VOH2	IOH = -20mA	VH-0.90		VH-0.17	V	3
L level output voltage	VOL1	IOL = 20mA	VL+0.10		VL+0.60	V	1,2
	VOL2	IL = 20mA	VL+0.14		VL+0.75	V	3
Middle level output voltage	VOM1	IOM = 20mA	0.10		1.10	V	1,2
	VOM2	IOM = -20mA	-1.10		-0.10	V	1,2

VDD in the above-mentioned table shows power source C (VDD) in the corresponding buffer.

Note1: It applies to the output terminal with 2 values of power sources D, E.

Note2: It applies to the output terminal with 3 values of power sources D, E.

Note3: It applies to the electronic shutter output terminal (POFD) of power sources D, E.

5.4.2. AC characteristic

(Power source C(VDD)=3.3±0.3V, D(VH)=15V, E(VL)= -8V,Ta= -30~75°C)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Delay time	TPLM	VL→VM	40		75	ns	
	TPMH	VM→VH	55		100	ns	
	TPLH	VL→VH	40		75	ns	
	TPHM	VH→VM	55		100	ns	
	TPML	VM→VL	40		75	ns	
	TPHL	VH→VL	40		75	ns	
Rise time	TPLM	VL→VM	200		380	ns	
	TPMH	VM→VH	240		450	ns	
	TPLH	VL→VH	40		75	ns	
Fall time	TPHM	VH→VM	240		450	ns	
	TPML	VM→VL	200		380	ns	
	TPHL	VH→VL	40		75	ns	

5.5. Electrical characteristics 3

An electric characteristic about Power sources F, G, H, J and K is shown below.

5.5.1. DC characteristic

(Power source F(VDDL)=1.8V±0.18V, G(VDDH), H(VDDH_TG)=3.3V±0.3V, T_a= -30~85°C)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
H level input voltage	VIH1		0.8VDDH			V	1
L level input voltage	VIL1				0.2VDDH	V	
H level input voltage	VIH1		0.8VDDH			V	2
L level input voltage	VIL1				0.2VDDH	V	
Hysteresis	VHIS1		0.05VDDH			V	
H level input current	|IIH1|	VIN = VDD	-1.0		1.0	μA	3
L level input current	|IIL1|	VIN = 0V	-1.0		1.0	μA	
H level input current	|IIH3|	VIN = VDD	-2.0		2.0	μA	4
L level input current	|IIL3|	VIN = 0V	10		100	μA	
H level input current	|IIH4|	VIN = VDD	10		100	μA	5
L level input current	|IIL4|	VIN = 0V	-2.0		2.0	μA	
H level output voltage	VOH1	I OH = 4mA	0.8VDDH			V	6
L level output voltage	VOL1	I OL = - 4mA			0.2VDDH	V	
H level output voltage	VOH2	I OH = 12mA	0.8VDDH			V	7
L level output voltage	VOL2	I OL = -12mA			0.2VDDH	V	
H level output voltage	VOH3	I OH = 3mA	0.8VDDL			V	8
L level output voltage	VOL3	I OL = 3mA			0.2VDDL	V	

VDDH in the above-mentioned table shows the power source kind (G, H) of the corresponding buffer.

Note1: It applies to the input terminal (I_D, I_U) and input-output pin (IO_4) of power sources G, H, J and K.

Note2: It applies to the input terminal (IS, IS_U, IS_D) and input-output terminal (IOS_4) of power sources G, H, J and K.

Note3: It applies to the input terminal (OSC_I) of power sources G, H, J and K.

Note4: It applies to the input terminal (IS_U) of power sources G, H, J and K.

Note5: It applies to the input terminal (I_D, IS_D) of power sources G, H, J and K.

Note6: It applies to the input-output terminal (IO_4, IOS_4) and output terminal (O_4) of power sources G, H, J and K

Note7: It applies to the output terminal (O_16) of power sources G, H, J and K.

Note8: It applies to the output terminal (OSC_O) of power sources G, H, J and K.

5.5.2. DA converter part

(Power source J(VDDDAA), K(VDDDAD)=3.3V±0.3V, T_a= -30~85°C)

Items	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Note
Resolution	RES			10		Bit	1
Linearity error	EL	Vref = 1.2 V Rref = 9.3kΩ Rout = 150Ω			TBD	LSB	
Differential linearity error	ED				TBD	LSB	
Full scale current	IFS			8		mA	
Full code output amplitude	OFS		1.1	1.2	1.3	V	
Output load resistance	Rout		75	150		Ω	
Reference voltage	Vref		1.0	1.2	1.3	V	2
Reference resistance	Rref		4.5	9.3		kΩ	3

Note1: It applies to VIDEO terminal.

Set the ratio to 64 times with the value of the output load resistance and the value of the reference resistance +400 Ω.

Note 2: It applies to VREF terminal.

Note 3: It applies to IREF terminal.

6 Package and packing specification

[Applicability]

This specification applies to an IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% (Relative humidity) max.
- Storage period : One year max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : ? hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : ? hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : ? hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

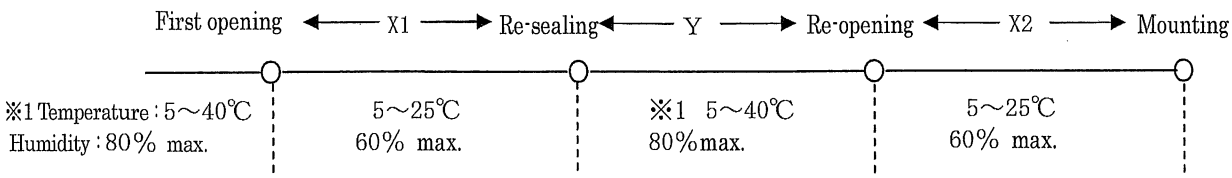
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1＋X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period :
  120+10/-0℃ for 2~3 hours.
- The above baking conditions apply since the trays are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

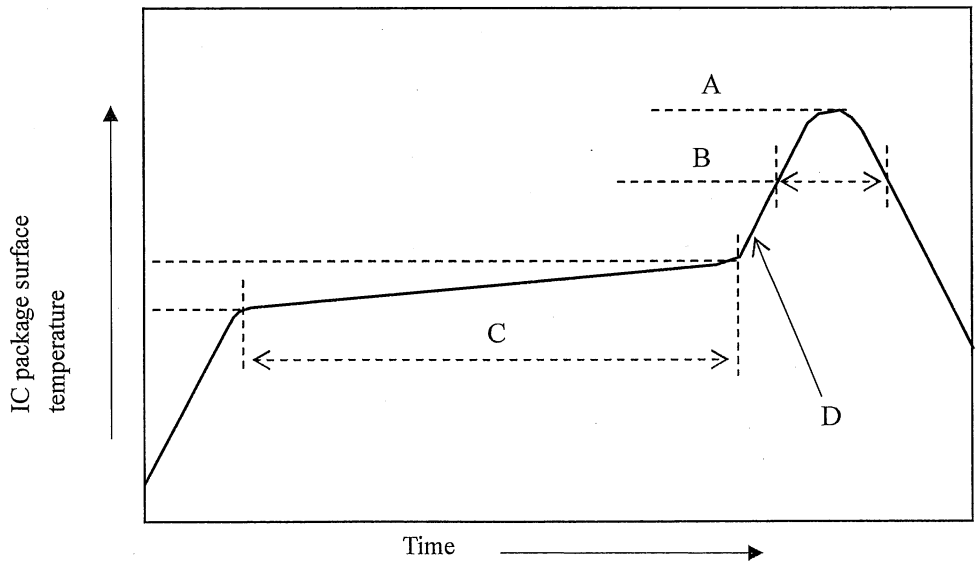
3. Surface mount conditions.

The following soldering conditions are recommended to ensure device quality.
(Use paste recommends Sn-Ag-Cu paste. However, Sn-Pb paste is not recommended.)

3-1.Soldering.

(1) Convection reflow or IR/Convection reflow. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  - A) Peak temperature. 250℃ max.
  - B) Heating temperature. 40 to 60 seconds as 220℃
  - C) Preheat temperature. It is 150 to 200℃, and is 120±30 seconds
  - D) Temperature increase rate. It is 1 to 3℃/seconds
- Measuring point : IC package surface.
- Temperature profile :



3-2.Recommended heating condition for repair.

Pre heating : 100℃ or more within 90 sec. from room temperature to 90±30 sec.
Reflow heating : within ten sec. at a temperature of 250℃ to 260℃
(Please confirm not only melting solder of the repair area but also the back of the PCB.)

Use of an "Under-fill"
Since the external terminal is using 0.5mm max. ball pitch, this product recommends using of an "Under-fill" for maintaining the same reliability as the conventional 0.8mm ball pitch.

4. Condition for removal of residual flux.
(1) Ultrasonic washing power : 25 watts / liter max.
(2) Washing time : Total 1 minute max.
(3) Solvent temperature : 15～40℃

5. Package outline specification.
Refer to the attached drawing.
(Plastic body dimensions do not include burr of resin.)
The contents of LEAD-FREE TYPE application of the specifications. (*2)

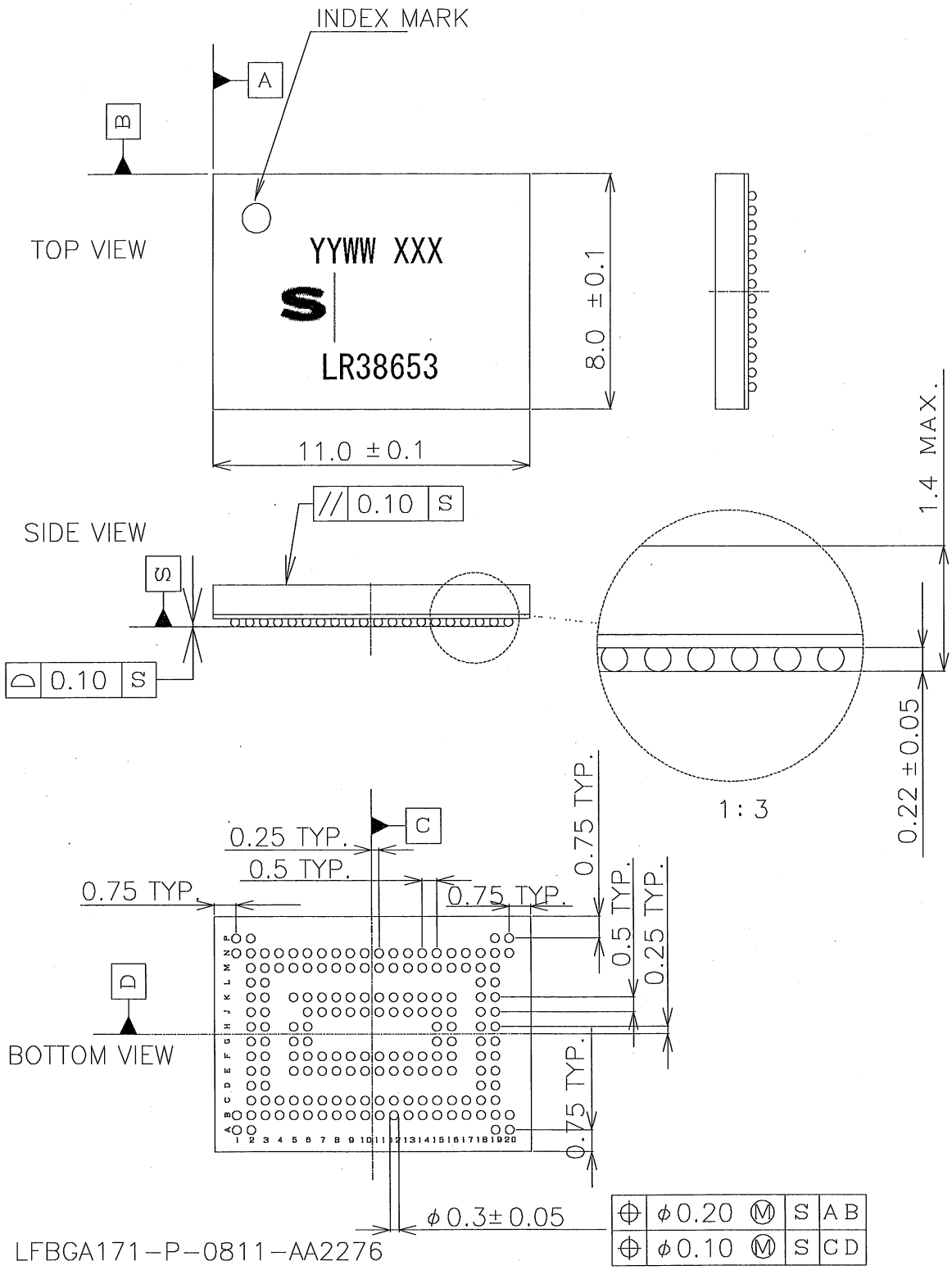
6. Markings.
6-1.Marking details. (The information on the package should be given as follows.)
(1) Product name : LR38653
(2) Company name : S
(3) Date code : (Example) YYWW XXX
YY → Denotes the production year. (Last two digits of the year.)
WW → Denotes the production week. (01・02・～・52・53)
XXX → Denotes the production ref. code (1～3 digits)

6-2.Marking layout.
The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-3Ag-0.5Cu)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note)It is those with an underline printing in a date code because of a LEAD-FREE type.



NAME	LFBGA171-P-0811			BALL TYPE
DRAWING NO.	AA2276	UNIT	mm	Sn-3Ag-0.5Cu
NOTE	Plastic body dimensions do not include burr of resin. Use of an "Under-fill": Since the external terminal is using 0.5mm max. ball pitch, this product recommends using of an "Under-fill" for maintaining the same reliability as the conventional 0.8mm ball pitch.			

*S20060223

7.Packing Specifications (Dry packing for surface mount packages.)

7-1.Packing materials.

Material name	Material specifications	Purpose
Inner carton	Cardboard (2310 devices / inner carton max.)	Packing the devices. (10 trays / inner carton)
Tray	Conductive plastic (231 devices / tray)	Securing the devices.
Upper cover tray	Conductive plastic (1 tray / inner carton)	Securing the devices.
Laminated aluminum bag	Aluminum polyethylene	Keeping the devices dry.
Desiccant	Silica gel	Keeping the devices dry.
Label	Paper	Indicates part number, quantity, and packed date.
PP band	Polypropylene (3 pcs. / inner carton)	Securing the devices.
Outer carton	Cardboard (9240 devices / outer carton max.)	Outer packing.

(Devices must be placed on the tray in the same direction.)

7-2.Outline dimension of tray.

Refer to the attached drawing.

7-3.Outline dimension of carton.

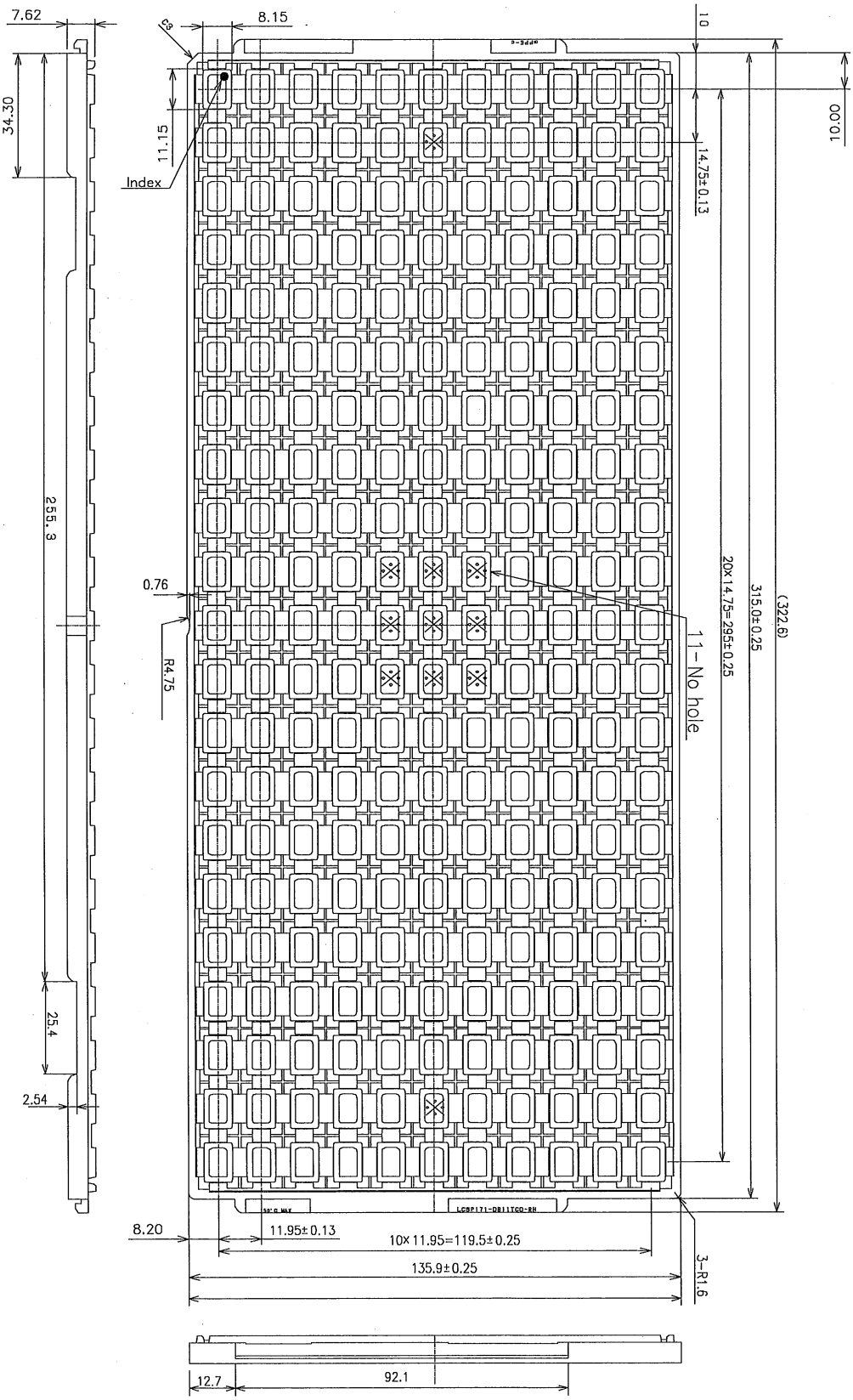
Refer to the attached drawing.

8. Precautions for use.

(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The trays have undergone either conductive or anti-ESD treatment.
If another tray is used, make sure it has also undergone conductive or anti-ESD treatment.

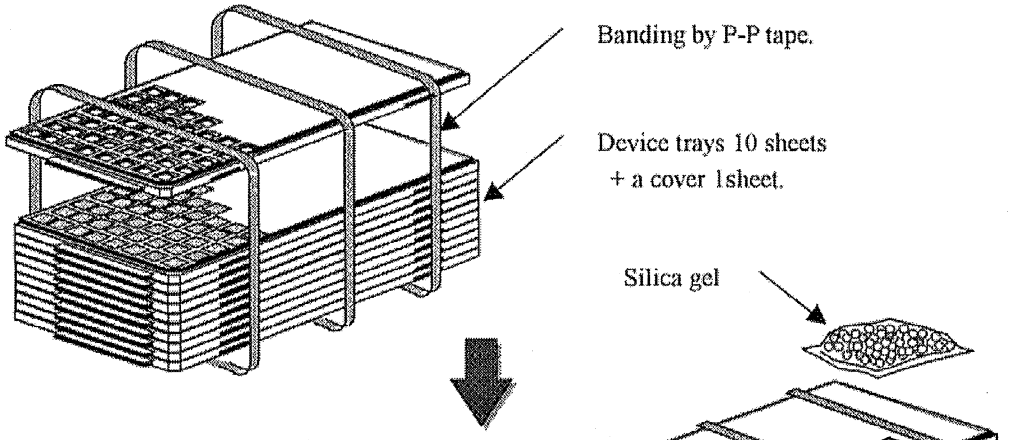
(3) The devices should be mounted within one year of the date of delivery.



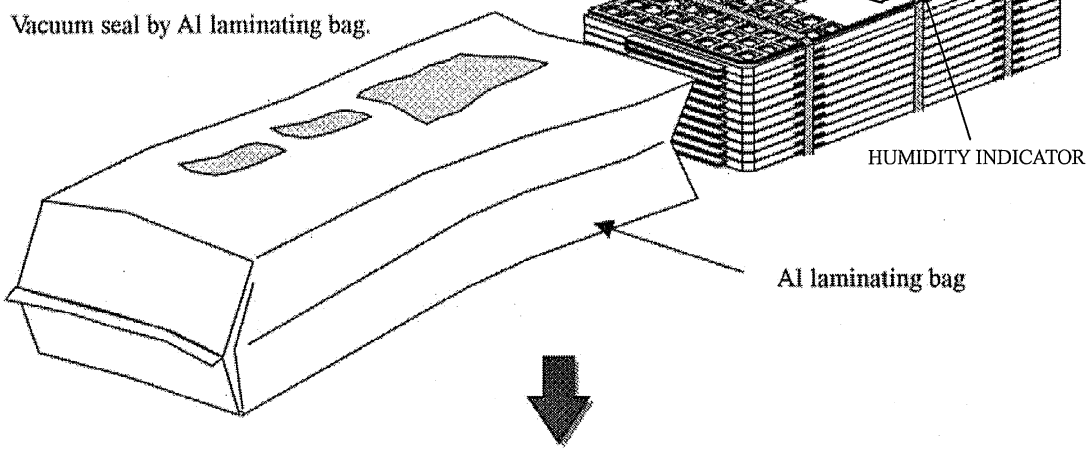
名称 NAME	LCSP171-0811TCO-RH	備考 NOTE
DRAWING NO.	CV922	単位 UNIT mm

*S20060223

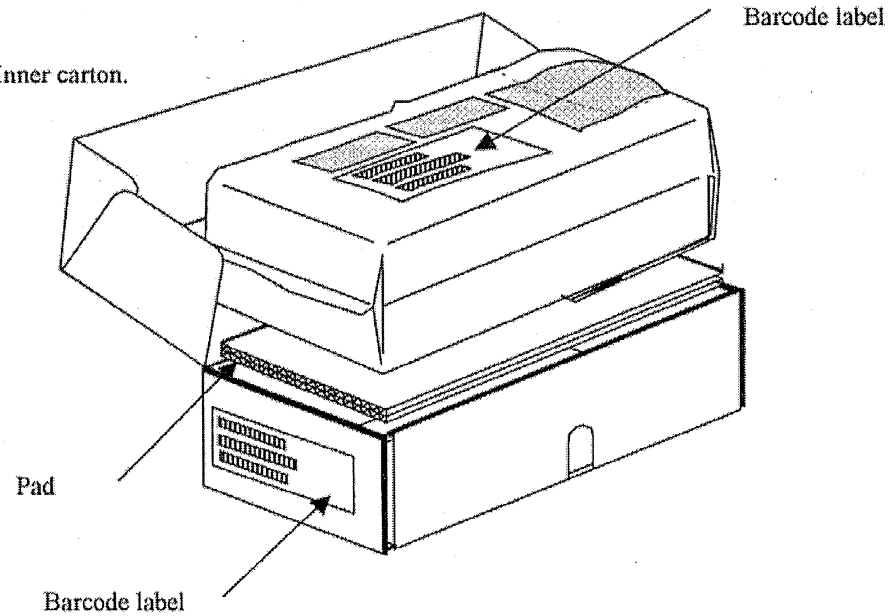
(1) Banding device tray together.



(2) Vacuum seal by Al laminating bag.

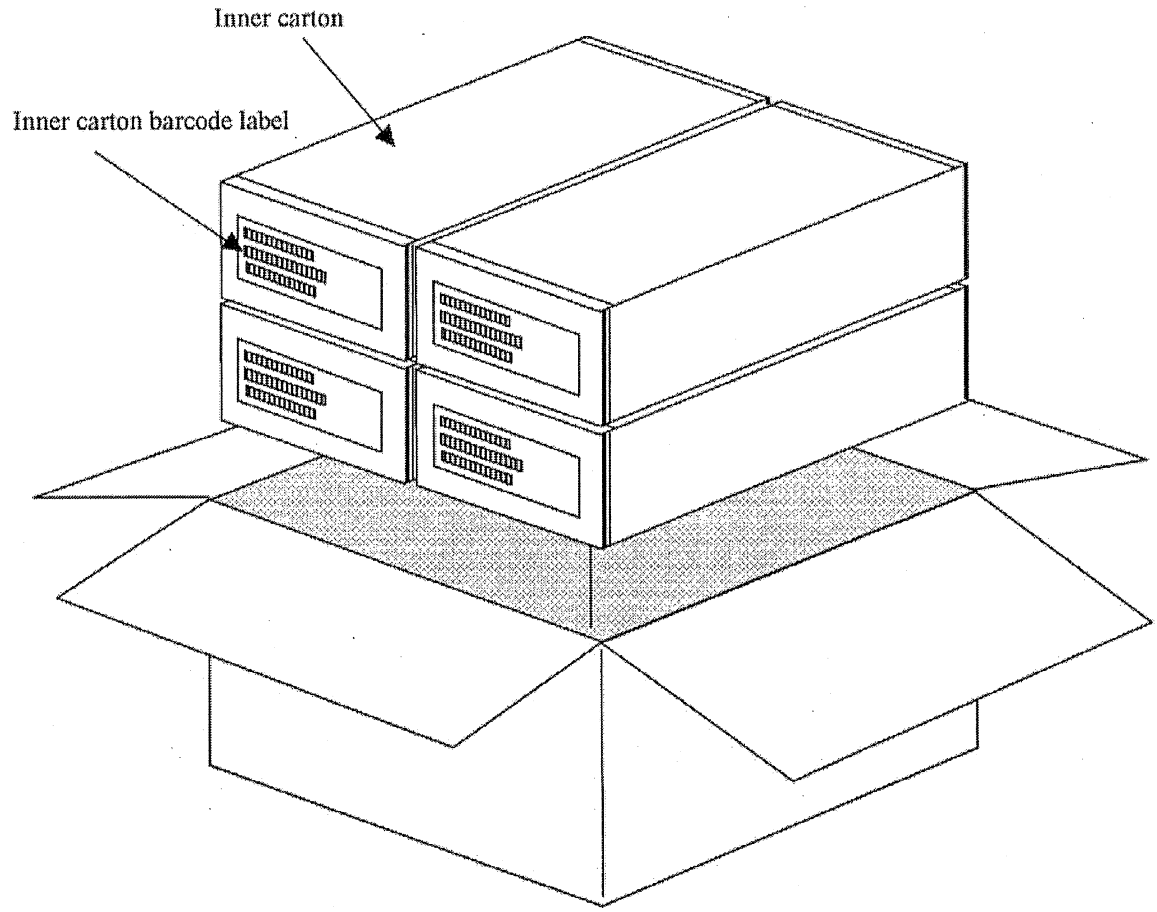


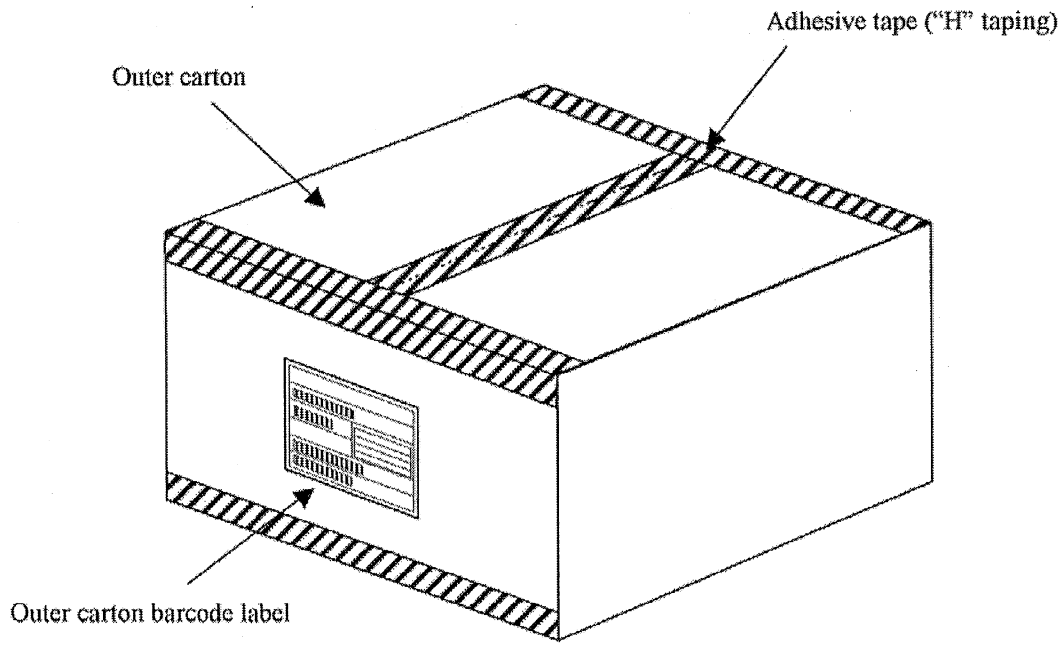
(3) Packing by Inner carton.



NAME	Packing specifications		
DRAWING NO.	BJ433c	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.





L × W× H

Inner carton - Outer dimensions : 360×150×95

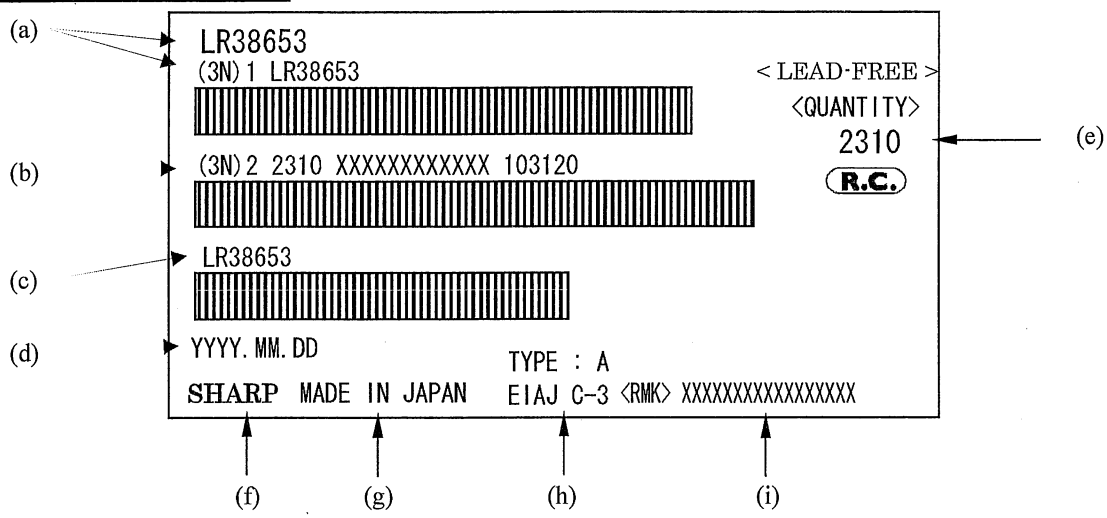
Outer carton - Outer dimensions : 390×335×230

NAME	Packing specifications		
DRAWING NO.	BJ433d	UNIT	mm

NOTE There is a possibility different from this specification when the number of shipments is fractions.

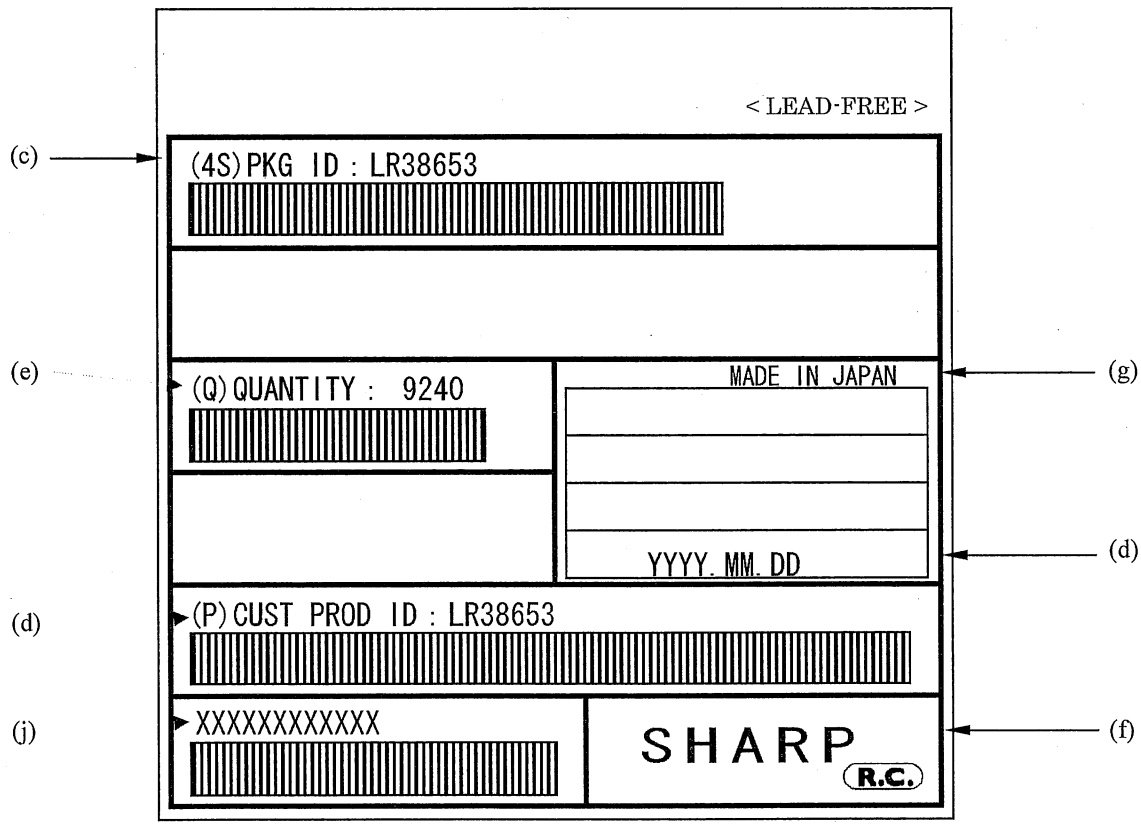
(Note) The << LEAD-FREE >> display shows a lead-free article.
"R.C." means "RoHS Compliant".

Inner carton label



Outer carton label

(Former) EIAJ B Standard conforming



(a) Product name
(b) Quantity PD lot Company code
(c) Part No. (SHARP)
(d) Packed date
(e) Quantity
(f) "SHARP" Logo
(g) The country of origin(It displays, when the country of origin is Japan.)
(h) Type name (Conformity standard)
(i) Assembly management No.
(j) Shipment lot