

# LR38666Y

## One-chip System LSI for Digital Still Cameras

### DESCRIPTION

The LR38666Y is a CMOS digital signal processor for color digital still camera systems of 1 310 k/ 2 140 k/ 3 300 k/3 370 k/4 200 k-pixel CCDs with primary color mosaic filters.

### FEATURES

- ARM7TDMI is used as the CPU core
- CCD signal processor modules
  - Supported image size : 1 310 k/ 2 140 k/3 300 k/ 3 370 k/4 200 k pixels
  - R, G and B primary color mosaic filters : Bayer matrix, 10 bits per color
  - Built-in auto focus, auto exposure and auto white balance functions
  - Built-in digital clamp and gamma correction functions
- Video encoder module
  - Composite analog signal output mode : [www.DataSheet4U.com](http://www.DataSheet4U.com)  
Switchable between NTSC and PAL
  - Built-in OSD function
- JPEG encoding/decoding module :  
Built-in circuits for encoding and decoding
  - Encoding rate : Max. 66 ms per frame (for 1/10-compression in VGA mode)
  - Decoding rate : Max. 66 ms per frame (for decompression in VGA mode)

(Assuming that SDRAM is used and the internal bus is occupied by the JPEG module)

- SDRAM/flash memory controller module
- Synchronous/asynchronous SIO
- USB 1.0 is supported
- General purpose I/O ports
- Built-in audio I/F
- Built-in resizing function
- Built-in CompactFlash I/F
- Built-in SmartMedia I/F

- Power supplies
  - +2.5 V for digital/analog circuits
  - +3.3 V for digital circuits
- Package : 240-ball CSP (T-TFBGA240-1414)

PIN CONNECTIONS

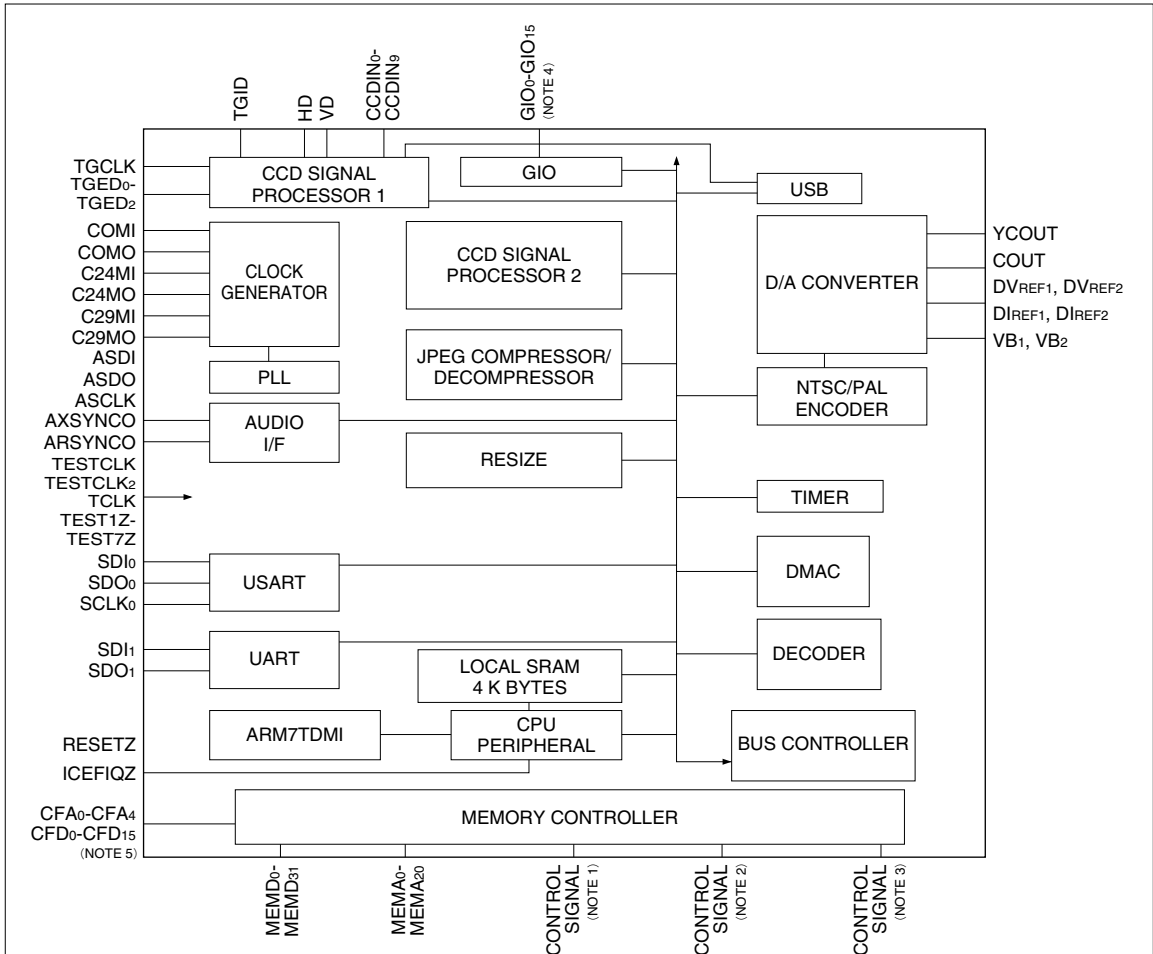
240-BALL CSP

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	○ Index mark															
A	○	237	236	232	228	227	221	215	209	204	198	193	188	186	183	○
	NC	PLVDD	PLGND	TESTCLK2	DVDD2	SDI0	C24MI	ASCLK	TGED1	CCDIN6	COMI	DVDD2	TGID	DIREF2	DAVDD	NC
B	3	1	238	234	230	224	218	212	206	201	195	190	185	182	181	177
	MEMCKE3	MEMCKE1	PLGND	DVDD	C29MI	DVDD	DVDD	ASDO	CCDIN8	DVDD	CCDIN1	TGCLK	DVREF2	DAGND	YCOUT	VB1
C	6	2	239	235	231	225	219	213	207	200	194	189	184	178	179	176
	MEMCS2Z	MEMCKE2	DGND	PLVDD	SDO0	SCLK0	SDI1	TCLK	CCDIN9	CCDIN3	CCDIN0	DVDD	COUT	DIREF1	DVREF1	DGND
D	8	5	4	233	229	226	220	211	208	202	192	187	173	175	174	172
	MEMCS3Z	MEMCS1Z	MEMCS0Z	ICEFIOZ	C29MO	DGND	DGND	ASDI	TGED0	CCDIN4	VD	VB2	GIO14	RESETZ	GIO15	GIO13
E	13	9	7	10	11	223	217	210	205	199	196	191	169	171	170	168
	DVDD2	DGND	DVDD	MEMD0	MEMD1	SDO1	ARSYNCO	TGED2	CCDIN7	DGND	CCDIN2	HD	GIO11	GIO12	TESTCLK	GIO10
F	19	14	15	12	16	222	216	214	203	197	162	163	167	164	165	166
	DVDD	MEMD3	DGND	MEMD2	MEMD4	C24MO	AXSYNCO	DGND	CCDIN5	COMO	GIO5	GIO6	GIO9	DGND	GIO7	GIO8
G	25	20	21	18	17	22					156	157	161	159	158	160
	MEMD11	MEMD7	DGND	MEMD6	MEMD5	MEMD8					GIO1	GIO2	GIO4	GIO3	DVDD2	DVDD
H	29	27	26	24	23	28					150	151	155	153	152	154
	DVDD	MEMD12	DGND	MEMD10	MEMD9	MEMD13					CFA1	CFA2	GIO0	DGND	CFA3	CFA4
J	35	32	33	31	30	34					143	145	148	147	146	149
	TEST2Z	TEST1Z	DGND	MEMD15	MEMD14	MEMD16					CFD11	CFD13	CFD15	CFD14	DVDD	CFA0
K	41	38	39	37	40	36					137	139	142	141	140	144
	MEMD20	MEMD18	MEMD19	MEMD17	DGND	TST3Z					CFD8	DVDD2	TEST2Z	DGND	CFD10	CFD12
L	45	44	46	48	43	42	82	89	94	96	102	133	136	134	135	138
	MEMD21	DVDD	MEMD22	DGND	TEST5Z	TEST4Z	TEST6Z	DGND	DVDD2	MEMA16	MEMA20	DGND	CFD7	CFD5	CFD6	CFD9
M	47	50	51	49	71	76	77	83	90	100	107	131	130	127	129	132
	MEMD23	DVDD2	MEMD25	MEMD24	MEMA0	MEMA3	MEMA4	MEMA8	MEMA12	DGND	FL_EXWWEZ	CFD3	CFD2	CFD0	DVDD	CFD4
N	52	54	55	53	70	72	79	85	91	97	103	109	113	124	125	128
	MEMD26	DGND	MEMD28	MEMD27	MEMWEZ	MEMA1	DGND	DGND	MEMA13	MEMA17	FLCE0Z	FLRPOZ	EXCS1Z	CFRST	CFCE1Z	CFD1
P	56	59	58	64	67	73	80	87	93	99	106	111	115	118	122	126
	DVDD	MEMD31	MEMD30	MEMRASZ	DGND	DGND	MEMA6	MEMA10	DGND	MEMA18	DGND	EXCS0Z	EXDACK1Z	CFCD1Z	CFREGZ	CFCE2Z
R	57	61	62	65	69	75	81	86	92	98	104	110	114	119	121	123
	MEMD29	DGND	MEMLDQM	MEMCASZ	DVDD2	DVDD	MEMA7	DVDD	MEMA14	DVDD	FLCE1Z	FLRP1Z	EXDACK0Z	CFCD2Z	CFWAITZ	DGND
T	○	63	66	68	74	78	84	88	95	101	105	108	112	116	117	○
	NC	MEMUDQM	DVDD	MEMCLK	MEMA2	MEMA5	MEMA9	MEMA11	MEMA15	MEMA19	FL_EXOEZ	FLWPZ	DVDD	EXINTZ	CFRDBY	NC

(T-TFBGA240-1414)

## BLOCK DIAGRAM



## NOTES :

- Control signal for SDRAM  
MEMCLK, MEMLDQM, MEMUDQM, MEMWEZ, MEMCASZ, MEMRASZ, MEMCKE1, MEMCS0Z-MEMCS3Z  
Control signal for SDRAM or general purpose I/O.  
MEMCKE2 = GIO16, MEMCKE3 = GIO17 (set by register)
- Control signal for flash memory and external device.  
FLCE0Z, FL\_EXOEZ, FL\_EXWEZ, FLWPZ, FLRP0Z, EXCS0Z, CFREGZ, CFRST, CFCE1Z to CFCE2Z  
Control signal for flash memory and external device or general purpose I/O  
FLCE1Z = GIO18, FLRP1Z = GIO19, EXCS1Z = GIO20 (set by register)
- Input signal from external device  
EXDACK0Z, EXINTZ, CFWAITZ, CFRDBY  
Input signal from external device or general purpose I/O.  
EXDACK1Z = GIO21, CFCD1Z = GIO22, CFCD2Z = GIO23 (set by register)
- General purpose I/O or PWM.  
GIO0 to GIO2 = CCDGEO0 to CCDGEO2, GIO9 = TX\_VPO, GIO10 = TX\_VMO, GIO11 = TX\_OE\_N, GIO12 = SUSPEND\_N, GIO13 = RX\_VPI, GIO14 = RX\_VMI, GIO15 = RX\_DATA (set by register)
- Data I/O for CompactFlash or general purpose I/O.  
CFD8 = GIO24, CFD9 = GIO25, CFD10 = GIO26, CFD11 = GIO27, CFD12 = GIO28, CFD13 = GIO29, CFD14 = GIO30, CFD15 = GIO31 (set by register)

## PIN DESCRIPTION

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
1	2B	MEMCKE1	IO8	SDRAM clock enable, Block 1
2	2C	MEMCKE2	IO8	SDRAM clock enable, Block 2/GIO16
3	1B	MEMCKE3	IO8	SDRAM clock enable, Block 3/GIO17
4	3D	MEMCS0Z	IO8	SDRAM chip select, Block 0
5	2D	MEMCS1Z	IO8	SDRAM chip select, Block 1
6	1C	MEMCS2Z	IO8	16-bit data mode : SDRAM chip select, Block 2 32-bit data mode : Control MEMD <sub>15</sub> to MEMD <sub>8</sub> of SDRAM
7	3E	DV <sub>DD</sub>	–	Power supply (+3.3 V)
8	1D	MEMCS3Z	IO8	16-bit data mode : SDRAM chip select, Block 3 32-bit data mode : Control MEMD <sub>7</sub> to MEMD <sub>0</sub> of SDRAM
9	2E	DGND	–	Ground
10	4E	MEMD <sub>0</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
11	5E	MEMD <sub>1</sub>	IO12U	
12	4F	MEMD <sub>2</sub>	IO12U	
13	1E	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
14	2F	MEMD <sub>3</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
15	3F	DGND	–	Ground
16	5F	MEMD <sub>4</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
17	5G	MEMD <sub>5</sub>	IO12U	
18	4G	MEMD <sub>6</sub>	IO12U	
19	1F	DV <sub>DD</sub>	–	Power supply (+3.3 V)
20	2G	MEMD <sub>7</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
21	3G	DGND	–	Ground
22	6G	MEMD <sub>8</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
23	5H	MEMD <sub>9</sub>	IO12U	
24	4H	MEMD <sub>10</sub>	IO12U	
25	1G	MEMD <sub>11</sub>	IO12U	
26	3H	DGND	–	Ground
27	2H	MEMD <sub>12</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
28	6H	MEMD <sub>13</sub>	IO12U	
29	1H	DV <sub>DD</sub>	–	Power supply (+3.3 V)
30	5J	MEMD <sub>14</sub>	IO12U	Data I/O for SDRAM/flash memory/external device
31	4J	MEMD <sub>15</sub>	IO12U	
32	2J	TEST1Z	IU	Test (Must be open.)
33	3J	DGND	–	Ground
34	6J	MEMD <sub>16</sub>	IO12U	Data I/O for SDRAM/external device/GIO16
35	1J	TEST2Z	IU	Test (Must be open.)
36	6K	TEST3Z	IU	
37	4K	MEMD <sub>17</sub>	IO12U	Data I/O for SDRAM/external device/GIO17
38	2K	MEMD <sub>18</sub>	IO12U	Data I/O for SDRAM/external device/GIO18
39	3K	MEMD <sub>19</sub>	IO12U	Data I/O for SDRAM/external device/GIO19

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
40	5K	DGND	–	Ground
41	1K	MEMD <sub>20</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>20</sub>
42	6L	TEST4Z	IU	Test (Must be open.)
43	5L	TEST5Z	IU	
44	2L	DV <sub>DD</sub>	–	Power supply (+3.3 V)
45	1L	MEMD <sub>21</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>21</sub>
46	3L	MEMD <sub>22</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>22</sub>
47	1M	MEMD <sub>23</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>23</sub>
48	4L	DGND	–	Ground
49	4M	MEMD <sub>24</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>24</sub>
50	2M	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
51	3M	MEMD <sub>25</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>25</sub>
52	1N	MEMD <sub>26</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>26</sub>
53	4N	MEMD <sub>27</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>27</sub>
54	2N	DGND	–	Ground
55	3N	MEMD <sub>28</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>28</sub>
56	1P	DV <sub>DD</sub>	–	Power supply (+3.3 V)
57	1R	MEMD <sub>29</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>29</sub>
58	3P	MEMD <sub>30</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>30</sub>
59	2P	MEMD <sub>31</sub>	IO12U	Data I/O for SDRAM/external device/GIO <sub>31</sub>
60	–	NC	–	Must be open.
61	2R	DGND	–	Ground
62	3R	MEMLDQM	O12	16-bit data mode : Control MEMD <sub>7</sub> -MEMD <sub>0</sub> of SDRAM 32-bit data mode : Control MEMD <sub>23</sub> -MEMD <sub>16</sub> of SDRAM
63	2T	MEMUDQM	O12	16-bit data mode : Control MEMD <sub>15</sub> -MEMD <sub>8</sub> of SDRAM 32-bit data mode : Control MEMD <sub>31</sub> -MEMD <sub>24</sub> of SDRAM
64	4P	MEMRASZ	O12	SDRAM row address strobe
65	4R	MEMCASZ	O12	SDRAM column address strobe
66	3T	DV <sub>DD</sub>	–	Power supply (+3.3 V)
67	5P	DGND	–	Ground
68	4T	MEMCLK	IO12	SDRAM clock output (49.0908 MHz : double of C24MI input)
69	5R	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
70	5N	MEMWEZ	O12	SDRAM write enable
71	5M	MEMA <sub>0</sub>	O12	Address for SDRAM/flash memory/external device
72	6N	MEMA <sub>1</sub>	O12	
73	6P	DGND	–	Ground
74	5T	MEMA <sub>2</sub>	O12	Address for SDRAM/flash memory/external device
75	6R	DV <sub>DD</sub>	–	Power supply (+3.3 V)
76	6M	MEMA <sub>3</sub>	O12	Address for SDRAM/flash memory/external device
77	7M	MEMA <sub>4</sub>	O12	Address for SDRAM/flash memory/external device
78	6T	MEMA <sub>5</sub>	O12	Address for SDRAM/flash memory/external device
79	7N	DGND	–	Ground

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
80	7P	MEMA <sub>6</sub>	O12	Address for SDRAM/flash memory/external device
81	7R	MEMA <sub>7</sub>	O12	Address for SDRAM/flash memory/external device
82	7L	TEST6Z	IU	Test (Must be open.)
83	8M	MEMA <sub>8</sub>	O12	Address for SDRAM/flash memory/external device
84	7T	MEMA <sub>9</sub>	O12	Address for SDRAM/flash memory/external device
85	8N	DGND	–	Ground
86	8R	DV <sub>DD</sub>	–	Power supply (+3.3 V)
87	8P	MEMA <sub>10</sub>	O12	Address for SDRAM/flash memory/external device
88	8T	MEMA <sub>11</sub>	O12	Address for SDRAM/flash memory/external device
89	8L	DGND	–	Ground
90	9M	MEMA <sub>12</sub>	O12	Address for SDRAM/flash memory/external device
91	9N	MEMA <sub>13</sub>	O12	Address for SDRAM/flash memory/external device
92	9R	MEMA <sub>14</sub>	O12	Address for SDRAM/flash memory/external device
93	9P	DGND	–	Ground
94	9L	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
95	9T	MEMA <sub>15</sub>	O12	Address for flash memory/external device/CompactFlash (CFA5)
96	10L	MEMA <sub>16</sub>	O12	Address for flash memory/external device/CompactFlash (CFA6)
97	10N	MEMA <sub>17</sub>	O12	Address for flash memory/external device/CompactFlash (CFA7)
98	10R	DV <sub>DD</sub>	–	Power supply (+3.3 V)
99	10P	MEMA <sub>18</sub>	O12	Address for flash memory/external device/CompactFlash (CFA8)
100	10M	DGND	–	Ground
101	10T	MEMA <sub>19</sub>	O12	Address for flash memory/external device/CompactFlash (CFA9)
102	11L	MEMA <sub>20</sub>	O12	Address for flash memory/external device/CompactFlash (CFA10)
103	11N	FLCE0Z	O8	Chip enable for flash memory, Block 0
104	11R	FLCE1Z	IO8	Chip enable for flash memory, Block 1/GIO <sub>18</sub>
105	11T	FL_EXOEZ	O8	Output enable for flash memory/external device/CompactFlash
106	11P	DGND	–	Ground
107	11M	FL_EXWEZ	O8	Write enable for flash memory/external device/CompactFlash
108	12T	FLWPZ	O8	Write protect for flash memory
109	12N	FLRP0Z	O8	Reset/deep power down for flash memory, Block 0
110	12R	FLRP1Z	IO8	Reset/deep power down for flash memory, Block 1/GIO <sub>19</sub>
111	12P	EXCS0Z	O8	Chip select 0 for external device
112	13T	DV <sub>DD</sub>	–	Power supply (+3.3 V)
113	13N	EXCS1Z	IO8	Chip select 1 for external device/GIO <sub>20</sub>
114	13R	EXDACK0Z	IU	Data acknowledge 0 for external device
115	13P	EXDACK1Z	IO8U	Data acknowledge 1 for external device/GIO <sub>21</sub>
116	14T	EXINTZ	IU	External device interrupt
117	15T	CFRDBY	IU	CompactFlash/SmartMedia READY/BUSY
118	14P	CFCD1Z	IO8U	CompactFlash/SmartMedia card detect signal 1/GIO <sub>22</sub>
119	14R	CFCD2Z	IO8U	CompactFlash card detect signal 2/SmartMedia write protect detect/GIO <sub>23</sub>
120	–	NC	–	Must be open.

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
121	15R	CFWAITZ	IU	CompactFlash –WAIT signal
122	15P	CFREGZ	IO8	CompactFlash –REG signal
123	16R	DGND	–	Ground
124	14N	CFRST	IO8	CompactFlash reset signal (RESET)/SmartMedia chip enable (–CE)
125	15N	CFCE1Z	IO8	Card enable 1 for CompactFlash (–CE1)
126	16P	CFCE2Z	IO8	Card enable 2 for CompactFlash (–CE2)
127	14M	CFD <sub>0</sub>	IO8U	Data I/O for CompactFlash/SmartMedia
128	16N	CFD <sub>1</sub>	IO8U	
129	15M	DVDD	–	Power supply (+3.3 V)
130	13M	CFD <sub>2</sub>	IO8U	Data I/O for CompactFlash/SmartMedia
131	12M	CFD <sub>3</sub>	IO8U	
132	16M	CFD <sub>4</sub>	IO8U	
133	12L	DGND	–	
134	14L	CFD <sub>5</sub>	IO8U	Data I/O for CompactFlash/SmartMedia
135	15L	CFD <sub>6</sub>	IO8U	
136	13L	CFD <sub>7</sub>	IO8U	
137	11K	CFD <sub>8</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>24</sub>
138	16L	CFD <sub>9</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>25</sub>
139	12K	DVDD <sub>2</sub>	–	Internal power supply (+2.5 V)
140	15K	CFD <sub>10</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>26</sub>
141	14K	DGND	–	Ground
142	13K	TEST7Z	IU	Test (Must be open.)
143	11J	CFD <sub>11</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>27</sub>
144	16K	CFD <sub>12</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>28</sub>
145	12J	CFD <sub>13</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>29</sub>
146	15J	DVDD	–	Power supply (+3.3 V)
147	14J	CFD <sub>14</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>30</sub>
148	13J	CFD <sub>15</sub>	IO8U	Data I/O for CompactFlash/GIO <sub>31</sub>
149	16J	CFA <sub>0</sub>	IO8	Address for CompactFlash/read enable for SmartMedia (–RE)
150	11H	CFA <sub>1</sub>	IO8	Address for CompactFlash/write enable for SmartMedia (–WE)
151	12H	CFA <sub>2</sub>	IO8	Address for CompactFlash/write protect for SmartMedia (–WP)
152	15H	CFA <sub>3</sub>	IO8	Address for CompactFlash/address latch enable for SmartMedia (ALE)
153	14H	DGND	–	Ground
154	16H	CFA <sub>4</sub>	IO8	Address for CompactFlash/command latch enable for SmartMedia (CLE)
155	13H	GIO <sub>0</sub>	IO8	General purpose I/O (+3.3 V)/PWM/CCD general purpose output
156	11G	GIO <sub>1</sub>	IO8	
157	12G	GIO <sub>2</sub>	IO8	
158	15G	DVDD <sub>2</sub>	–	Internal power supply (+2.5 V)

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
159	14G	GIO3	IO8	General purpose I/O (+3.3 V)/PWM
160	16G	DVDD	–	Power supply (+3.3 V)
161	13G	GIO4	IO8	General purpose I/O (+3.3 V)/PWM
162	11F	GIO5	IO8	
163	12F	GIO6	IO8	
164	14F	DGND	–	Ground
165	15F	GIO7	IO8	General purpose I/O (+3.3 V)/PWM
166	16F	GIO8	IO8	
167	13F	GIO9	IO8	General purpose I/O (+3.3 V)/PWM/TX_VPO output for USB (send data +)
168	16E	GIO10	IO8	General purpose I/O (+3.3 V)/PWM/TX_VMO output for USB (send data –)
169	13E	GIO11	IO8	General purpose I/O (+3.3 V)/PWM/TX_OE_N output for USB (send enable)
170	15E	TESTCLK	I	Ground
171	14E	GIO12	IO8	General purpose I/O (+3.3 V)/PWM/SUSPEND_N output for USB (suspend request)
172	16D	GIO13	IO8	General purpose I/O (+3.3 V)/PWM/RX_VPI input from USB (receive data +)
173	13D	GIO14	IO8	General purpose I/O (+3.3 V)/PWM/RX_VMI input from USB (receive data –)
174	15D	GIO15	IO8	General purpose I/O (+3.3 V)/PWM/RX_DATA input from USB (receive enable)
175	14D	RESETZ	IS	Reset
176	16C	DGND	–	Ground
177	16B	VB1	–	Biased voltage output 1
178	14C	DIREF1	DAIREF	DAC reference current output 1
179	15C	DVREF1	DAVREF	DAC full scaled reference voltage input 1
180	–	NC	–	Must be open.
181	15B	YCOUT	DAI	NTSC/PAL composite/luminance analog output (1 Vp-p : must be connected to 75 Ω.)
182	14B	DAGND	–	Ground for DAC
183	15A	DAVDD	–	Power supply for DAC (+2.5 V)
184	13C	COUT	DAI	NTSC/PAL composite/chrominance analog output (1 Vp-p : must be connected to 75 Ω)
185	13B	DVREF2	DAVREF	DAC full-scale reference voltage input 2
186	14A	DIREF2	DAIREF	DAC reference current output 2
187	12D	VB2	–	Bias voltage output 2
188	13A	TGID	I	Identification pulse for color line of CCD signal from TG (High at R-line)
189	12C	DVDD	–	Power supply (+3.3 V)



PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
190	12B	TGCLK	I	Pixel clock input from TG
191	12E	HD	IO8	Horizontal synchronization pulse for CCD
192	11D	VD	IO8	Vertical synchronization pulse for CCD
193	12A	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
194	11C	CCDIN <sub>0</sub>	I	RGB input from CCD
195	11B	CCDIN <sub>1</sub>	I	
196	11E	CCDIN <sub>2</sub>	I	
197	10F	COMO	OSC	24 MHz crystal oscillator output
198	11A	COMI	IA	24 MHz crystal oscillator input (for communication)
199	10E	DGND	–	Ground
200	10C	CCDIN <sub>3</sub>	I	RGB input from CCD
201	10B	DV <sub>DD</sub>	–	Power supply (+3.3 V)
202	10D	CCDIN <sub>4</sub>	I	RGB input from CCD
203	9F	CCDIN <sub>5</sub>	I	
204	10A	CCDIN <sub>6</sub>	I	
205	9E	CCDIN <sub>7</sub>	I	
206	9B	CCDIN <sub>8</sub>	I	
207	9C	CCDIN <sub>9</sub>	I	
208	9D	TGED <sub>0</sub>	IO8	Serial signal output for setting register of TG
209	9A	TGED <sub>1</sub>	IO8	
210	8E	TGED <sub>2</sub>	O8	
211	8D	ASDI	IU	Input data for audio serial I/F
212	8B	ASDO	O8	Output data for audio serial I/F
213	8C	TCLK	I	Master clock input for audio serial I/F
214	8F	DGND	–	Ground
215	8A	ASCLK	O8	Shift clock for audio serial I/F
216	7F	AXSYNCO	O8	Transmit synchronous signal for audio serial I/F
217	7E	ARSYNCO	O8	Receive synchronous signal for audio serial I/F
218	7B	DV <sub>DD</sub>	–	Power supply (+3.3 V)
219	7C	SDI <sub>1</sub>	I	Input data for asynchronous serial I/F
220	7D	DGND	–	Ground
221	7A	C24MI	IA	24.5454 MHz crystal oscillator input (system clock)
222	6F	C24MO	OSC	24.5454 MHz crystal oscillator output
223	6E	SDO <sub>1</sub>	O8	Output data for asynchronous serial I/F
224	6B	DV <sub>DD</sub>	–	Power supply (+3.3 V)
225	6C	SCLK <sub>0</sub>	IO8U	Clock for synchronous serial I/F
226	6D	DGND	–	Ground
227	6A	SDI <sub>0</sub>	I	Input data for synchronous serial I/F
228	5A	DV <sub>DD2</sub>	–	Internal power supply (+2.5 V)
229	5D	C29MO	OSC	29.5 MHz crystal oscillator output
230	5B	C29MI	IA	29.5 MHz crystal oscillator input (for PAL)

PIN NO.	COORDINATE	SYMBOL	IO SYMBOL	DESCRIPTION
231	5C	SDO <sub>0</sub>	O8	Output data for synchronous serial I/F
232	4A	TESTCLK <sub>2</sub>	I	Input signal for test (Must be connected to ground.)
233	4D	ICEFIQZ	IU	FIQ interrupt input for ROMICE (Must be open during normal operation.)
234	4B	DVDD	–	Power supply (+3.3 V)
235	4C	PLVDD	–	Power supply for PLL (+2.5 V)
236	3A	PLGND	–	Ground for PLL
237	2A	PLVDD	–	Power supply for PLL (+2.5 V)
238	3B	PLGND	–	Ground for PLL
239	3C	DGND	–	Ground
240	–	NC	–	Must be open.

I	: Input pin	IO12	: Input/output pin
IS	: Schmitt input pin	IO12U	: Input/output pin with pull-up resistor
IU	: Input pin with pull-up resistor	DAI	: Analog output pin
O8	: Output pin	DAVREF	: Analog input pin for DAC
O12	: Output pin	DAIREF	: Analog output pin for DAC
IO8	: Input/output pin	IA	: Input pin for oscillation
IO8U	: Input/output pin with pull-up resistor	OSC	: Output pin for oscillation

**REMARKS :**

PIN TYPE (MAX. OUTPUT CURRENT)	APPLICABLE PINS
+3.3 V I/O pin (12 mA) or output pin	MEMLDQM, MEMUDQM, MEMCLK, MEMWEZ, MEMCASZ, MEMRASZ, MEMA <sub>0</sub> to MEMA <sub>20</sub>
+3.3 V I/O pin (8 mA) or output pin	MEMCKE <sub>1</sub> to MEMCKE <sub>3</sub> , MEMCS0Z to MEMCS3Z, FLCE0Z to FLCE1Z, FL_EXOEZ, FL_EXWEZ, FLWPZ, FLRP0Z to FLRP1Z, EXCS0Z to EXCS1Z, CFREGZ, CFRST, CFCE1Z to CFCE2Z, CFA <sub>0</sub> to CFA <sub>4</sub> , GIO <sub>0</sub> to GIO <sub>15</sub> , HD, VD, TGED <sub>0</sub> to TGED <sub>2</sub> , ASDO, ASCLK, AXSYNCO, ARSYNCO, SDO <sub>1</sub> , SDO <sub>0</sub>
+3.3 V I/O pin (12 mA, 98 kΩ pull-up resistor installed)	MEMD <sub>0</sub> to MEMD <sub>31</sub>
+3.3 V I/O pin (8 mA, 98 kΩ pull-up resistor installed) or input pin	TEST1Z to TEST7Z, EXDACK0Z to EXDACK1Z, EXINTZ, CFRDBY, CFWAITZ, CFD <sub>0</sub> to CFD <sub>15</sub> , ASDI, SCLK <sub>0</sub> , ICEFIQZ

**NOTES :**

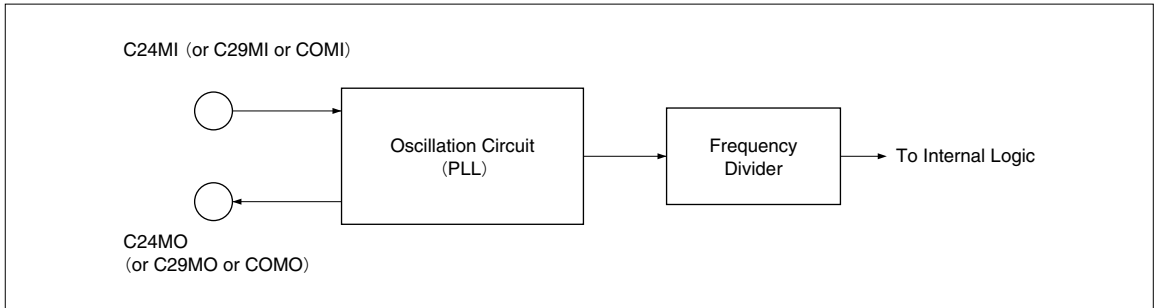
- When an I/O pin is set to "input", take care not to let the pin to have a floating address.
- Keep test pins TEST1Z to TEST7Z normally open.
- I/O pins MEMCKE<sub>2</sub>, MEMCKE<sub>3</sub>, FLCE1Z, FLRP1Z, EXCS1Z and MEMCLK are set to "output" when reset (RESETZ input is Low level), while other I/O pins are "input".

## FUNCTIONAL DESCRIPTION

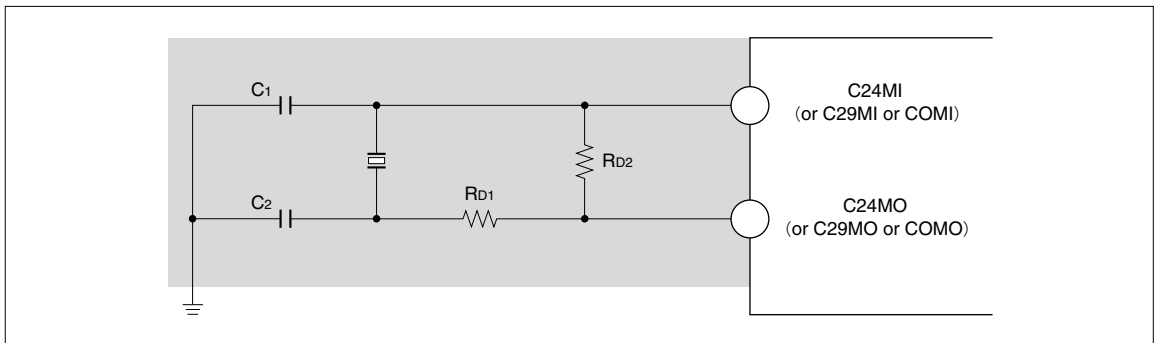
passes through the doubled frequency of the quartz crystal connected to I/O pins, and provides it to the internal logic circuits as shown in **Fig.1** and **Fig.2**.

### Oscillation Circuit

The PLL included in the LR38666Y divides or



**Fig. 1 Block Diagram of Oscillation Circuit**



**Fig. 2 Clock Input to Oscillation Circuit**

### Connection of Quartz Crystal (TA = 0 to +70°C) : Example of Oscillation under Fundamental Frequencies

APPLICABLE PINS	FUNDAMENTAL FREQUENCY [MHz]	RECOMMENDED COEFFICIENT			
		C1 [pF]	C2 [pF]	RD1 [Ω]	RD2 [Ω]
C24MI, C24MO	24.5454	10	10	220	1 M
C29MI, C29MO	29.5000	10	10	220	1 M
COMI, COMO	24.0000	10	10	220	1 M

#### NOTES :

1. The oscillation circuit should be located as close to C24MI, C24MO (C29MI, C29MO, COMI, COMO) as possible.
2. Do not install other signal lines in the shaded area.
3. Perform due evaluation on the match between the LR38666Y and the quartz crystal.

## Clock

The clock supplied to C24MI is doubled in frequency by an internal PLL and then is used as the main system clock. This clock is also used by the NTSC/PAL module in NTSC mode.

The clock supplied to C29MI is doubled in frequency by an internal PLL and then is used by the NTSC/PAL module in PAL mode only. The PAL mode allows clock oscillation. If the PAL mode is not used, fix the input level to High or Low. Note that, in NTSC mode, the accuracy of burst signals (deflection from the specified frequency) for video output depends on the accuracy of the clock supplied to C24MI. In PAL mode, the accuracy of burst signals (deflection from the specified frequency) for video output depends on the accuracy of the clock supplied to C29MI.

The clock supplied to COMI is doubled in frequency by an internal PLL and then is used by the UART, USART, USB and AUDIOIF modules. Only 24 MHz frequency can be used.

Note that the accuracy of the clock supplied to COMI influences the pulse width of the I/O signals. Supply the clock (synchronized with CCD data) to

TGCLK. Use as low a noise level signal as possible. Note that accuracy of the clock supplied to TCLK influences the accuracy of the clock of AUDIOIF. If TCLK is not used, fix the input level to High or Low.

## Power Supply Pins

Connect low noise power lines to the PLL power supply pin (PLVDD), the PLL ground pin (PLGND), the DA converter power supply pin (DAVDD) and the DA converter ground pin (DAGND).

Note that PLVDD and DAVDD are connected to DVDD2, and PLGND and DAGND are connected to DGND inside the LR38666Y.

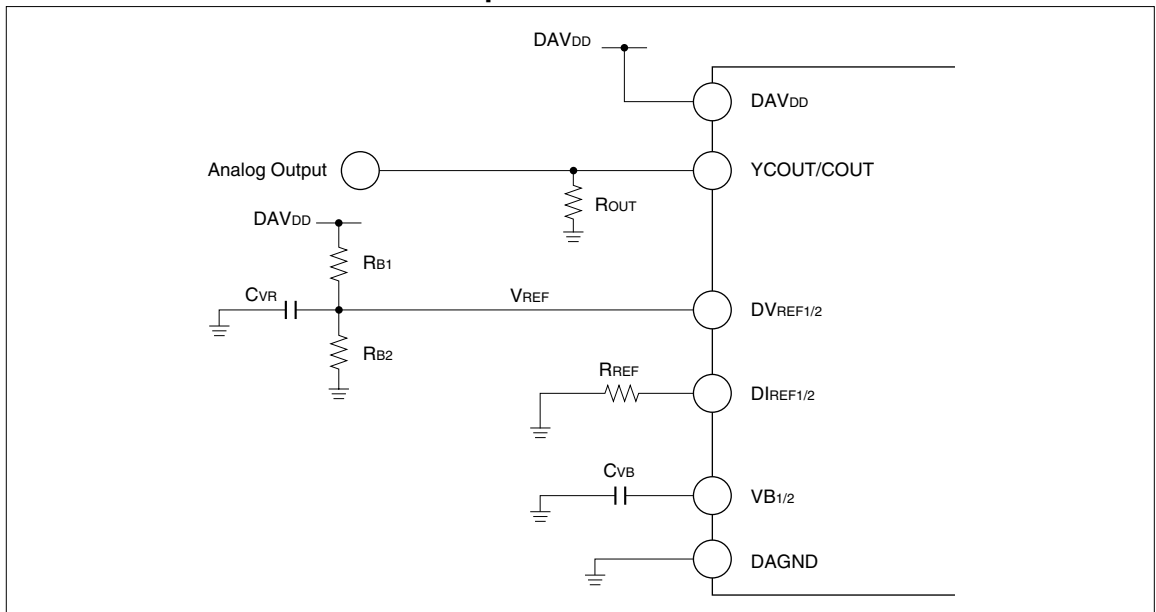
## Power ON/OFF Sequence

Two power supplies are used with the LR38666Y. One (DVDD) is used for I/O buffer and the other (DVDD2) is used for the core logic circuits.

Power ON : Be sure to turn ON the internal power supply of DVDD2 first.

Power OFF : Be sure to turn OFF the I/O buffer of DVDD first.

## Recommended DAC Circuit (Example)



**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	RATING	UNIT
I/O power supply voltage	DVDD	-0.3 to +4.3	V
Internal power supply voltage	DVDD2	-0.3 to +3.3	V
Input voltage	VI	-0.3 to DVDD + 0.3	V
Output voltage	VO	-0.3 to DVDD + 0.3	V
Storage temperature	TSTG	-55 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply voltage	DVDD	I/O digital power supply	3.0	3.3	3.6	V
	DVDD2	Internal digital power supply	2.25	2.5	2.75	V
	DAVDD	Analog power supply	2.25	2.5	2.75	V
Operating temperature	TOPR		0	+25	+70	°C
Operating frequency	fOPR	Maximum operating frequency		49.0908		MHz

## ELECTRICAL CHARACTERISTICS

## DC Characteristics

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V <sub>IL</sub>				0.2 DV <sub>DD</sub>	V	1
Input "High" voltage	V <sub>IH</sub>		0.8 DV <sub>DD</sub>			V	
Positive trigger voltage	V <sub>T</sub> <sup>+</sup>		1.37			V	2
Negative trigger voltage	V <sub>T</sub> <sup>-</sup>				1.33	V	
Hysteresis	V <sub>T</sub> <sup>+</sup> - V <sub>T</sub> <sup>-</sup>		0.2			V	
Input leakage current	I <sub>I</sub>	V <sub>IN</sub> = 0 V to DV <sub>DD</sub>	-1.0		+1.0	μA	3
		V <sub>IN</sub> = DV <sub>DD</sub> [with pull-up 98 kΩ]	-5.0		+5.0	μA	4
Input "Low" current	I <sub>IL</sub>	V <sub>IN</sub> = 0 V [with pull-up 98 kΩ]		-35		μA	4
Output "Low" voltage 1	V <sub>OL1</sub>	I <sub>OL</sub> = 8 mA			0.5	V	5
Output "High" voltage 1	V <sub>OH1</sub>	I <sub>OH</sub> = -8 mA	DV <sub>DD</sub> - 0.5			V	
Output "Low" voltage 2	V <sub>OL2</sub>	I <sub>OL</sub> = 12 mA			0.5	V	6
Output "High" voltage 2	V <sub>OH2</sub>	I <sub>OH</sub> = -12 mA	DV <sub>DD</sub> - 0.5			V	
Resolution	RES			9		Bit	7
Linearity error	EL	V <sub>REF</sub> = 1.24 V R <sub>REF</sub> = 4.8 kΩ R <sub>OUT</sub> = 75 Ω C <sub>VB</sub> = 0.1 μF	-3.0		+6.0	LSB	
Differential linearity error	ED		-1.0		+1.0	LSB	
Full-scale current	I <sub>FS</sub>			16.5		mA	
Output load resistance	R <sub>OUT</sub>			75		Ω	
Reference voltage	V <sub>REF</sub>		1.12	1.24	1.36	V	8
Reference resistance	R <sub>REF</sub>			4.8		kΩ	9
Oscillation frequency 1	F <sub>OSC1</sub>			24.5454		MHz	10
Oscillation frequency 2	F <sub>OSC2</sub>			29.5000		MHz	11
Oscillation frequency 3	F <sub>OSC3</sub>			24.0000		MHz	12
Supply current (a) (DV <sub>DD</sub> )	I <sub>DDa</sub>	Input image display mode : 1/4 VGA		55		mA	13
Supply current (a) (DV <sub>DD2</sub> , DAV <sub>DD</sub> , PLV <sub>DD</sub> )	I <sub>DD2a</sub>			115		mA	
Supply current (b) (DV <sub>DD</sub> )	I <sub>DDb</sub>	Input image display & capture image mode : VGA		70		mA	14
Supply current (b) (DV <sub>DD2</sub> , DAV <sub>DD</sub> , PLV <sub>DD</sub> )	I <sub>DD2b</sub>			125		mA	
Standby current (DV <sub>DD</sub> )	I <sub>DDSB</sub>	waiting for ARM operation with 1/4 clock		25		mA	15
Standby current (DV <sub>DD2</sub> , DAV <sub>DD</sub> , PLV <sub>DD</sub> )	I <sub>DD2SB</sub>			15		mA	

**NOTES :**

1. Applicable to IO symbols I, IU, IO8, IO8U, IO12, IO12U.
2. Applicable to IO symbol IS.
3. Applicable to IO symbols I, IO8, IO12, IS.
4. Applicable to IO symbols IU, IO8U, IO12U.
5. Applicable to IO symbols O8, IO8, IO8U.
6. Applicable to IO symbols O12, IO12, IO12U.
7. Applicable to IO symbol DAI.
8. Applicable to IO symbol DAVREF.
9. External resistance value. Applicable to IO symbol DAIREF.
10. Applicable to IO symbols IA (C24MI), OSC (C24MO).
11. Applicable to IO symbols IA (C29MI), OSC (C29MO).
12. Applicable to IO symbols IA (COMI), OSC (COMO).
13. Supply voltage  $DV_{DD} : 3.3 \text{ V}$ ,  $DV_{DD2} : 2.5 \text{ V}$   
Measuring conditions : 1 310 k-pixel CCD is used.  
CCD1 output image size 640 x 240,  
CCD2 output image size 320 x 240,  
16 bits external bus width, Local SRAM is not used.  
Always active modules :  
ARM, CCD1, CCD2, VENC, MEMC, DMAC  
Inactive modules :  
JPEG, SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO
14. Supply voltage  $DV_{DD} : 3.3 \text{ V}$ ,  $DV_{DD2} : 2.5 \text{ V}$   
Measuring conditions : 1 310 k-pixel CCD is used.  
CCD1 output image size 640 x 480,  
CCD2 output image size 640 x 480,  
16 bits external bus width, Local SRAM is not used.  
Always active modules :  
ARM, CCD1, CCD2, JPEG, VENC, MEMC, DMAC  
Inactive modules :  
SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO
15. Supply voltage  $DV_{DD} : 3.3 \text{ V}$ ,  $DV_{DD2} : 2.5 \text{ V}$   
Always active modules :  
ARM, MEMC, DMAC (Internal clock is divided into 1/4.)  
Inactive modules :  
JPEG, CCD1, CCD2, VENC, SRAM, USART, UART, USB, RESIZE, PLL (for PAL), AUDIOIF, GIO

## AC Characteristics

### SDRAM INTERFACE TIMING

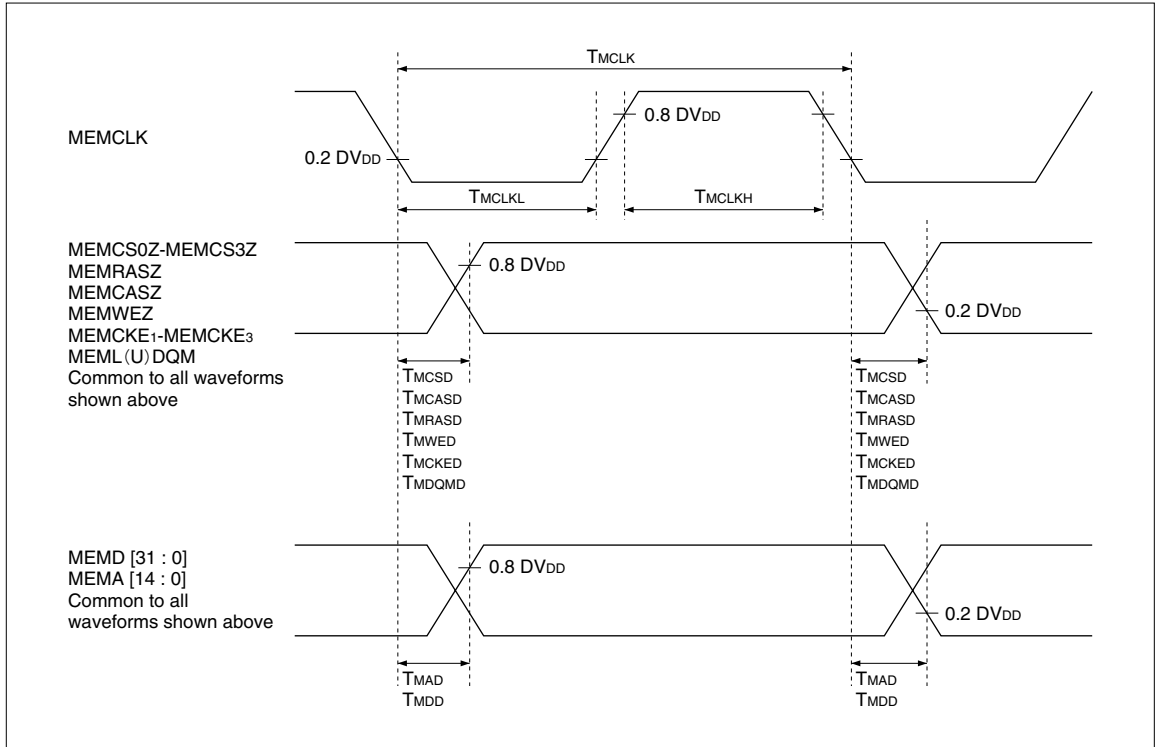


Fig. 3 SDRAM Output Timing

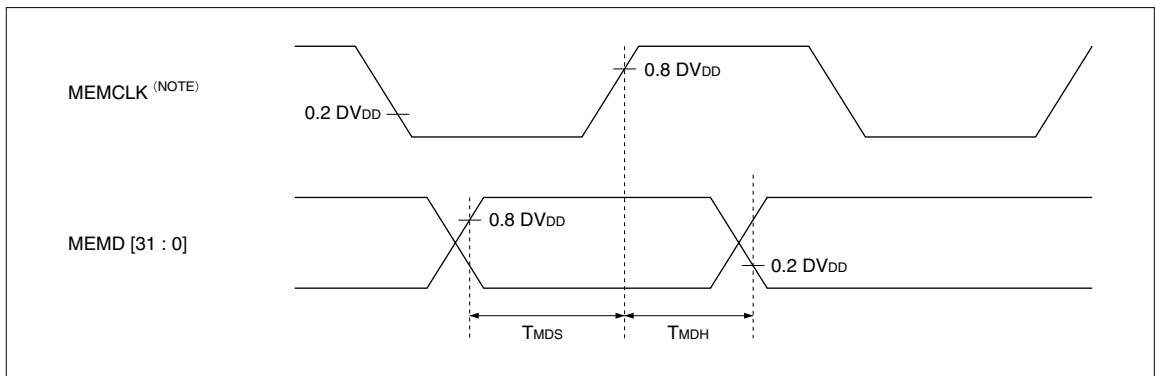


Fig. 4 SDRAM Input Timing

**NOTE :** MEMCLK is also used as the data latch clock inside the LR38666Y. Check the waveform of the incoming MEMCLK signal for no distortion.



(DV<sub>DD</sub> = 3.3 V, DV<sub>DD2</sub> = 2.5 V, C24MI = 24.5454 MHz, T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Clock cycle	TMCLK	20			ns	2
Pulse width (High)	TMCLKH	9			ns	2
Pulse width (Low)	TMCLKL	9			ns	2
Chip select delay	TMCS	0		7	ns	1
MEMRASZ output delay	TMRASD	0		7	ns	2
MEMCASZ output delay	TMCASD	0		7	ns	2
Write enable delay	TMWED	0		7	ns	2
Addressing delay	TMAD	0		7	ns	2
MEMCKE <sub>1</sub> to MEMCKE <sub>3</sub> output delay	TMCKED	0		7	ns	1
MEML(U)DQM output delay	TMDQMD	0		7	ns	2
Data output delay (write cycle)	TMDD	0		7	ns	2
Data setup delay (read cycle)	TMDS	10			ns	
Data hold delay (read cycle)	TMDH	3			ns	

**NOTES :**

1. Output load capacity C<sub>L</sub> = 10 pF
2. Output load capacity C<sub>L</sub> = 50 pF

FLASH MEMORY INTERFACE TIMING

• Read/write timing

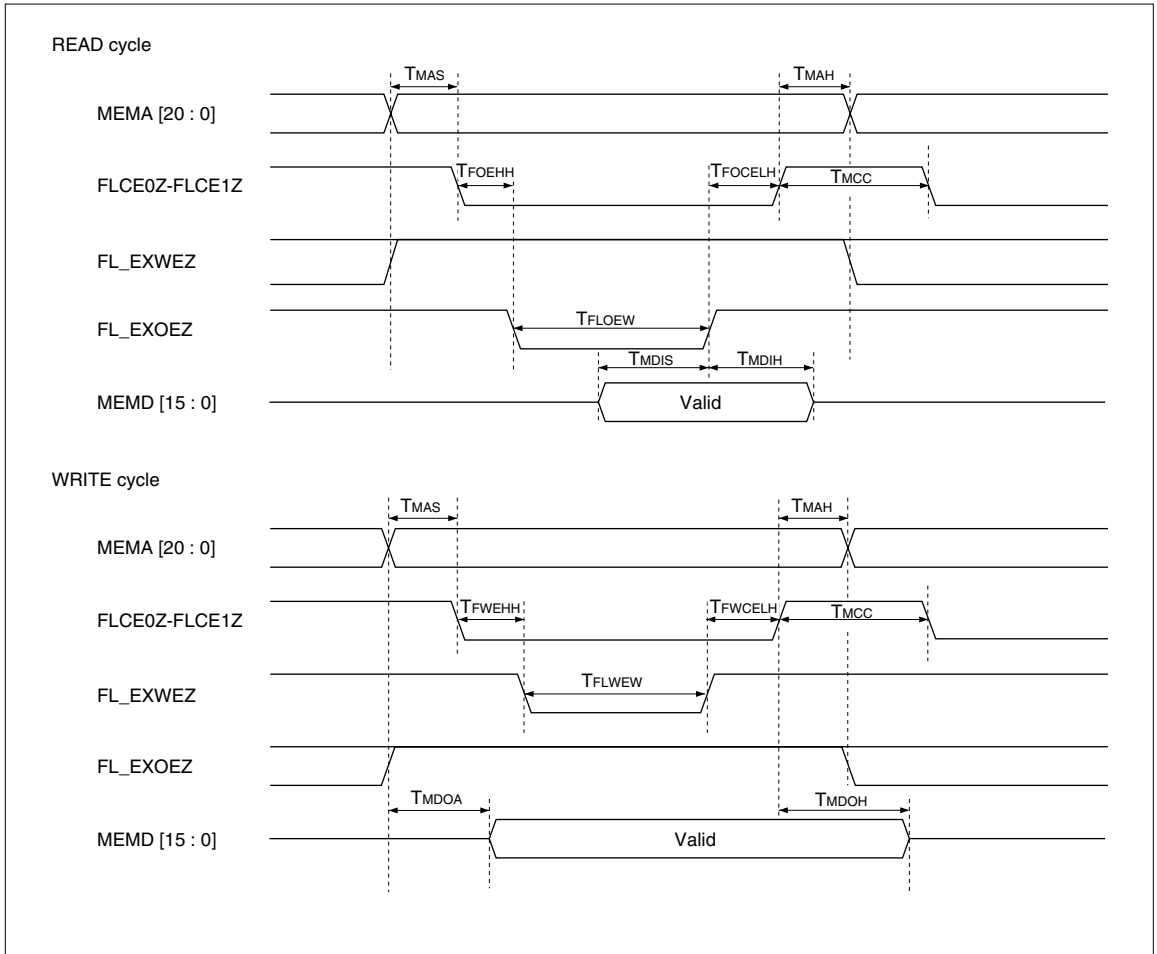


Fig. 5 Flash Memory Read/Write Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Address output setup time (relative to the falling edge of FLCE0Z/1Z)	T <sub>MAS</sub>	T <sub>CNT0</sub> - 5		ns	2
		T <sub>CNT5</sub> - 5			
Address output hold time (relative to the rising edge of FLCE0Z/1Z)	T <sub>MAH</sub>	T <sub>CNT4</sub> - 5		ns	2
		T <sub>CNT9</sub> - 5			
Minimum "High" period of FLCE0Z/1Z	T <sub>MCC</sub>	$\alpha$		ns	1
"High" hold time of FL_EXOEZ (relative to the falling edge of FLCE0Z/1Z)	T <sub>FOEHH</sub>	T <sub>CNT1</sub> - 5	T <sub>CNT1</sub> + 5	ns	2
"Low" pulse width of FL_EXOEZ	T <sub>FLOEW</sub>	T <sub>CNT2</sub> - 5	T <sub>CNT2</sub> + 5	ns	2
"Low" hold time of FLCE0Z/1Z (relative to the rising edge of FL_EXOEZ)	T <sub>FOCELH</sub>	T <sub>CNT3</sub> - 5	T <sub>CNT3</sub> + 5	ns	1
"High" hold time of FL_EXWEZ (relative to the falling edge of FLCE0Z/1Z)	T <sub>FWEHH</sub>	T <sub>CNT6</sub> - 5	T <sub>CNT6</sub> + 5	ns	2
"Low" pulse width of FL_EXWEZ	T <sub>FLWEW</sub>	T <sub>CNT7</sub> - 5	T <sub>CNT7</sub> + 5	ns	2
"Low" hold time of FLCE0Z/1Z (relative to the rising edge of FL_EXWEZ)	T <sub>FWCELH</sub>	T <sub>CNT8</sub> - 5	T <sub>CNT8</sub> + 5	ns	1
MEMD input setup time (relative to the rising edge of FL_EXOEZ)	T <sub>MDIS</sub>	2T <sub>MCLK</sub> - 5		ns	
MEMD input hold time (relative to the rising edge of FL_EXOEZ)	T <sub>MDIH</sub>	0		ns	
MEMD output delay (relative to the point at which the status of MEMA changes)	T <sub>MDOA</sub>	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	2
MEMD output hold time (relative to the rising edge of FLCE0Z/1Z)	T <sub>MDOH</sub>	T <sub>CNT9</sub> + 2T <sub>MCLK</sub> - 5	T <sub>CNT9</sub> + 2T <sub>MCLK</sub> + 5	ns	2

**NOTES :**

1. Output load capacity C<sub>L</sub> = 15 pF
2. Output load capacity C<sub>L</sub> = 50 pF

T<sub>CNT0</sub>, T<sub>CNT1</sub>, T<sub>CNT2</sub>, T<sub>CNT3</sub>, T<sub>CNT4</sub>, T<sub>CNT5</sub>, T<sub>CNT6</sub>, T<sub>CNT7</sub>, T<sub>CNT8</sub>, T<sub>CNT9</sub> and  $\alpha$  each has a value within the following range depending on the register setting. T<sub>MAS</sub> corresponds to T<sub>CNT0</sub> in read cycle and T<sub>CNT5</sub> in write cycle, T<sub>MAH</sub> corresponds to T<sub>CNT4</sub> in read cycle and T<sub>CNT9</sub> in write cycle.

T<sub>CNT0</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT1</sub> : 0T<sub>MCLK</sub> to 7T<sub>MCLK</sub>, T<sub>CNT2</sub> : 3T<sub>MCLK</sub> to 15T<sub>MCLK</sub>, T<sub>CNT3</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT4</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT5</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT6</sub> : 0T<sub>MCLK</sub> to 7T<sub>MCLK</sub>, T<sub>CNT7</sub> : 3T<sub>MCLK</sub> to 15T<sub>MCLK</sub>, T<sub>CNT8</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT9</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>

$\alpha$  : Min. "High" period between read cycles :  
 $3T_{MCLK} \leq (T_{CNT0} + T_{CNT4} + 1T_{MCLK}) \leq 7T_{MCLK}$   
 Min. "High" period from read cycle to write cycle :  
 $3T_{MCLK} \leq (T_{CNT4} + T_{CNT5} + 1T_{MCLK}) \leq 7T_{MCLK}$   
 Min. "High" period from write cycle to read cycle :  
 $3T_{MCLK} \leq (T_{CNT0} + T_{CNT9} + 1T_{MCLK}) \leq 7T_{MCLK}$   
 Min. "High" period between write cycles :  
 $3T_{MCLK} \leq (T_{CNT5} + T_{CNT9} + 1T_{MCLK}) \leq 7T_{MCLK}$

• Flash memory hard reset timing

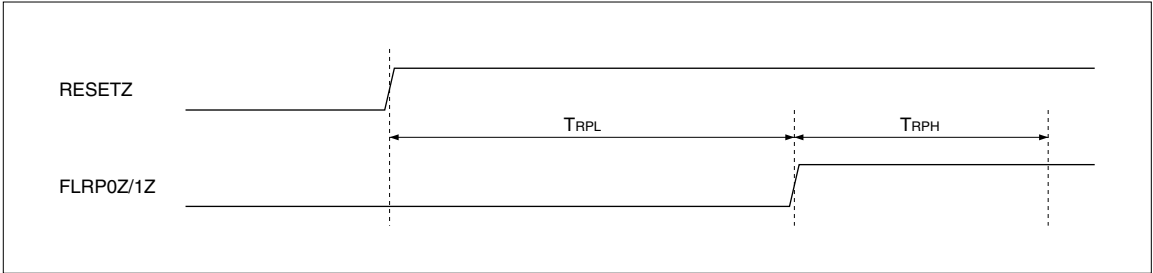


Fig. 6 Flash Memory Reset Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
"Low" pulse period of FLRP0Z/1Z (relative to the rising edge of RESETZ)	TRPL	11TMCLK	12TMCLK	ns	1
"High" pulse period of FLRP0Z/1Z (relative to the rising edge of FLR0/1Z)	TRPH	98TMCLK		ns	1, 2

NOTES :

1. Output load capacity CL = 15 pF
2. When the internal bus of the LR38666Y accesses to the flash memory during TRPH, it is made to wait.

• Flash memory initialization timing

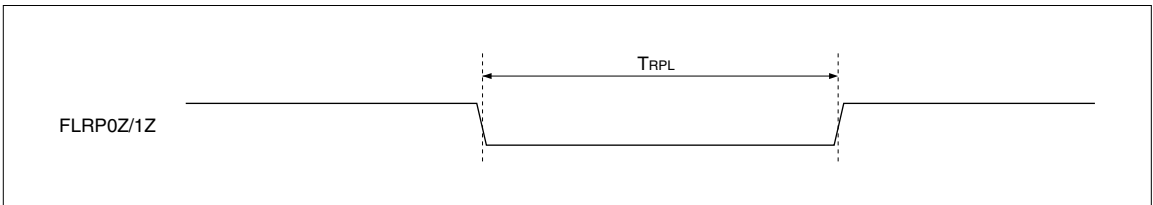


Fig. 7 Flash Memory Initialization Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
"Low" pulse period of FLRP0Z/1Z	TRPL	12TMCLK	12TMCLK	ns	1

NOTE :

1. Output load capacity CL = 15 pF

INTERFACE TIMING OF OTHER DEVICES

- S-type device timing

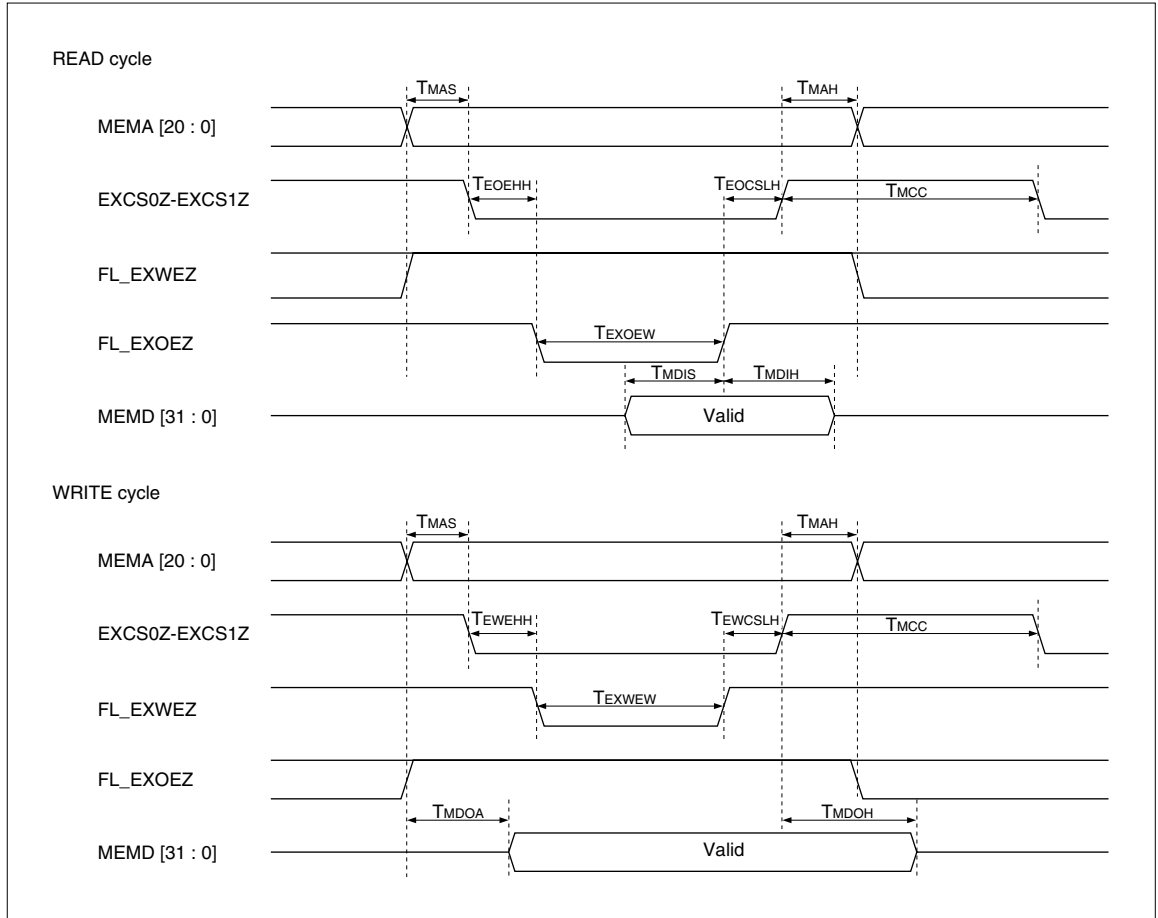


Fig. 8 S-type Device Read/Write Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = -10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	TMAS	TCNT00 - 5		ns	2
		TCNT05 - 5			
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	TMAH	TCNT04 - 5		ns	2
		TCNT09 - 5			
Minimum "High" period of EXCS0Z/1Z	TMCC	$\alpha$		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of EXCS0Z/1Z)	TEOEHH	TCNT01 - 5	TCNT01 + 5	ns	2
"Low" pulse width of FL_EXOEZ	TEXOEW	TCNT02 - 5	TCNT02 + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXOEZ)	TEWCSLH	TCNT03 - 5	TCNT03 + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of EXCS0Z/1Z)	TEWEHH	TCNT06 - 5	TCNT06 + 5	ns	2
"Low" pulse width of FL_EXWEZ	TEXWEW	TCNT07 - 5	TCNT07 + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXWEZ)	TEWCSLH	TCNT08 - 5	TCNT08 + 5	ns	1
Input setup period of MEMD (relative to the rising edge of FL_EXOEZ)	TMDIS	2TMCLK - 5		ns	
Input hold period of MEMD (relative to the rising edge of FL_EXOEZ)	TMDIH	0		ns	
Output delay period of MEMD (relative to MEMA)	TMDOA	2TMCLK - 5	2TMCLK + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	TMDOH	TCNT09 +	TCNT09 +	ns	2
		2TMCLK - 5	2TMCLK + 5		

**NOTES :**

1. Output load capacity CL = 15 pF
2. Output load capacity CL = 50 pF

TCNT00, TCNT01, TCNT02, TCNT03, TCNT04, TCNT05, TCNT06, TCNT07, TCNT08, TCNT09 and  $\alpha$  each has a value within the following range depending on the register setting.

TMAS corresponds to TCNT00 in read cycle and TCNT05 in write cycle, and TCNT04 in read cycle and TCNT09 in write cycle.

TCNT00 : 1TMCLK to 3TMCLK, TCNT01 : 0TMCLK to 3TMCLK, TCNT02 : 3TMCLK to 15TMCLK, TCNT03 : 0TMCLK to 7TMCLK, TCNT04 : 1TMCLK to 7TMCLK, TCNT05 : 1TMCLK to 3TMCLK, TCNT06 : 0TMCLK to 3TMCLK, TCNT07 : 3TMCLK to 15TMCLK, TCNT08 : 0TMCLK to 7TMCLK, TCNT09 : 1TMCLK to 7TMCLK

$\alpha$  : Min. "High" period between read cycles :

$$3TMCLK \leq (TCNT00 + TCNT04 + 1TMCLK) \leq 11TMCLK$$

Min. "High" period from read cycle to write cycle :

$$3TMCLK \leq (TCNT04 + TCNT05 + 1TMCLK) \leq 11TMCLK$$

Min. "High" period from write cycle to read cycle :

$$3TMCLK \leq (TCNT00 + TCNT09 + 1TMCLK) \leq 11TMCLK$$

Min. "High" period between write cycles :

$$3TMCLK \leq (TCNT05 + TCNT09 + 1TMCLK) \leq 11TMCLK$$

• I-type timing

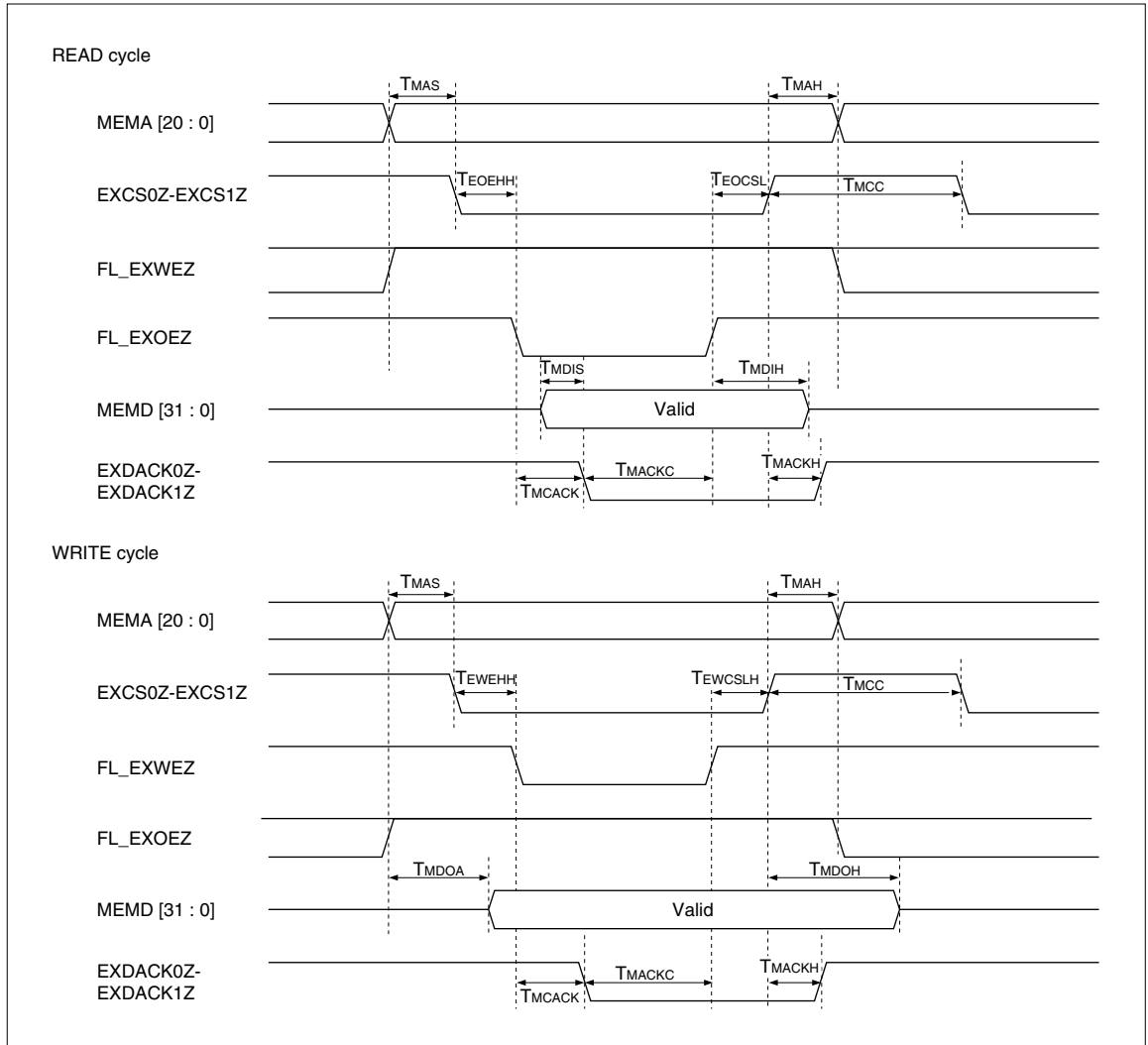


Fig. 9 I-type Read/Write Cycle

**NOTE :**

It is able to invert the polarity of EXDACK0Z/1Z by internal register.

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = -10 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	T <sub>MAS</sub>	T <sub>CNT10</sub> - 5		ns	2
		T <sub>CNT14</sub> - 5			
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	T <sub>MAH</sub>	T <sub>CNT13</sub> - 5		ns	2
		T <sub>CNT17</sub> - 5			
Minimum "High" period of EXCS0Z/1Z	T <sub>MCC</sub>	$\alpha$		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of EXCS0Z/1Z)	T <sub>EOEHH</sub>	T <sub>CNT11</sub> - 5	T <sub>CNT11</sub> + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXOEZ)	T <sub>EOCSLH</sub>	T <sub>CNT12</sub> - 5	T <sub>CNT12</sub> + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of EXCS0Z/1Z)	T <sub>EWEEH</sub>	T <sub>CNT15</sub> - 5	T <sub>CNT15</sub> + 5	ns	2
"Low" hold period of EXCS0Z/1Z (relative to the rising edge of FL_EXWEZ)	T <sub>EWCSLH</sub>	T <sub>CNT16</sub> - 5	T <sub>CNT16</sub> + 5	ns	1
Input setup period of MEMD (relative to the falling edge of EXDACK0Z/1Z)	T <sub>MDIS</sub>	0		ns	
Input hold period of MEMD (relative to the rising edge of FL_EXOEZ)	T <sub>MDIH</sub>	0		ns	
Output delay period of MEMD (relative to MEMA)	T <sub>MDOA</sub>	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	T <sub>MDOH</sub>	T <sub>CNT17</sub> + 2T <sub>MCLK</sub> - 5	T <sub>CNT17</sub> + 2T <sub>MCLK</sub> + 5	ns	2
Setup period of EXDACK0Z/1Z (relative to the falling edge of FL_EXOEZ, FL_EXWEZ)	T <sub>MACK</sub>	0		ns	
Rising period of FL_EXOEZ/FL_EXWEZ (relative to the falling edge of EXDACK0Z/1Z)	T <sub>MACKC</sub>	2T <sub>MCLK</sub> - 5	3T <sub>MCLK</sub> + 5	ns	2
Hold period of EXDACK0Z/1Z (relative to the rising edge of EXCS0Z/1Z)	T <sub>MACKH</sub>	0		ns	

**NOTES :**

1. Output load capacity CL = 15 pF
2. Output load capacity CL = 50 pF

T<sub>CNT10</sub>, T<sub>CNT11</sub>, T<sub>CNT12</sub>, T<sub>CNT13</sub>, T<sub>CNT14</sub>, T<sub>CNT15</sub>, T<sub>CNT16</sub>, T<sub>CNT17</sub>, and  $\alpha$  each has a value within the following range depending on the register setting. T<sub>MAS</sub> corresponds to T<sub>CNT10</sub> in read cycle and T<sub>CNT14</sub> in write cycle. T<sub>MAH</sub> corresponds to T<sub>CNT13</sub> in read cycle and T<sub>CNT17</sub> in write cycle.

T<sub>CNT10</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT11</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT12</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT13</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT14</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT15</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT16</sub> : 0T<sub>MCLK</sub> to 3T<sub>MCLK</sub>, T<sub>CNT17</sub> : 1T<sub>MCLK</sub> to 3T<sub>MCLK</sub>

$\alpha$  : Min. "High" period between read cycles :

$$3T_{MCLK} \leq (T_{CNT10} + T_{CNT13} + 1T_{MCLK}) \leq 7T_{MCLK}$$

Min. "High" period from read cycle to write cycle :  $3T_{MCLK} \leq (T_{CNT13} + T_{CNT14} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period from write cycle to read cycle :  $3T_{MCLK} \leq (T_{CNT10} + T_{CNT17} + 1T_{MCLK}) \leq 7T_{MCLK}$

Min. "High" period between write cycles :  $3T_{MCLK} \leq (T_{CNT14} + T_{CNT17} + 1T_{MCLK}) \leq 7T_{MCLK}$



• M-type timing

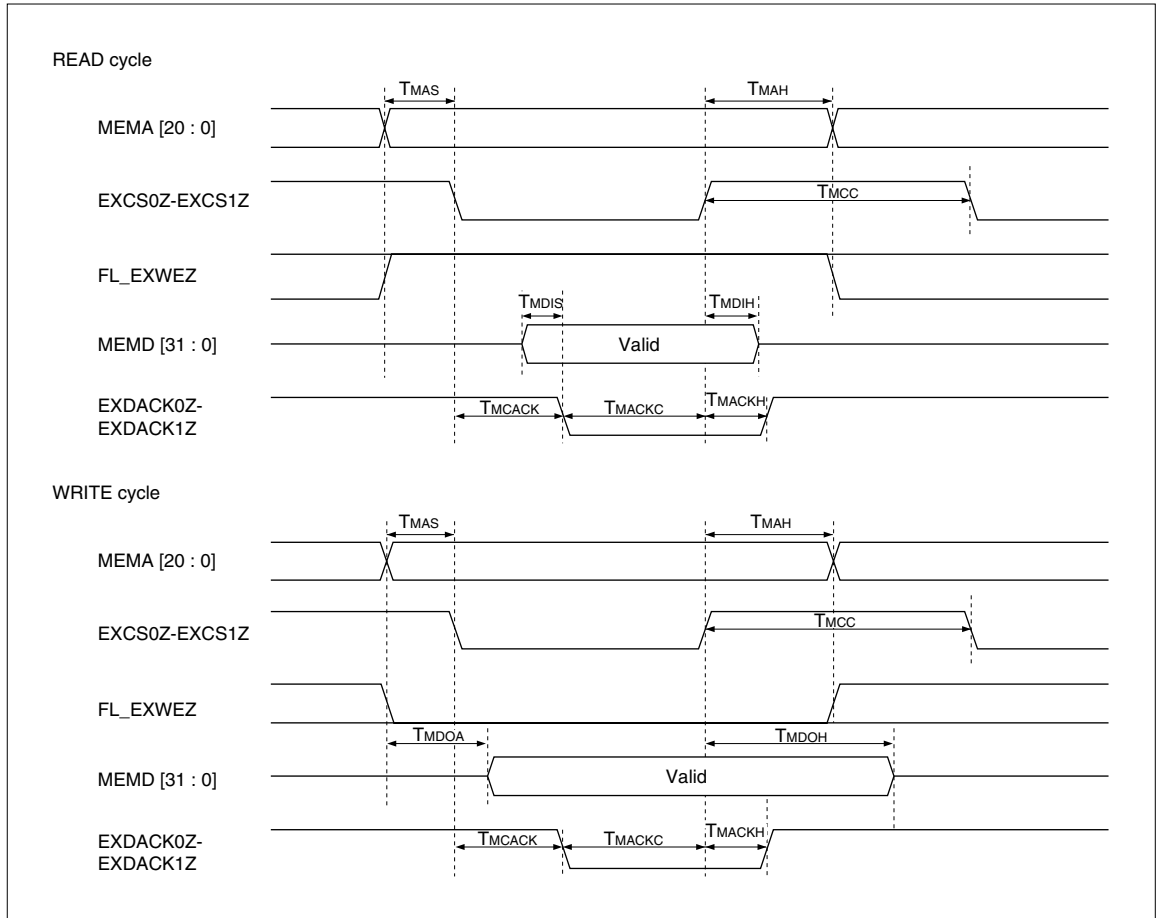


Fig. 10 M-type Read/Write Cycle

**NOTE :**

It is able to invert the polarity of EXDACK0Z/1Z by internal register.

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA (relative to the falling edge of EXCS0Z/1Z)	TMAS	TCNT20 - 5		ns	2
		TCNT22 - 5			
Output hold period of MEMA (relative to the rising edge of EXCS0Z/1Z)	TMAH	TCNT21 - 5		ns	2
		TCNT23 - 5			
Minimum "High" period of EXCS0Z/1Z	TMCC	$\alpha$		ns	1
Input setup period of MEMD (relative to the falling edge of EXDACKZ)	TMDIS	0		ns	
Input hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	TMDIH	0		ns	
Output delay period of MEMD (relative to MEMA)	TMDOA	2TMCLK - 5	2TMCLK + 5	ns	2
Output hold period of MEMD (relative to the rising edge of EXCS0Z/1Z)	TMDOH	TCNT23 + 2TMCLK - 5	TCNT23 + 2TMCLK + 5	ns	2
Setup period of EXDACK0Z/1Z (relative to the falling edge of EXCS0Z/1Z)	TMCAK	0		ns	
Rising period of EXCS0Z/1Z (relative to the falling edge of EXDACK0Z/1Z)	TMACKC	2TMCLK - 5	3TMCLK + 5	ns	1
Hold period of EXDACK0Z/1Z (relative to the rising edge of EXCS0Z/1Z)	TMACKH	0		ns	

**NOTES :**

1. Output load capacity CL = 15 pF
2. Output load capacity CL = 50 pF

TCNT20, TCNT21, TCNT22, TCNT23, and  $\alpha$  each has a value within the following range depending on the register setting. TMAS corresponds to TCNT20 in read cycle and TCNT22 in write cycle, and TMAH corresponds to TCNT21 in read cycle and TCNT23 in write cycle.

TCNT20 : 1TMCLK to 3TMCLK, TCNT21 : 1TMCLK to 3TMCLK, TCNT22 : 1TMCLK to 3TMCLK, TCNT23 : 1TMCLK to 3TMCLK

$\alpha$  : Min. "High" period between read cycles :  
 $3TMCLK \leq (TCNT20 + TCNT21 + 1TMCLK) \leq 7TMCLK$

Min. "High" period from read cycle to write cycle :  
 $3TMCLK \leq (TCNT21 + TCNT22 + 1TMCLK) \leq 7TMCLK$

Min. "High" period from write cycle to read cycle :  
 $3TMCLK \leq (TCNT20 + TCNT23 + 1TMCLK) \leq 7TMCLK$

Min. "High" period between write cycles :  
 $3TMCLK \leq (TCNT22 + TCNT23 + 1TMCLK) \leq 7TMCLK$

• CompactFlash attribute memory access timing

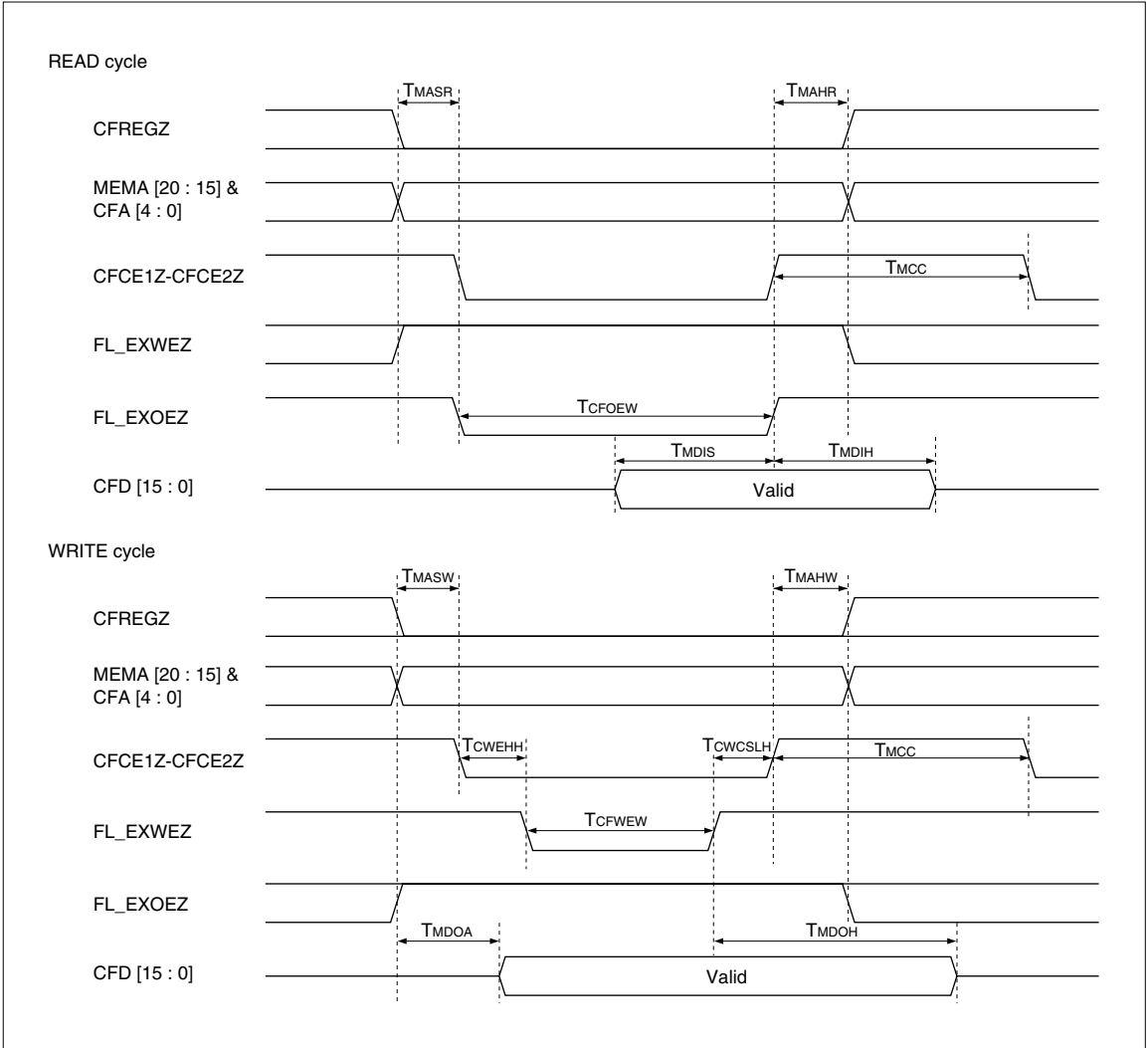


Fig. 11 CompactFlash Attribute Memory Read/Write Cycle

(DV<sub>DD</sub> = 3.3 V, DV<sub>DD2</sub> = 2.5 V, T<sub>A</sub> = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA [20 : 15] & CFA at reading (relative to the falling edge of CFCE1Z/2Z)	T <sub>MASR</sub>	2T <sub>MCLK</sub> - 5		ns	2
Output setup period of MEMA [20 : 15] & CFA at writing (relative to the falling edge of CFCE1Z/2Z)	T <sub>MASW</sub>	T <sub>MCLK</sub> - 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at reading (relative to the rising edge of CFCE1Z/2Z)	T <sub>MAHR</sub>	3T <sub>MCLK</sub> - 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at writing (relative to the rising edge of CFCE1Z/2Z)	T <sub>MAHW</sub>	T <sub>MCLK</sub> - 5		ns	2
Minimum "High" period of CFCE1Z/2Z	T <sub>MCC</sub>	3T <sub>MCLK</sub> - 5		ns	1
"Low" pulse width of FL_EXOEZ	T <sub>CFOW</sub>	17T <sub>MCLK</sub> - 5	17T <sub>MCLK</sub> + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of CFCE1Z/2Z)	T <sub>CWEHH</sub>	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
"Low" pulse width of FL_EXWEZ	T <sub>CFWEW</sub>	8T <sub>MCLK</sub> - 5	8T <sub>MCLK</sub> + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXWEZ)	T <sub>CWCSLH</sub>	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
Input setup period of CFD (relative to the rising edge of FL_EXOEZ)	T <sub>MDIS</sub>	2T <sub>MCLK</sub> - 5		ns	
Input hold period of CFD (relative to the rising edge of FL_EXOEZ)	T <sub>MDIH</sub>	0		ns	
Output delay period of CFD (relative to MEMA [20 : 15] & CFA)	T <sub>MDOA</sub>	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
Output hold period of CFD (relative to the rising edge of FL_EXWEZ)	T <sub>MDOH</sub>	5T <sub>MCLK</sub> - 5	5T <sub>MCLK</sub> + 5	ns	1

**NOTES :**

1. Output load capacity C<sub>L</sub> = 50 pF
2. MEMA [20 : 15] output load capacity C<sub>L</sub> = 50 pF, CFA [4 : 0] output load capacity C<sub>L</sub> = 30 pF.

• CompactFlash common memory access timing

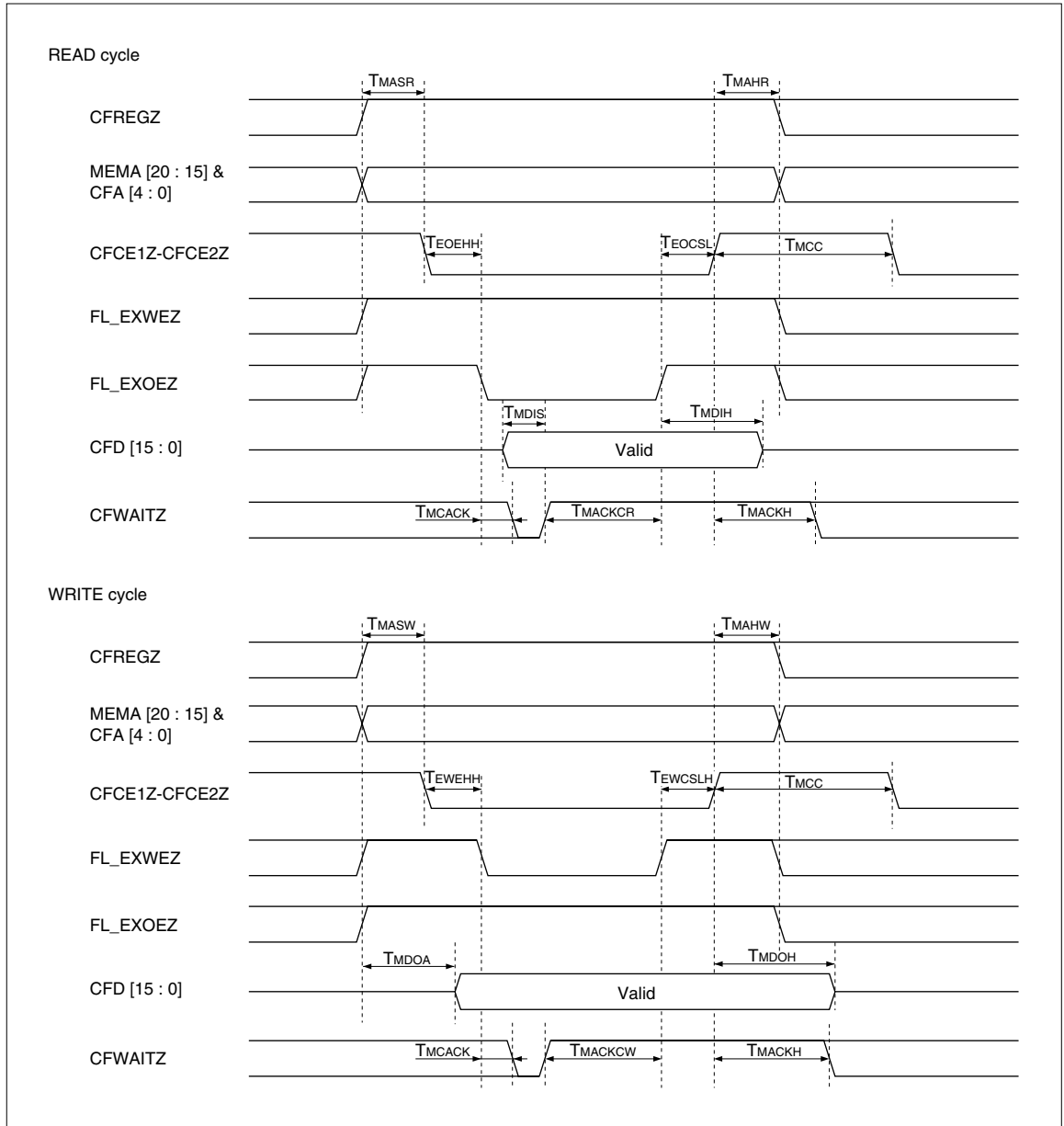


Fig. 12 CompactFlash Common Memory Read/Write Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of MEMA [20 : 15] & CFA at reading (relative to the falling edge of CFCE1Z/2Z)	TMASR	T <sub>MCLK</sub> - 5		ns	2
Output setup period of MEMA [20 : 15] & CFA at writing (relative to the falling edge of CFCE1Z/2Z)	TMASW	T <sub>MCLK</sub> - 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at reading (relative to the rising edge of CFCE1Z/2Z)	TMAHR	2T <sub>MCLK</sub> - 5		ns	2
Output hold period of MEMA [20 : 15] & CFA at writing (relative to the rising edge of CFCE1Z/2Z)	TMAHW	T <sub>MCLK</sub> - 5		ns	2
Minimum "High" period of CFCE1Z/2Z	TMCC	3T <sub>MCLK</sub> - 5		ns	1
"High" hold period of FL_EXOEZ (relative to the falling edge of CFCE1Z/2Z)	TEOEH	T <sub>MCLK</sub> - 5	T <sub>MCLK</sub> + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXOEZ)	TEOCSLH	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
"High" hold period of FL_EXWEZ (relative to the falling edge of CFCE1Z/2Z)	TEWEH	T <sub>MCLK</sub> - 5	T <sub>MCLK</sub> + 5	ns	1
"Low" hold period of CFCE1Z/2Z (relative to the rising edge of FL_EXWEZ)	TEWCSLH	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
Input setup period of CFD (relative to the rising edge of CFWAITZ)	TMDIS	0		ns	
Input hold period of CFD (relative to the rising edge of FL_EXOEZ)	TMDIH	0		ns	
Output delay period of CFD (relative to MEMA [20 : 15] & CFA)	TMDOA	2T <sub>MCLK</sub> - 5	2T <sub>MCLK</sub> + 5	ns	1
Output hold period of CFD (relative to the rising edge of CFCE1Z/2Z)	TMDOH	5T <sub>MCLK</sub> - 5	5T <sub>MCLK</sub> + 5	ns	1
Determination period of CFWAITZ (relative to the falling edge of FL_EXOEZ/FL_EXWEZ)	TMCK		2T <sub>MCLK</sub> + 5	ns	
Rising period of FL_EXOEZ (relative to the rising edge of CFWAITZ)	TMACKCR	2T <sub>MCLK</sub> - 5	3T <sub>MCLK</sub> + 5	ns	1
Rising period of FL_EXWEZ (relative to the rising edge of CFWAITZ)	TMACKCW	4T <sub>MCLK</sub> - 5	5T <sub>MCLK</sub> + 5	ns	1
Hold period of CFWAITZ (relative to the rising edge of EXDACK0Z/1Z)	TMACKH	0		ns	

**NOTES :**

1. Output load capacity CL = 50 pF
2. MEMA [20 : 15] output load capacity CL = 50 pF, CFA [4 : 0] output load capacity CL = 30 pF.

• SmartMedia access timing

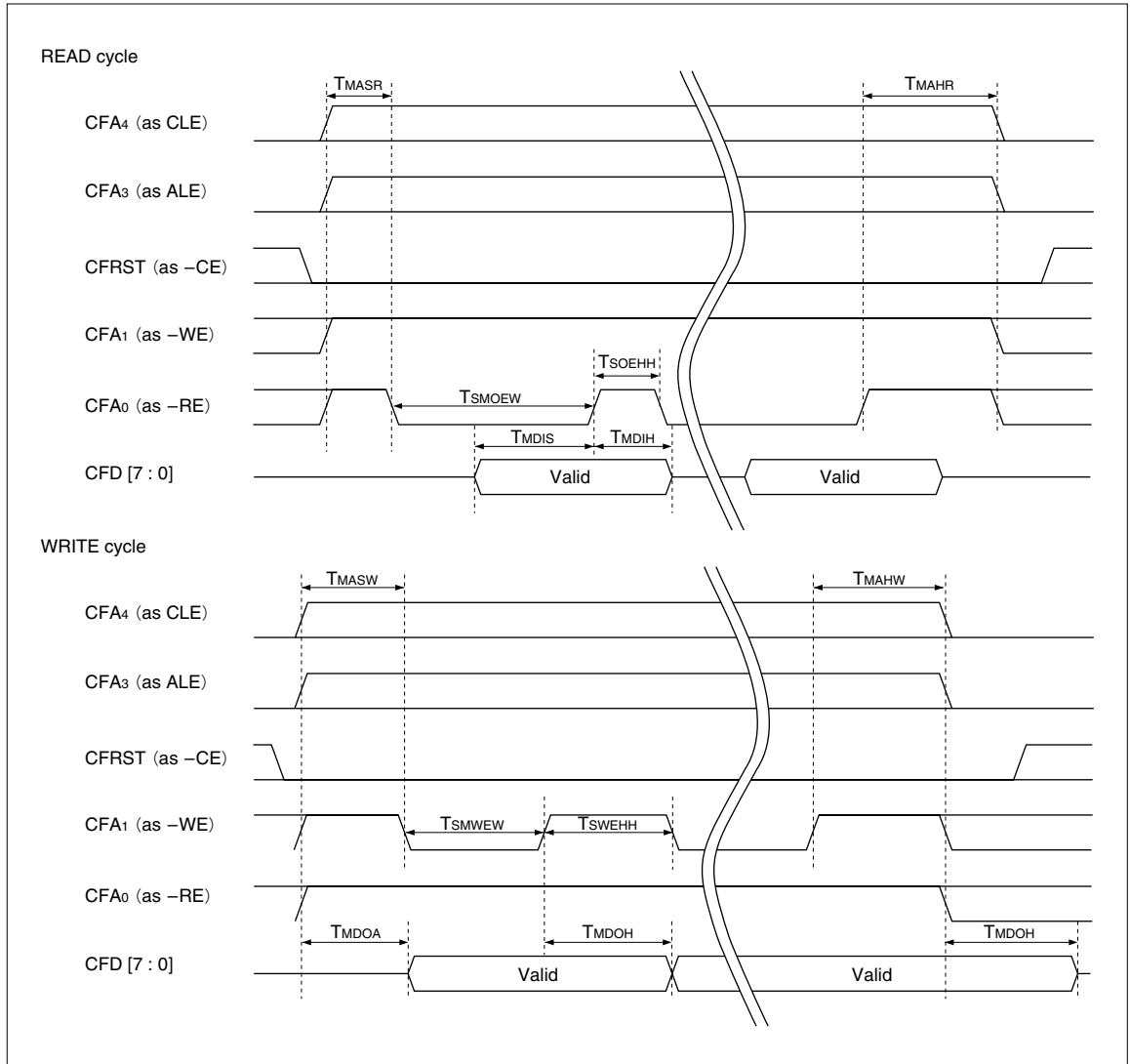


Fig. 13 SmartMedia Read/Write Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		UNIT	NOTE
		MIN.	MAX.		
Output setup period of CLE, ALE, $\text{-WE}$ at reading (relative to the falling edge of $\text{-RE}$ )	TMASR	2TMCLK - 5		ns	1
Output setup period of CLE, ALE, $\text{-RE}$ at writing (relative to the falling edge of $\text{-WE}$ )	TMASW	2TMCLK - 5		ns	1
Output hold period of CLE, ALE, $\text{-WE}$ at reading (relative to the rising edge of $\text{-RE}$ )	TMAHR	3TMCLK - 5		ns	1
Output hold period of CLE, ALE, $\text{-RE}$ at writing (relative to the rising edge of $\text{-WE}$ )	TMAHW	3TMCLK - 5		ns	1
"Low" pulse width of $\text{-RE}$	TSMOEW	4TMCLK - 5	4TMCLK + 5	ns	1
"High" pulse width of $\text{-RE}$	TSOEHH	2TMCLK - 5	2TMCLK + 5	ns	1
"Low" pulse width of $\text{-WE}$	TSMWEW	3TMCLK - 5	3TMCLK + 5	ns	1
"High" pulse width of $\text{-WE}$	TSWEHH	2TMCLK - 5	2TMCLK + 5	ns	
Input setup period of CFD [7 : 0] (relative to the rising edge of $\text{-RE}$ )	TMDIS	2TMCLK - 5		ns	
Input hold period of CFD [7 : 0] (relative to the rising edge of $\text{-RE}$ )	TMDIH	0		ns	
Output delay period of CFD [7 : 0] (relative to the rising edge of CLE, ALE)	TMDOA	2TMCLK - 5	2TMCLK + 5	ns	1
Output hold period of CFD [7 : 0] (relative to the rising edge of $\text{-WE}$ )	TMDOH	2TMCLK - 5	2TMCLK + 5	ns	1

**NOTE :**

1. Output load capacity CL = 50 pF



USB TIMING

• USB transmitting timing

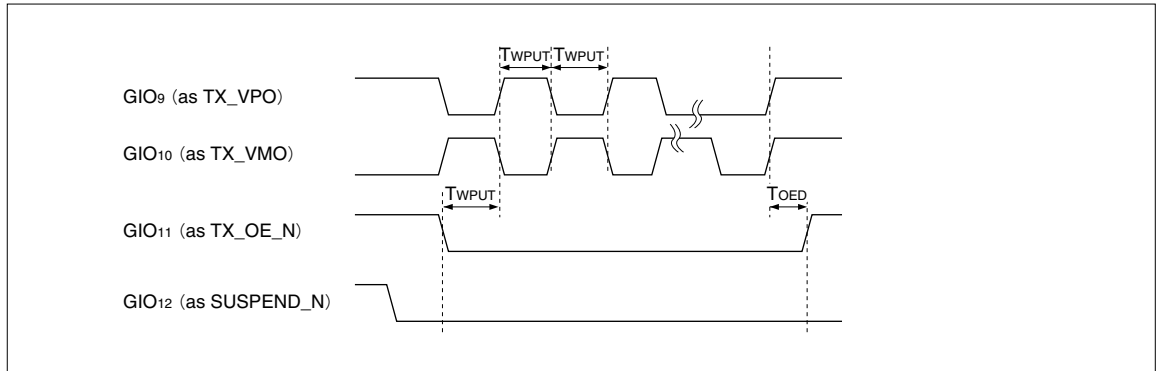


Fig. 14 USB Transmitting Cycle

( $DV_{DD} = 3.3\text{ V}$ ,  $DV_{DD2} = 2.5\text{ V}$ ,  $T_A = 0\text{ to }+70^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Transmission period of 1 bit	$T_{WPUT}$	80	83	86	ns	1, 2
Output delay period of TX_OE_N	$T_{OED}$	162	167	172	ns	2

NOTES :

1. When "High" or "Low" continues for N bits period, it is  $(48\text{ MHz})^{-1} \times 4 \times N \pm 3\text{ ns}$ .
2. Output load capacity  $C_L = 15\text{ pF}$
3. USB module will be reset when SE0 status ( $GIO_{13} = GIO_{14} = \text{"Low"}$ ) is input longer than  $2.5\text{ }\mu\text{s}$ , in transmitting, so choose USB transceiver IC carefully.

• USB receiving timing

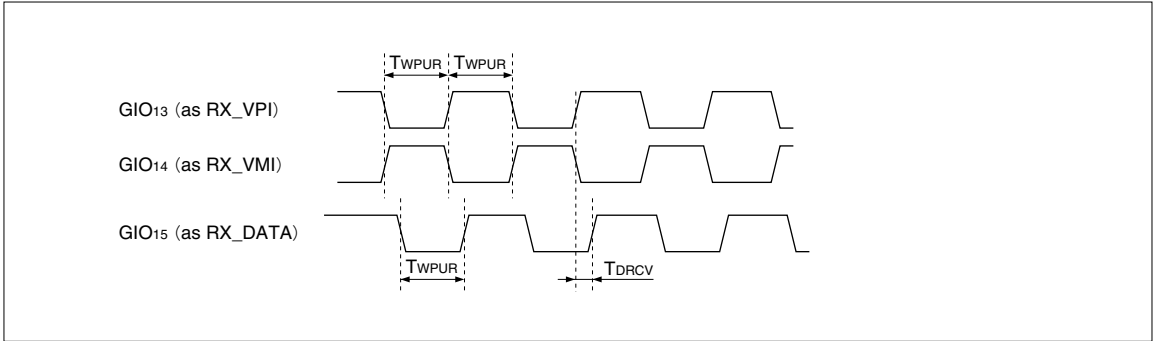


Fig. 15 USB Receiving Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Receiving period of 1 bit	TWPUR	68	83	98	ns	1
Permissible delay period of received data	TDRCV	0		14	ns	

NOTE :

- When "High" or "Low" continues for N bits period, it is  $(48 \text{ MHz})^{-1} \times 4 \times N \pm 3 \text{ ns}$ .

UART TIMING

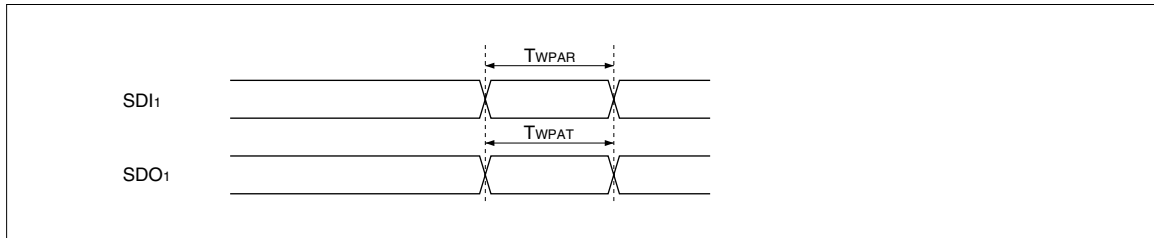


Fig. 16 UART Communication Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
SDI1 input pulse width	TWPUR	8.57			μs	2
SDO1 output pulse width	TWPAT	8.57			μs	1, 2

NOTES :

- Output load capacity CL = 15 pF
- The baud rate is assumed to be 115.2 k bps.

## USART TIMING

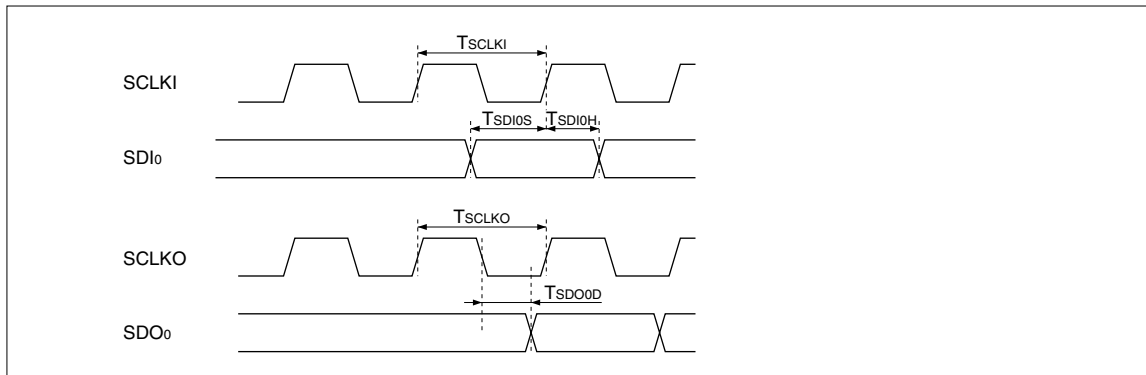


Fig. 17 USART Communication Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
SCLKI clock input cycle	T_SCLKI		T_BRCK		ns	2
SDI0 input setup time	T_SDI0S	1/4 T_BRCK			ns	2
SDI0 input hold time	T_SDI0H	1/4 T_BRCK			ns	2
SCLKO clock output cycle	T_SCLKO		T_BRCK		ns	1, 2
SDO0 output delay	T_SDO0D	-1/4 T_BRCK		1/4 T_BRCK	ns	1, 2

## NOTES :

- Output load capacity  $C_L = 15 \text{ pF}$
- T\_BRCK means the baud rate clock frequency.  
If COMI (24 MHz) is used and baud rate generator control register BKGC is set to 0x138 (9 600 bps), T\_BRCK is given as follows :  $T_{BRCK} = [48 \text{ MHz}/(312 \cdot 16)]^{-1} = 104 \text{ } \mu\text{s}$

## GIO PORT PWM OUTPUT TIMING

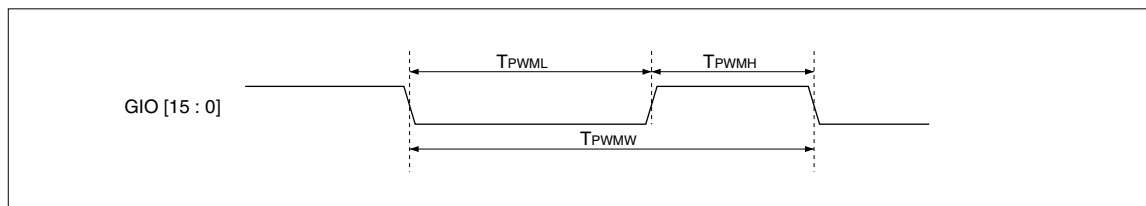


Fig. 18 GIO I/O Timing

PARAMETER	SYMBOL	CONDITIONS	UNIT	NOTE
Output pulse width	TPWMW	256	T_BCLK	1, 2
"Low" output pulse width	TPWML	0 to 256	T_BCLK	1, 2
"High" output pulse width	TPWMH	TPWMW - TPWML	T_BCLK	1, 2

## NOTES :

- Output load capacity  $C_L = 15 \text{ pF}$
- T\_BCLK is twice the internal bus clock period.

## CCD INTERFACE TIMING

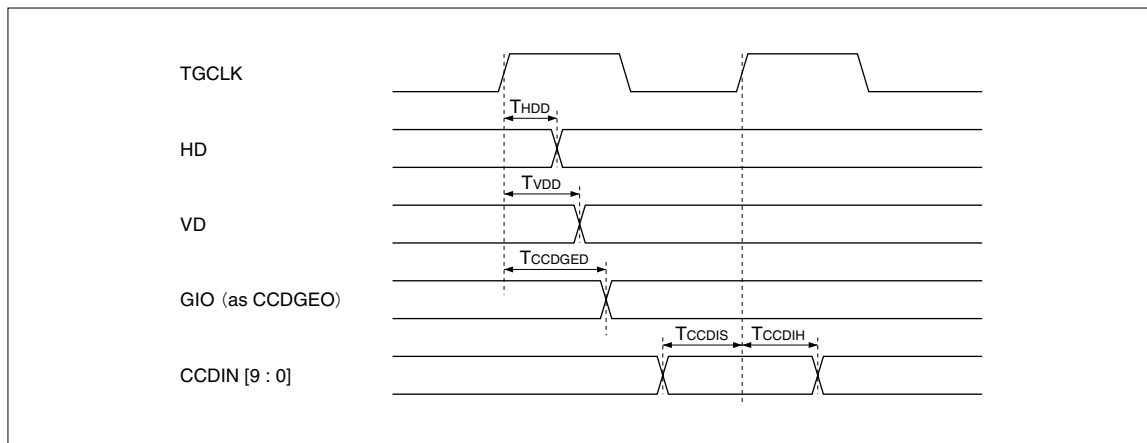


Fig. 19 CCD Data Input Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
HD output delay	$T_{HDD}$			15	ns	1
VD output delay	$T_{VDD}$			15	ns	1
CCDGEO output delay	$T_{CCDGED}$			15	ns	1
CCDIN input setup time	$T_{CCDIS}$	10			ns	
CCDIN input hold time	$T_{CCDIH}$	10			ns	

**NOTE :**

1. Output load capacity  $C_L = 15$  pF

## AUDIOIF TIMING

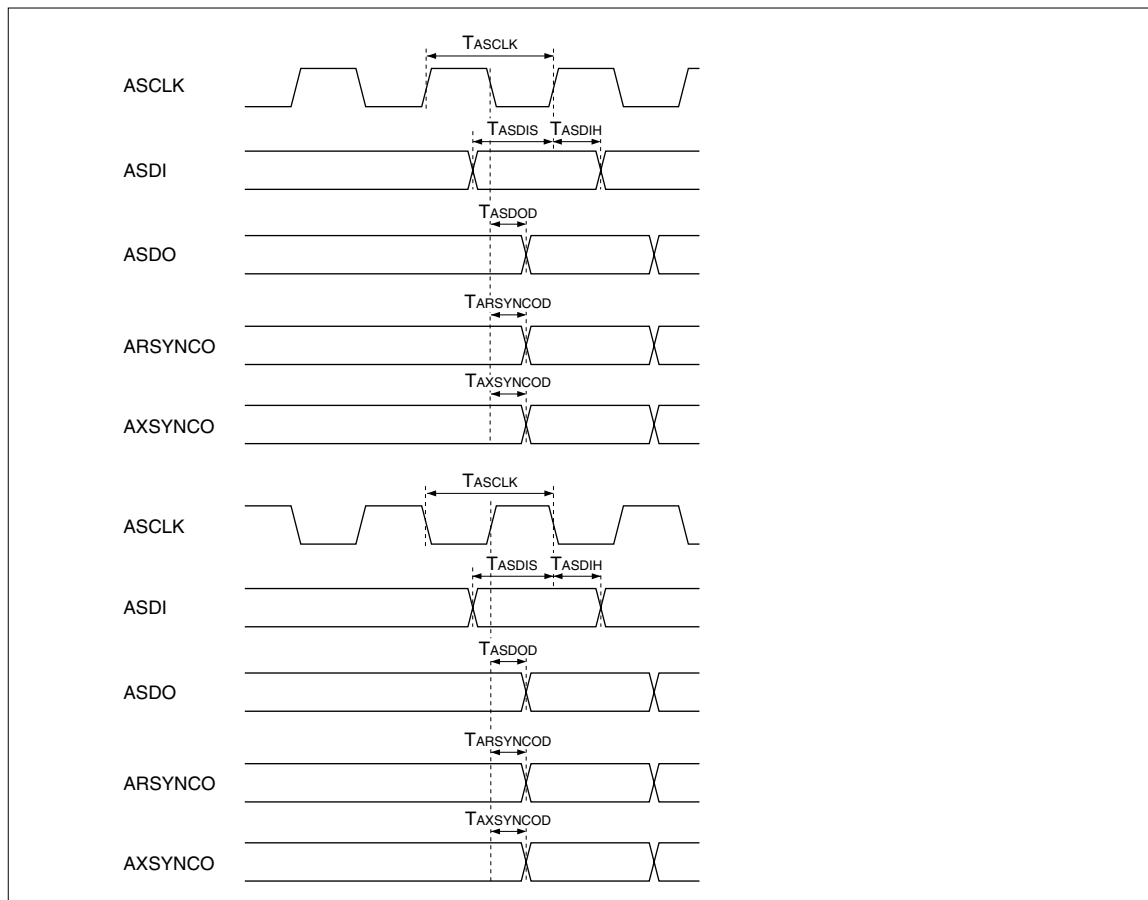


Fig. 20 AUDIOIF Communication Cycle

(DVDD = 3.3 V, DVDD2 = 2.5 V, TA = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS			UNIT	NOTE
		MIN.	TYP.	MAX.		
Input setup period of ASDI	TASDIS	1/4 TASCCK			ns	2
Input hold period of ASDI	TASDIH	1/4 TASCCK			ns	2
Clock output cycle of ASCLK	TASCLK		TASCCK		ns	1, 2
Output delay period of ASDO	TASDDOD			20	ns	1
Output delay period of ARSYNCO	TARSYNCO			20	ns	1
Output delay period of AXSYNCO	TAXSYNCO			20	ns	1

## NOTES :

1. Output load capacity CL = 15 pF

2. TASCCK means the clock period of bit-shift-clock.

If the sampling clock frequency is 32 kHz, TCLK input is 16.384 MHz (512 fs) and bit-shift-clock register (BSCG) is set to 0x0010 (bit-shift-clock is 1.024 MHz or 32 fs), TASCCK is given as follows :

$$T_{ASCK} = (16.384 \text{ MHz}/16)^{-1} = 976.5625 \text{ ns}$$

PACKAGE OUTLINES

240 CSP (T-TFBGA240-1414)

(Unit : mm)

