LRF020

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

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UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

1. General Information

The LRF020 module is an IEEE 802.15.4 compliant solution that satisfies the requirements of low-cost and long-range wireless applications. The module, containing UBEC's UZ2400D, UP2206, UA2725 and other necessary components, operates in the ISM 2.4 GHz frequency band. The corresponding MCU can accesses to various UZ2400D internal subunits, such as registers, FIFOs, and security key table, via a 4-wire SPI bus. Its small form factor saves valuable board spaces and provides a reliable delivery of critical data between the devices.

2. Features

- 2.4GHz IEEE 802.15.4 compliant
- 3.0 ~ 3.6V Operation
- Effective Distance: 1000 meters (line of sight, environment dependent, typical)
- MMCX Connector or LTCC antenna on PCB(optional when mass production)
- Additional 2 GSG (ground-signal-ground) Interfaces Provided
- RX Sensitivity: -100dBm, typical
- TX Output Power: 18dBm, typical
- TX Current Consumption: 210mA, typical
- RX Current Consumption: 34mA, typical
- Dimension: 38.4mm x 14mm (without MMCX connector)

3. Pin Configuration

3.1. Pin Assignment

Top view of a LRF020 Module and its pin allocation map are shown in Figures 1 and 2 respectively.

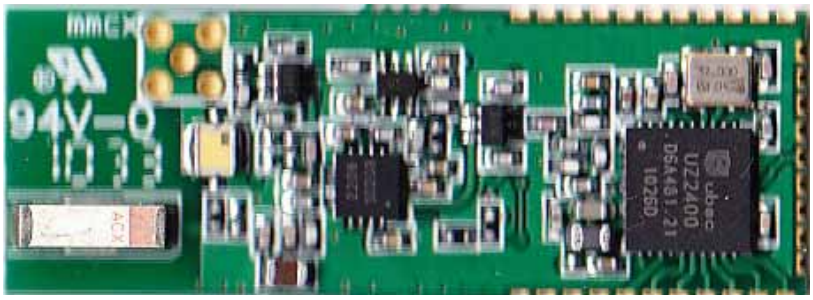

Figure 1. Top View of LRF020 Module without MMCX

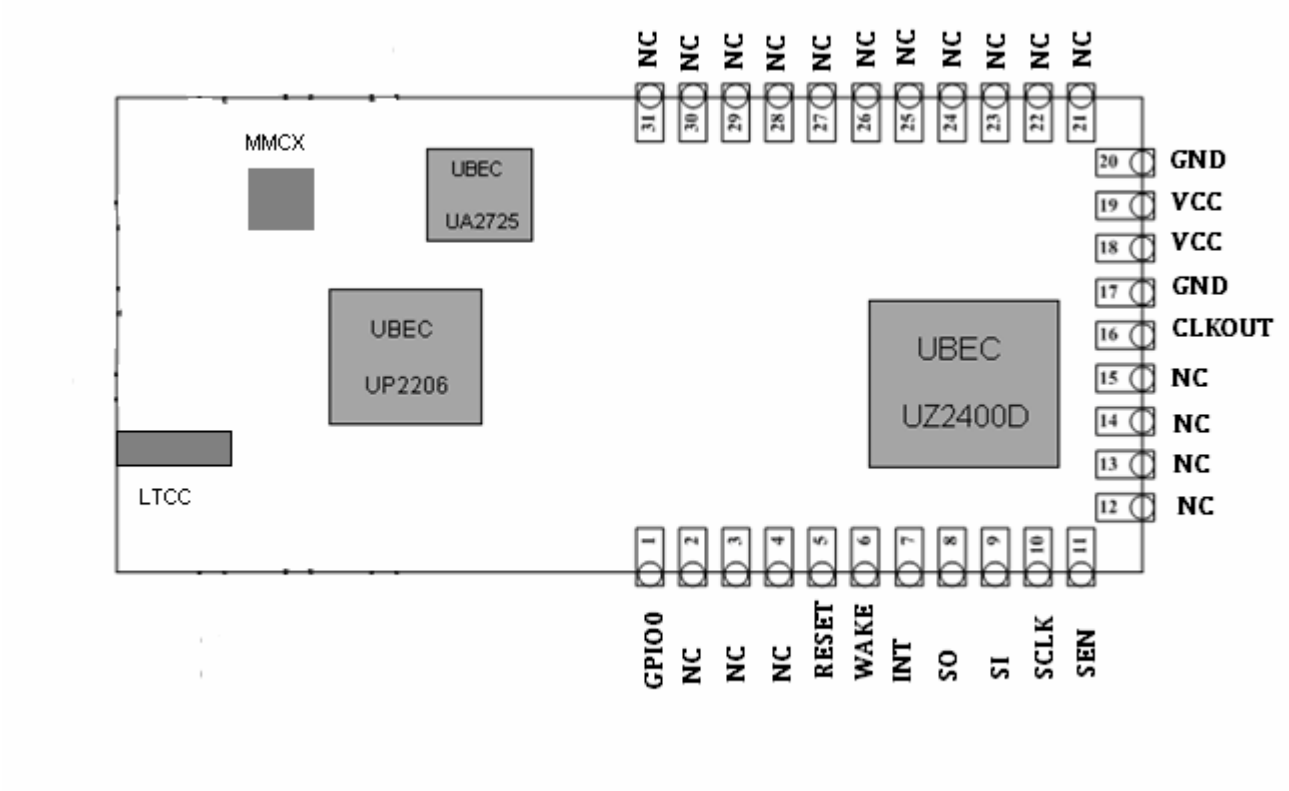

Figure 2. Pin Allocation

3.2. Pin Description

Pin type abbreviation: A = Analog, D = Digital, I = Input, O = Output, P = Power, G = Ground

Pin Number	Pin Name	Type	Description
1	GPIO0	DIO	General purpose digital I/O, also used as an external PA enable
2	NC		No connection
3	NC		No connection
4	NC		No connection
5	RESETN	DI	Global hardware reset pin, active low
6	WAKE	DI	External wake up trigger, active high / low can be programmable.
7	INT	DO	Interrupt pin to microprocessor : Level trigger, Hi / Low programmable
8	SO	DO	Serial interface data output from UZ2400 or I2C clock
9	SI	DIO	Serial interface data input to UZ2400 or I2C data in/out
10	SCLK	DI	Serial interface clock
11	SEN	DI	Serial interface enable
12	NC		No connection
13	NC		No connection
14	NC		No connection
15	NC		No connection
16	CLKOUT	DO	32 / 16 / 8 / 4 / 2 / 1 MHz clock output
17	GND	G	Ground
18	VCC	P	Power Supply
19	VCC	P	Power Supply
20	GND	G	Ground
21~31	NC		No connection

Table 1. Pin Assignment

4. Electrical Specifications

Test conditions: T_A = 25°C, VDD = 3.3 V, ($P_{out,UZ2400D}$=-10dBm)

ITEM	Condition	Specification			Unit
		Min.	Typ.	Max.	
Frequency		2405		2480	MHz
Supply voltage		3.0	3.3	3.6	V
TX Current consumption	(P_{out} =18 dBm)		210		mA
RX Current consumption			34		mA
TX Output power	P_{out}(UZ2400)=-10dBm		18		dBm
TX EVM	P_{out}(UZ2400)=-10dBm		14		%
RX sensitivity	PER<=1% O-QPSk 250kbps		-100		dBm
Communication Range	Throughput >120kbps at 250kbps data rate, LOS		1000		m

Table 2. Electrical Specifications

For detailed electrical characteristics of the UZ2400D chip, please refer to UZ2400D datasheet.

4.1. TX Output Power

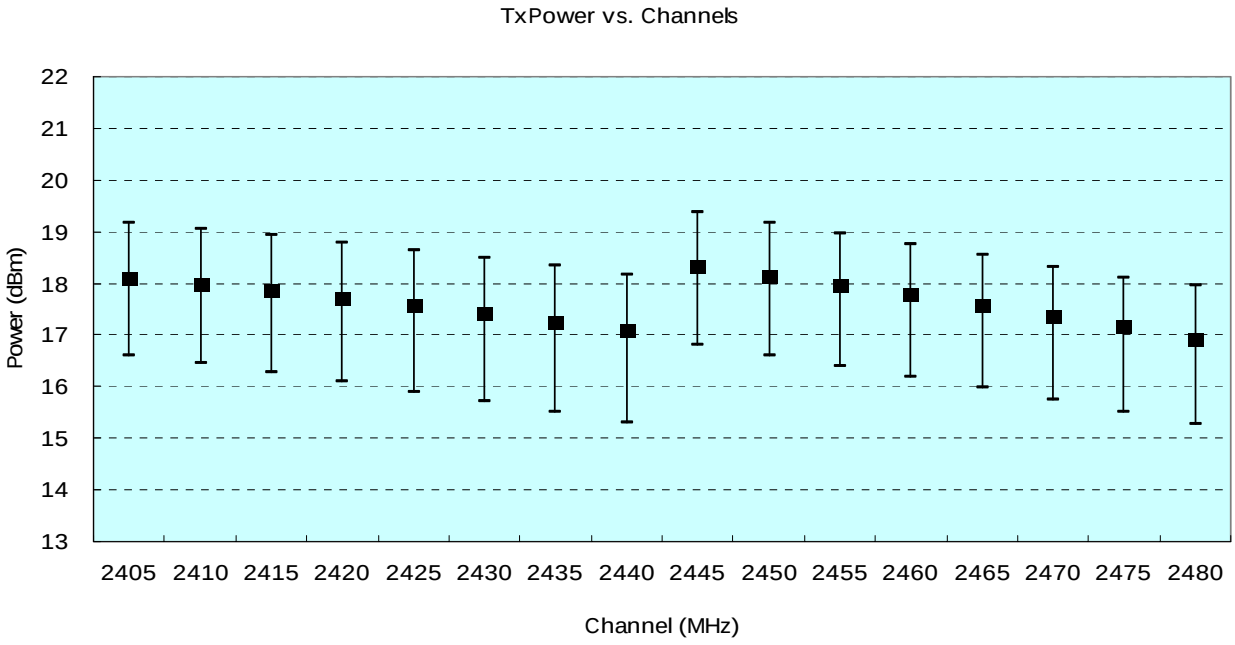

Figure 3. Typical TX Output Power

*Note. Set LREG0x274=0xc6 between channel 2445MHz to 2480MHz.

4.2. TX EVM

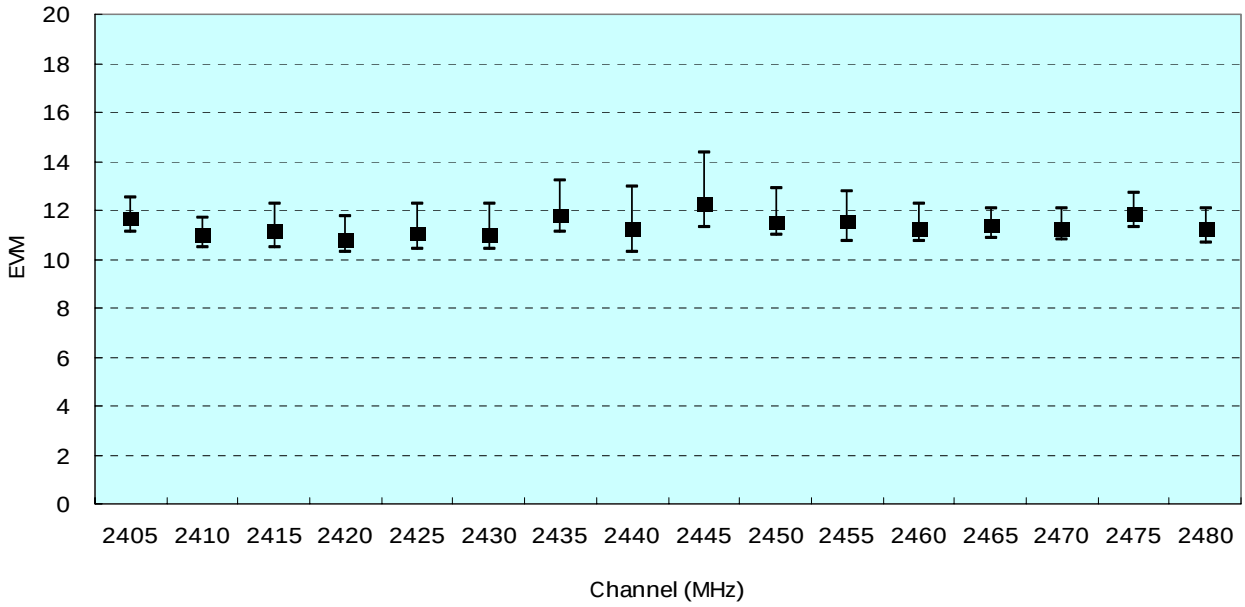

Figure 4. Typical TX EVM

4.3. RX Sensitivity

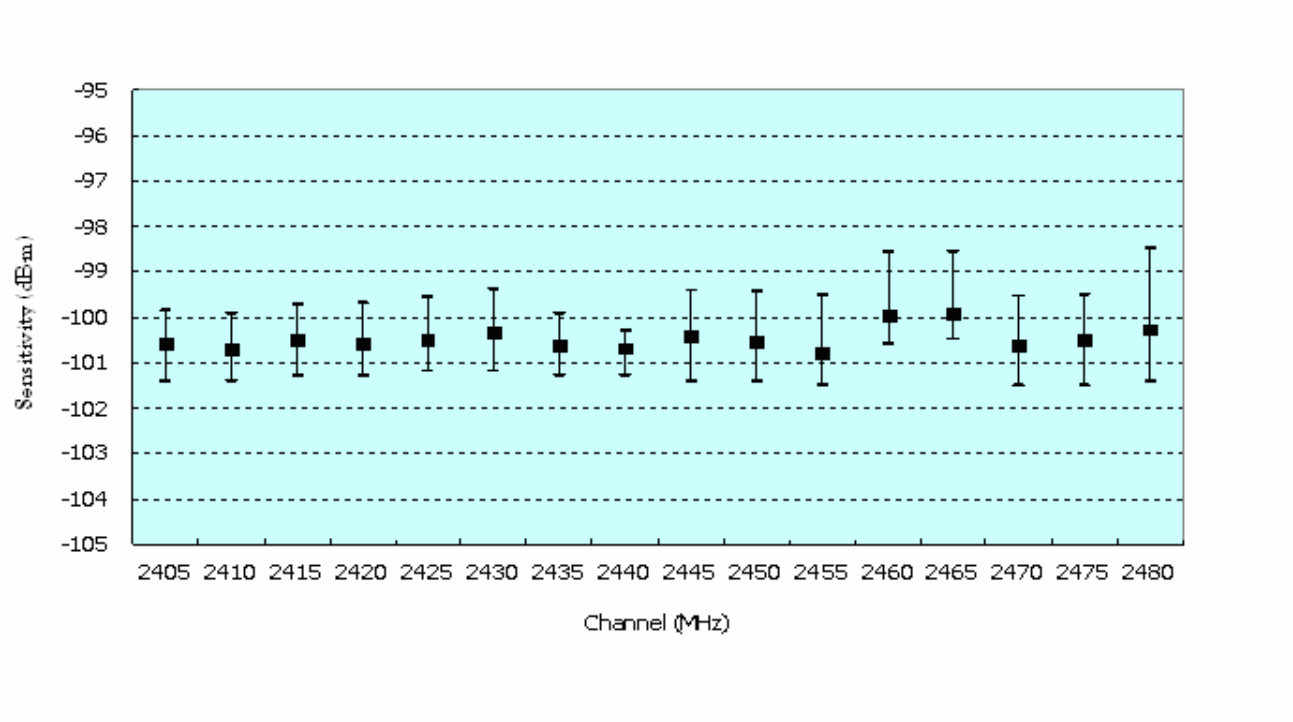

Figure 5. Typical RX Sensitivity

5. Register Initial Settings

The procedure to configure the initial settings is described as below.

Sep 1. Initialization

Refer to UZ2400D datasheet section 4.3.1 to initialize this module.

Step 2. Set Channel

The module operates in the 2.4 GHz ISM unlicensed band. The operating frequency is divided into 16 channels. RFCTL0 (LREG0x200) should be configured for the selected channel.

Address mode	Address	Register Name	Descriptions	Setting Value(hex)	Note	
					Channel	Frequency
LREG	0x200	RFCTL0	Set RF operation channel	03	11	2405 MHz
				13	12	2410 MHz
				23	13	2415 MHz
				33	14	2420 MHz
				43	15	2425 MHz
				53	16	2430 MHz
				63	17	2435 MHz
				73	18	2440 MHz
				83	19	2445 MHz
				93	20	2450 MHz
				A3	21	2455 MHz
				B3	22	2460 MHz
				C3	23	2465 MHz
				D3	24	2470 MHz
				E3	25	2475 MHz
				F3	26	2480 MHz

Step 3. Reset

After the operation channel is set, RF state machine should be reset by setting RFCTL (SREG0x36) to “0x04” and then setting RFCTL(SREG0x36) to “0x00”. After reset, 192us delay is required for the VCO calibration to calibrate the PLL block to the correct frequency.

Address mode	Address	Register Name	Descriptions	Setting Value(hex)
SREG	0x36	RFCTL	Reset RF state machine	0x04
SREG	0x36	RFCTL	Reset RF state machine	0x00

Step 4. PA/LNA Control

Address mode	Address	Register Name	Descriptions	Setting Value(hex)
LREG	0x22F	TESTMODE	GPIO0, GPIO1, GPIO2 are configured to control external PA, LNA or switch	0x29
LREG	0x203	RFCTL3	RF optimized control for LRF020	0xF8
LREG	0x253	RFCTL53	RF optimized control for LRF020	0x0B
LREG	0x274	RFCTL74	RF optimized control for LRF020	0xA6

After finishing all the above four steps, a basic initialization procedure is completed. This configuration procedure should be valid for most of the applications.

*Note. LREG0x203, 0x253, 0x274 control the PA gain. Refer to Appendix A.

6. Mechanical Dimension

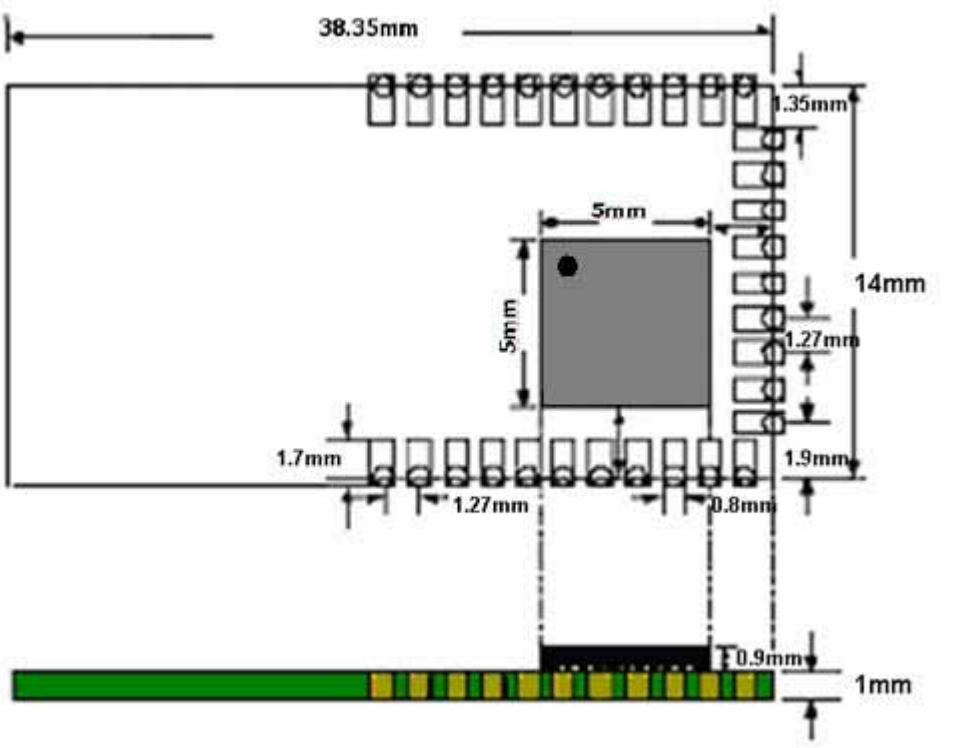

Figure 12. Dimensions of LRF020 Module

Appendix A. TX Power Configuration

If the TX power is inadequate for the initial register settings, user can set the PA gain using Table A-1 where different output power offsets are listed.

Tx Output Power Register Control			
LREG0x203<7:3>	**LREG0x253<3:0>**	**LREG0x274<7:0>**	**Tx Output Power offset (dB)**
0xF8	0x0B	0xC6	+2
	0x0B	0xB6	+1
	0x0B	0xA6	0 (initial setting)
	0x0D	0x96	-1
	0x09	0x96	-2
	0x0F	0x8A	-3
	0x0C	0x8A	-4
	0x0A	0x8A	-5
	0x08	0x8A	-6

Table A-1. Gain Table of LRF020

Revision History

Revision	Date	Description of Change
0.0	2010/7/26	Initial release.

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