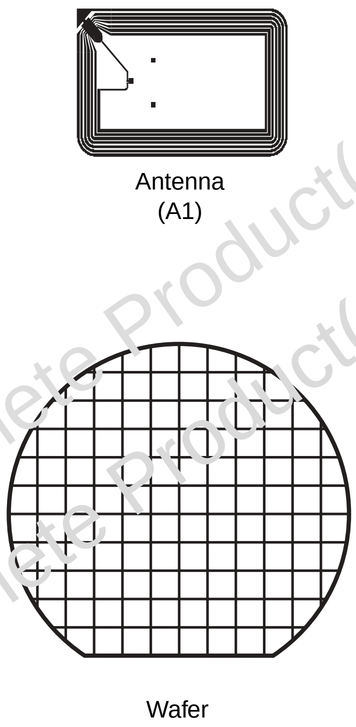
LRI512

ISO 15693 standard compliant, 13.56 MHz, 512 bit, high-endurance EEPROM TAG IC with EAS

Not For New Design

Features

- ISO 15693 standard: fully compliant
- 13.56 MHz ±7 kHz carrier frequency
- To the LRI512:
  - 10% or 100% ASK modulation using:
  - 1/4 pulse position coding (26 Kbit/s)
  - 1/256 pulse position coding (1.6 Kbit/s)
- From the LRI512:
  - Load modulation using Manchester coding with 423 kHz and 484 kHz subcarrier in Fast data rate (26 Kbit/s) and Low data rate (6.6 Kbit/s)
- Internal tuning capacitor
- 512 bit EEPROM with Block Lock feature
- 64-bit unique identifier (UID)
- EAS (electronic article surveillance) features
- READ block and WRITE block (32 bit blocks)
- 5 ms programming time (typical)
- More than 100 000 Erase/Write cycles
- More than 40 year data retention
- Packages
  - ECOPACK® (RoHS compliant)



This is information on a product still in production but not recommended for new designs.

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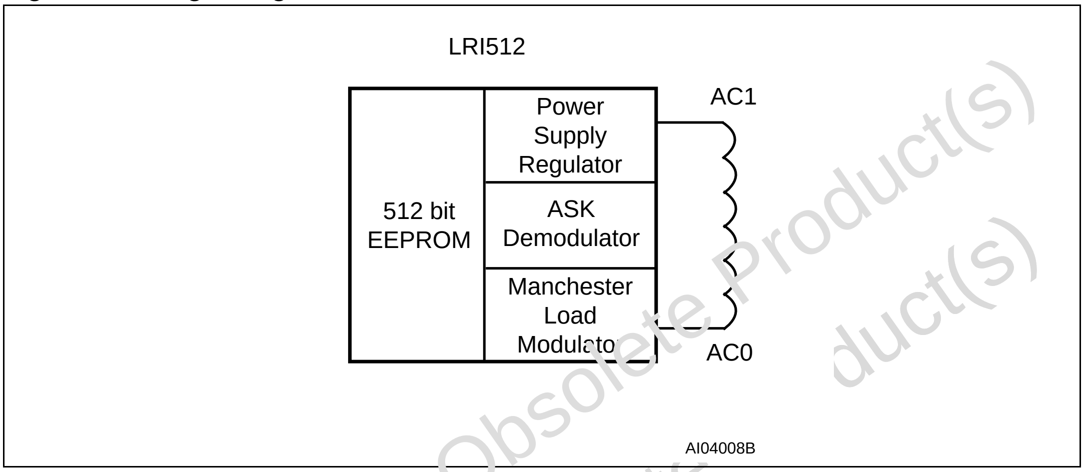
1 Description

The LRI512 is a contactless memory, powered by an externally transmitted radio wave. It is fully compliant with the ISO15693 recommendation for radio-frequency power and signal interface.

The LRI512 contains 512 bit of electrically erasable programmable memory (EEPROM). The memory is organized as 16 blocks of 32 bits.

Figure 1. Logic diagram



The LRI512 is accessed by modulating the 13.56 MHz carrier frequency. Incoming data are demodulated from the received signal amplitude modulation (ASK, Amplitude Shift Keying). The received ASK wave is 10% or 100% modulated (amplitude modulation). The Data transfer rate is 1.6 Kbit/s using the 1/256 pulse coding mode and 26 Kbit/s using the 1/4 pulse coding modes.

Outgoing data are generated by antenna load variation, using the Manchester coding, using one or two subcarrier frequencies at 423 kHz and 484 kHz. The Data transfer rate is 6.6 Kbit/s, in the low data rate mode, and 26 Kbit/s, in the fast data rate mode.

Table 1. Signal names

Signal name	Function
AC1	Antenna coil
AC0	Antenna coil

1.1 Memory mapping

The LRI512 is divided in 16 blocks of 32 bits. Each block can be individually Write Protected using a specific Lock command.

Table 2. LRI512 memory map

Address	0 7	8 15	16 23	24 31
0	User area			
1	User area			
2	User area			
3	User area			
4	User area			
5	User area			
6	User area			
7	User area			
8	User area			
9	User area			
10	User area			
11	User area			
12	User area			
13	User area			
14	User area			
15	User area			
	UID 0	UID 1	UID 2	UID 3
	UID 4	UID 5	UID 6	UID 7
	AFI			

The user area consists of blocks that are always accessible in Read. Write commands are possible if the addressed block is not locked. During a Write, the 32 bits of the block are replaced by the new 32-bit value.

The LRI512 also has a 64-bit block that is used to store the 64-bit unique identifier (UID). This UID is compliant to the ISO 15963 description, and its value is used during the anticollision sequence (Inventory). This block is not accessible by the user, and the value is written by ST on the production line.

The LRI512 also has an AFI register in which the application family identifier (AFI) is stored, for use in the anticollision algorithm.

1.2 Commands

The LRI512 supports the following commands:

- ***Inventory***: used to perform the anticollision sequence.
- ***Stay Quiet:*** to put the LRI512 in quiet mode. The LRI512 is then deselected and does not respond to any command.
- ***Select:*** used to select the LRI512. After this command, the LRI512 processes all READ/WRITE commands with the Select_Flag set.
- ***Reset to Ready:*** to put the LRI512 in the ready state.
- ***Read Block:*** to output the 32 bits of the selected block and its locking status.
- ***Write Block:*** to write the 32-bit value in the selected block, provided that it is not locked.
- ***Lock Block:*** to lock the selected block. After this command, the block cannot be modified.
- ***Write AFI:*** to write the 8-bit value in the AFI register, provided that it is not locked.
- ***Lock AFI:*** to lock the AFI register.
- ***Activate EAS:*** to set the non volatile EAS bit. When the EAS bit is set, the LRI512 answers to the Pool EAS command.
- ***Deactivate EAS:*** to reset the non volatile EAS bit, so that the LRI512 no longer answers to the Pool EAS command.
- ***Pool EAS***: used to request all LRI512s in the Reader field to generate the EAS signal, provided that their EAS bit is set.

1.3 Initial dialogue for vicinity cards

The dialogue between the vicinity coupling device (VCD) and the vicinity integrated circuit card (LRI512) is conducted through the following consecutive operations:

- activation of the LRI512 by the RF operating field of the VCD.
- transmission of a command by the VCD.
- transmission of a response by the LRI512.

These operations use the RF power transfer and communication signal interface specified in the following paragraphs. This technique is called reader talk first (RTF).

1.4 Power transfer

Power transfer to the LRI512 is accomplished by radio frequency at 13.56 MHz via coupling antennas in the LRI512 and in the VCD. The RF operating field of the VCD is transformed on the LRI512 antenna as an AC voltage which is re-dressed, filtered and internally regulated. The amplitude modulation (ASK) on this received signal is demodulated by the ASK demodulator.

1.5 Frequency

The ISO 15693 standard defines the carrier frequency (f_C) of the operating field to be 13.56 MHz ± 7 kHz.

1.6 Operating field

The LRI512 operates continuously between H_{min} and H_{max}.

- The minimum operating field is H_{min} and has a value of 150 mA/m rms.
- The maximum operating field is H_{max} and has a value of 5 A/m rms.

A VCD must generate a field of at least H_{min} and not exceeding H_{max} in the operating volume.

2 Communication signal from VCD to LRI512

Since the LRI512 is fully compliant with the ISO 15693 recommendation, the descriptions and illustrations that follow are very heavily based on those of the ISO/IEC documents: ISO/IEC 15693-2:2000(E) and ISO/IEC 15693-3:2001(E). This has been done with the kind permission of the ISO Copyright Office.

Communications between the VCD and the LRI512 takes place using the modulation principle of ASK (amplitude modulation). Two modulation indices are used, 10% and 100%. The LRI512 decodes both. The VCD determines which index is used.

The modulation index is defined as [a – b]/[a + b] where a and b are the peak and minimum signal amplitude, respectively, of the carrier frequency.

Depending of the choice made by the VCD, a “pause” will be created as described in *Figure 2* and *Figure 3*.

The LRI512 is operational for any degree of modulation index from between 10% and 30%.

Figure 2. 100% modulation waveform

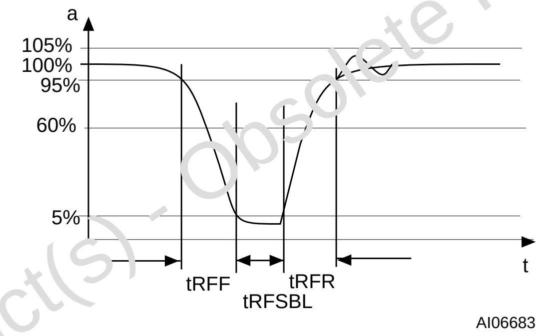
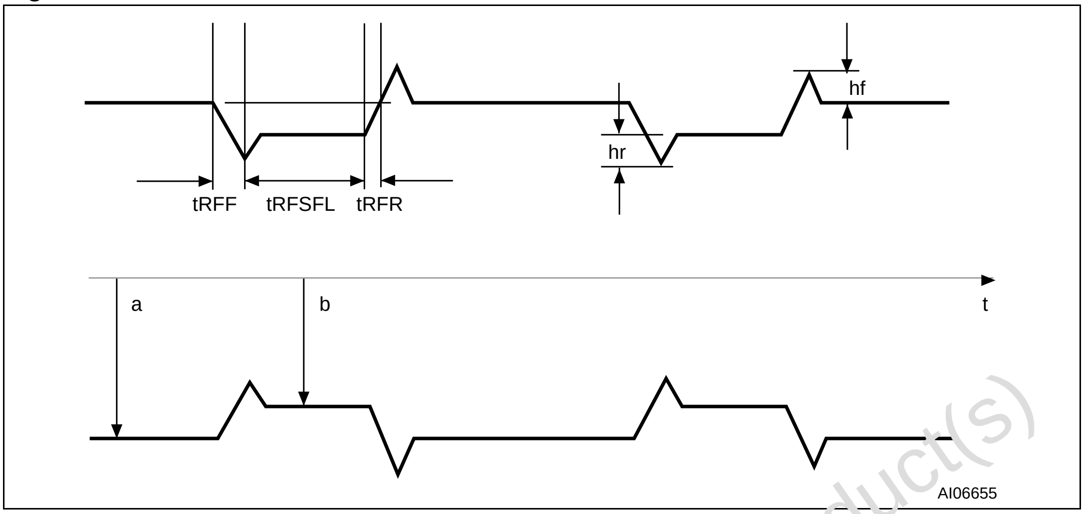


Table 3. 10% modulation parameters

Parameter	Value	
hr	0.1 × (a – b)	max
hf	0.1 × (a – b)	max

Figure 3. 10% modulation waveform



3 Data rate and data coding

The data coding implemented in the LRI512 uses pulse position modulation. Both data coding modes that are described in the ISO15693 are supported by the LRI512. The selection is made by the VCD and indicated to the LRI512 within the Start of Frame (SOF).

3.1 Data coding mode: 1 out of 256

The value of one single byte is represented by the position of one pause. The position of the pause on 1 of 256 successive time periods of 18.88 µs ($256/f_C$), determines the value of the byte. In this case the transmission of one byte takes 4.833 ms and the resulting data rate is 1.65 Kbit/s ($f_C/8192$).

Figure 4 illustrates this pulse position modulation technique. In this figure, data E1h (225d) is sent by the VCD to the LRI512.

The pause shall occur during the second half of the position of the time period that determines the value, as shown in *Figure 5*.

A pause during the first period transmit the data value 00h. A pause during the last period transmits the data value FFh (255d).

Figure 4. 1 out of 256 coding mode

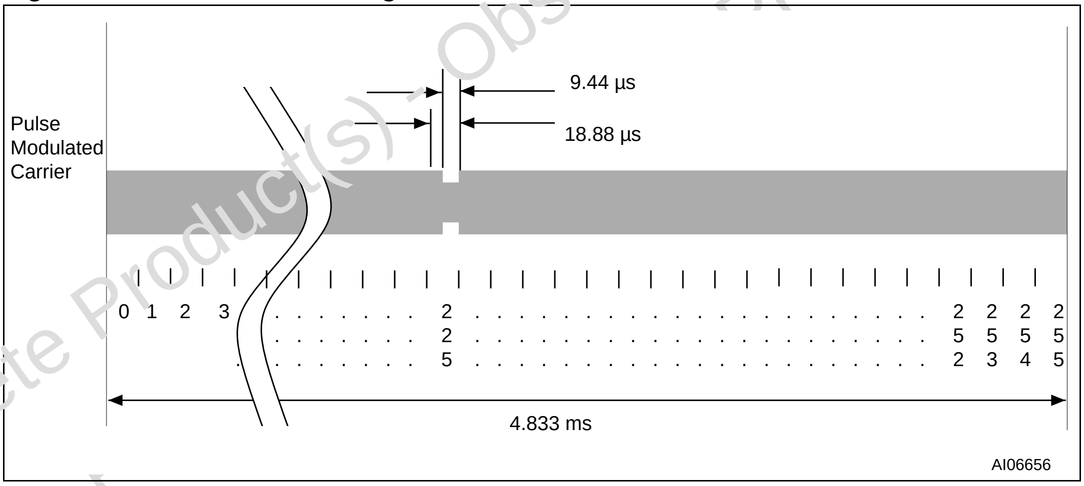
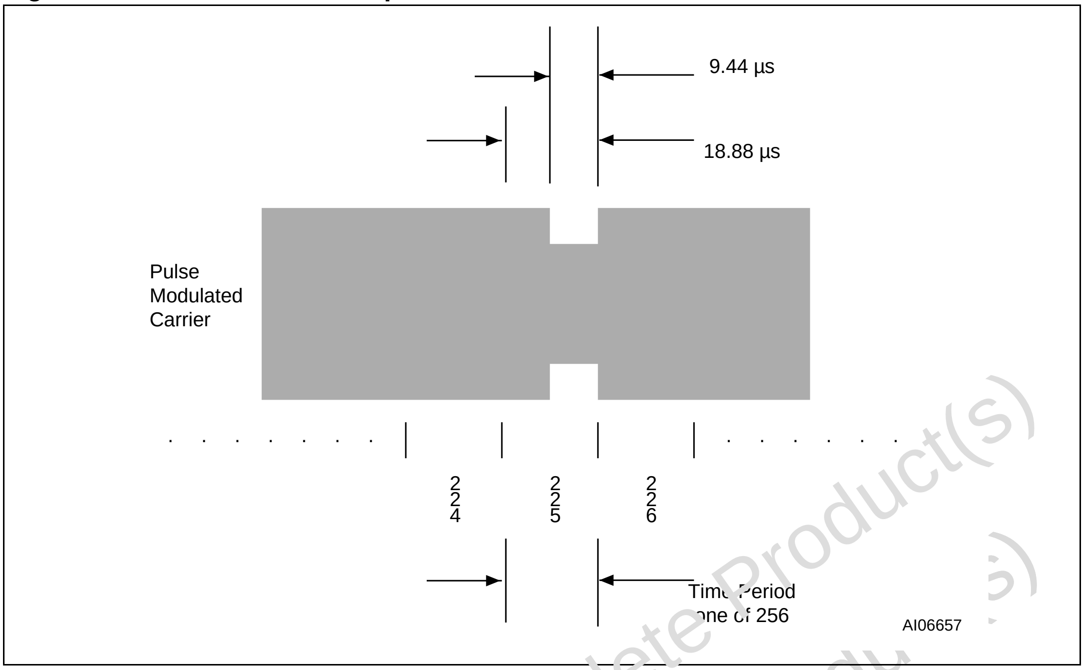


Figure 5. Detail of one time period

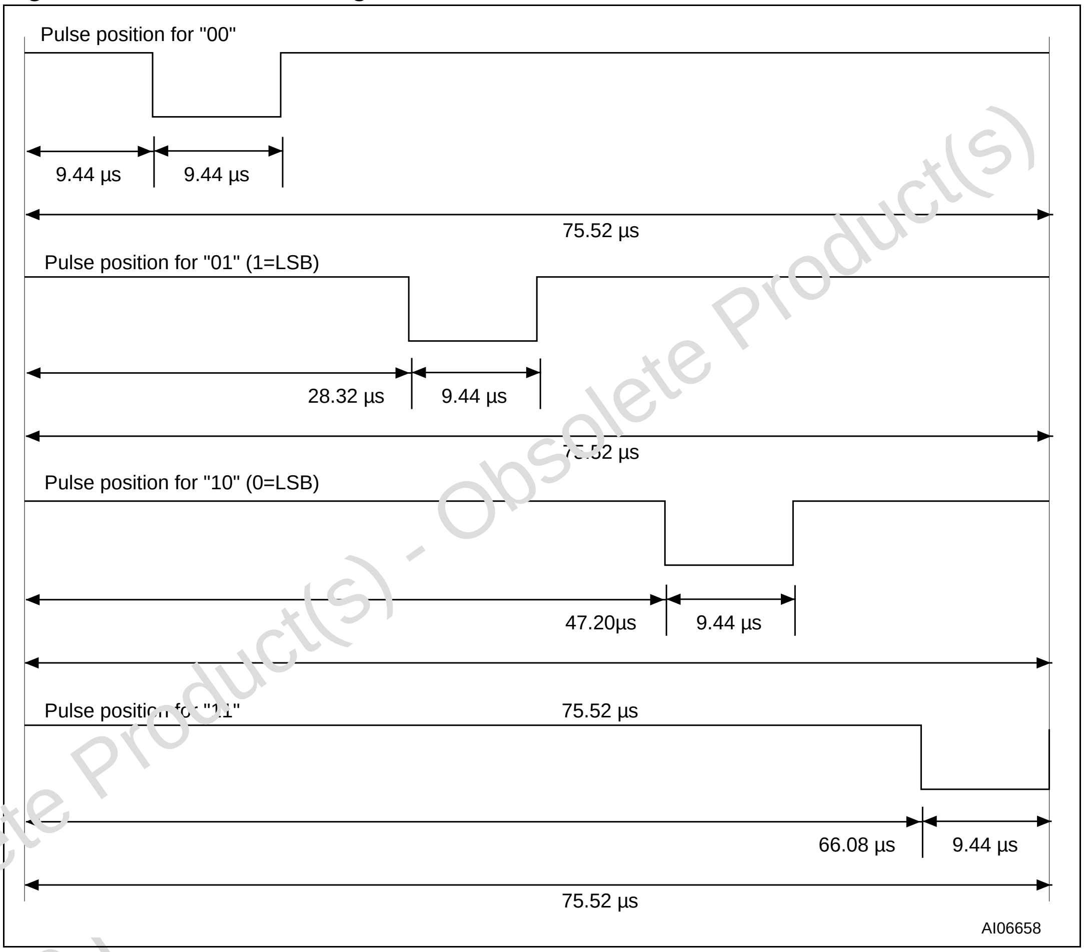


3.2 Data coding mode: 1 out of 4

The value of 2 bits is represented by the position of one pause. The position of the pause on 1 of 4 successive time periods of 18.88 µs ($256/f_C$), determines the value of the 2 bits. Four successive pairs of bits form a byte, where the least significant pair of bits is transmitted first.

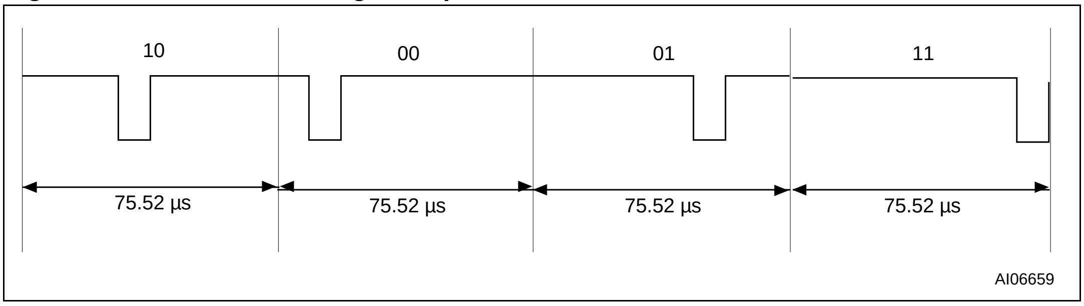
In this case the transmission of one byte takes 302.08 µs and the resulting data rate is 26.48 Kbit/s ($f_C/512$). *Figure 6* illustrates the 1 out of 4 pulse position technique and coding.

Figure 6. 1 out of 4 coding mode



For example *Figure 7* shows the transmission of E1h (225d, 1110 0001b) by the VCD.

Figure 7. 1 out of 4 coding example



3.3 VCD to LRI512 frames

Frames are delimited by a Start of Frame (SOF) and an End of Frame (EOF) and are implemented using code violation. Unused options are reserved for future use.

The LRI512 is ready to receive a new command frame from the VCD after a delay of t_2 after having sent a response frame to the VCD (as specified in *Table 54*).

The LRI512 generates a Power-on delay of t_{MINCD} after being activated by the powering field (as specified in *Table 54*). After this delay, the LRI512 is ready to receive command frames from the VCD.

3.4 Start of frame (SOF)

The SOF defines the data coding mode the VCD is to use for the following command frame. The SOF sequence described in *Figure 8* selects the 1 out of 256 data coding mode. The SOF sequence described in *Figure 9* selects the 1 out of 4 data coding mode. The EOF sequence for either coding mode is described in *Figure 10*.

Figure 8. SOF to select 1 out of 256 data coding mode

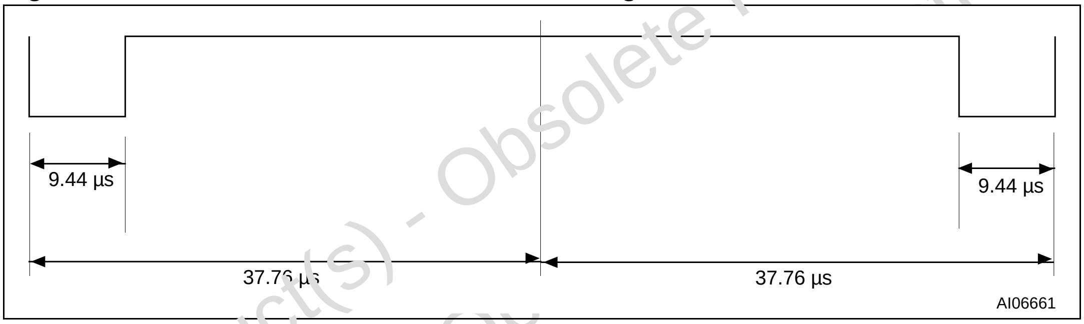


Figure 9. SOF to select 1 out of 4 data coding mode

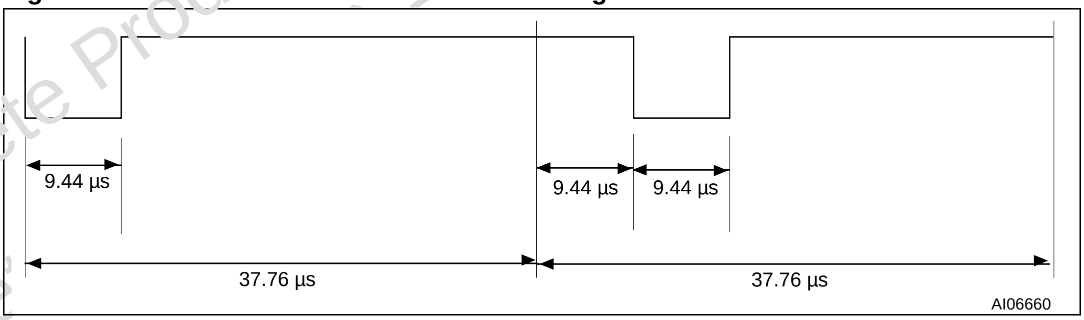
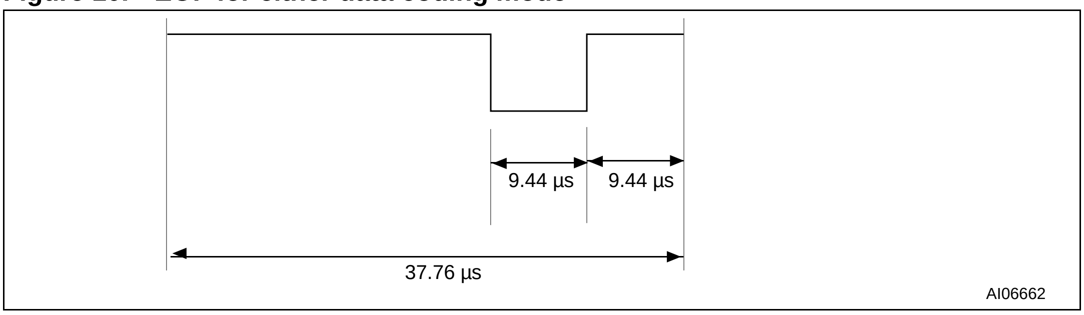


Figure 10. EOF for either data coding mode



4 Communications signal from LRI512 to VCD

For some parameters several modes have been defined in order to allow for use in different noise environments and application requirements.

4.1 Load modulation

The LRI512 is capable of communication to the VCD via an inductive coupling area in which the carrier is loaded to generate a subcarrier with frequency f_S. The subcarrier is generated by switching in a load in the LRI512.

4.2 Subcarrier

The LRI512 supports the one subcarrier and two subcarriers response formats. These formats are selected by the VCD using the first bit in the protocol header.

When one subcarrier is used, the frequency f_S1 of the subcarrier load modulation is 423.75kHz (f_C/32).

When two subcarriers are used, the frequency f_S1 is 423.75 kHz (f_C/32), and the frequency f_S2 is 484.28 kHz (f_C/28). When using the two subcarriers mode, the LRI512 generates a continuous phase relationship between f_S1 and f_S2.

4.3 Data rates

The LRI512 can respond using the low or the high data rate format. The selection of the data rate is made by the VCD using the second bit in the protocol header.

Table 4 shows the different data rates the LRI512 can achieve using each combination.

Table 4. Response data rate

Data rate	One subcarrier	Two subcarriers
Low	6.62 Kbit/s (f_C/2048)	6.67 Kbit/s (f_C/2032)
High	26.48 Kbit/s (f_C/512)	26.69 Kbit/s (f_C/508)

5 Bit representation and coding

Data bits are encoded using Manchester coding, according to the following schemes.

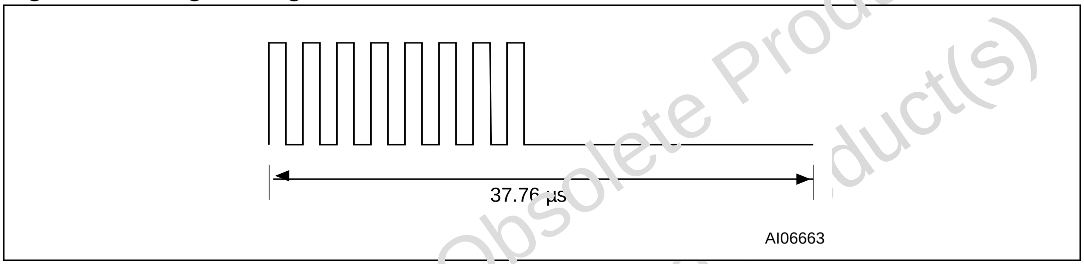
For the low data rate the same subcarrier frequency or frequencies are used, in this case the number of pulses shall be multiplied by 4 and all times will increase by this factor.

5.1 Bit coding using one subcarrier

5.1.1 High data rate

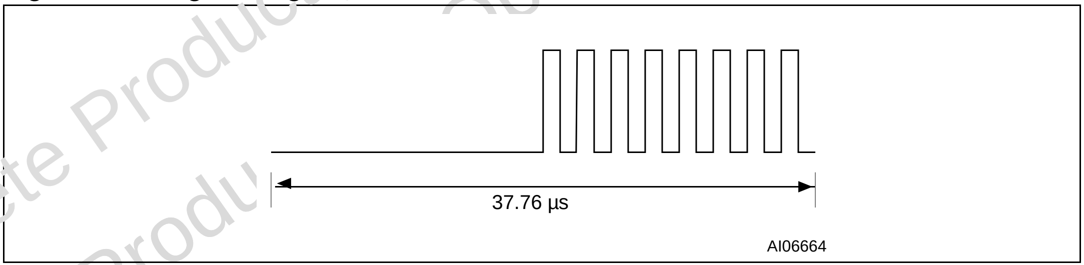
A logic 0 starts with 8 pulses of 423.75 kHz (f_C/32) followed by an unmodulated time of 18.88 µs as shown in *Figure 11*.

Figure 11. Logic 0, high data rate



A logic 1 starts with an unmodulated time of 18.88 µs followed by 8 pulses of 423.75 kHz (f_C/32) as shown in *Figure 12*.

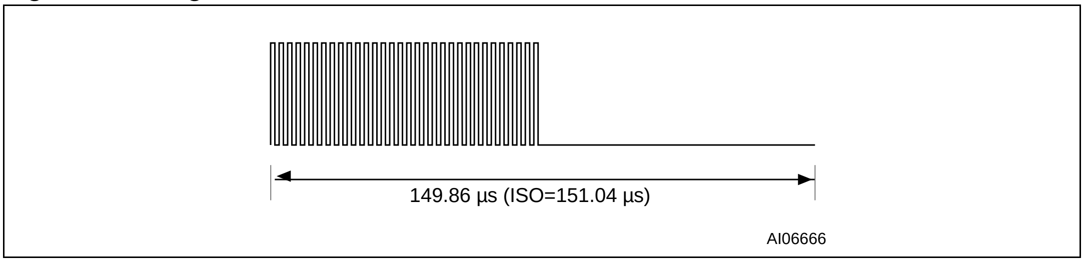
Figure 12. Logic 1, high data rate



5.1.2 Low data rate

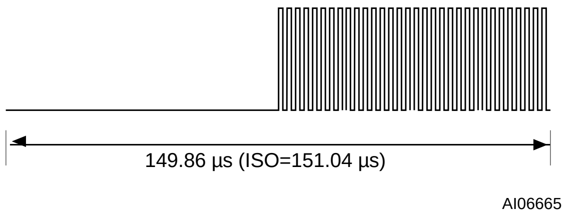
A logic 0 starts with 32 pulses of 423.75 kHz (f_C/32) followed by an unmodulated time of 75.52 µs as shown in *Figure 13*.

Figure 13. Logic 0, low data rate



A logic 1 starts with an unmodulated time of 75.52 µs followed by 32 pulses of 423.75 kHz (f_C/32) as shown in *Figure 14*.

Figure 14. Logic 1, low data rate

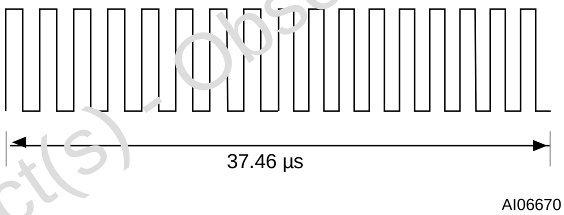


5.2 Bit coding using two subcarriers

5.2.1 High data rate

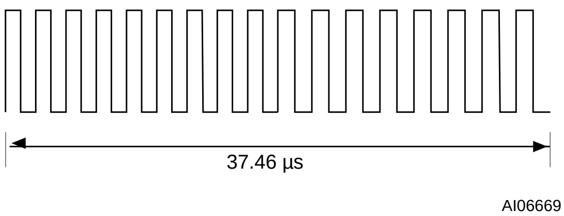
A logic 0 starts with 8 pulses of 423.75 kHz (f_C/32) followed by 9 pulses of 484.28 kHz (f_C/28) as shown in *Figure 15*.

Figure 15. Logic 0, high data rate



A logic 1 starts with 9 pulses of 484.28 kHz (f_C/28) followed by 8 pulses of 423.75 kHz (f_C/32) as shown in *Figure 16*.

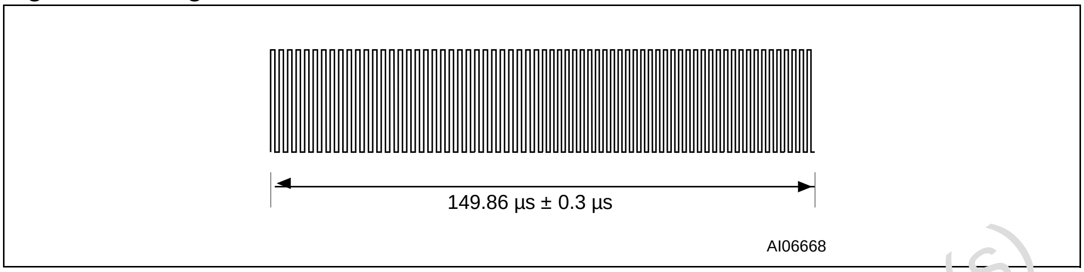
Figure 16. Logic 1, high data rate



5.2.2 Low data rate

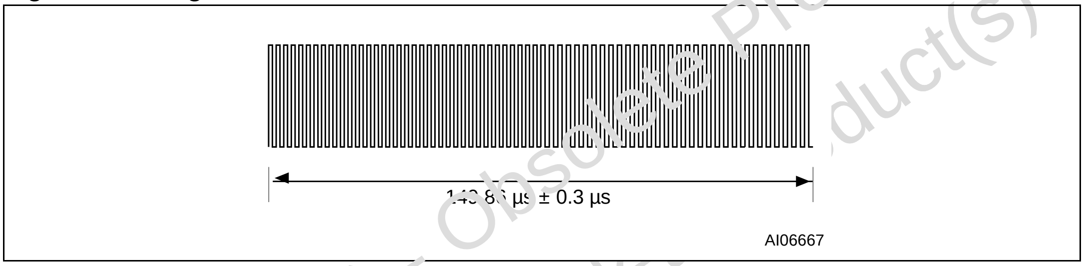
A logic 0 starts with 32 pulses of 423.75 kHz (f_C/32) followed by 36 pulses of 484.28 kHz (f_C/28) as shown in *Figure 17*.

Figure 17. Logic 0, low data rate



A logic 1 starts with 36 pulses of 484.28 kHz (f_C/28) followed by 32 pulses of 423.75 kHz (f_C/32) as shown in *Figure 18*.

Figure 18. Logic 1, low data rate



6 LRI512 to VCD frames

Frames are delimited by an SOF and EOF and are implemented using code violation. Unused options are reserved for future use.

For the low data rate, the same subcarrier frequency or frequencies are used. In this case the number of pulses shall be multiplied by 4.

The VCD is ready to receive a response frame from the LRI512 within less than t_1 after having sent a command frame (as specified in *Table 54*).

6.1 SOF when using one subcarrier

6.1.1 High data rate

SOF comprises 3 parts: (see *Figure 19*)

- an unmodulated time of 56.64 µs,
- 24 pulses of 423.75 kHz (f_c/32),
- a logic 1 which starts with an unmodulated time of 18.88 µs followed by 8 pulses of 423.75 kHz.

6.1.2 Low data rate

SOF comprises 3 parts: (see *Figure 20*)

- an unmodulated time of 226.56 µs,
- 96 pulses of 423.75 kHz (f_c/32),
- a logic 1 which starts with an unmodulated time of 75.52 µs followed by 32 pulses of 423.75 kHz.

Figure 19. Start of frame, high data rate, one subcarrier

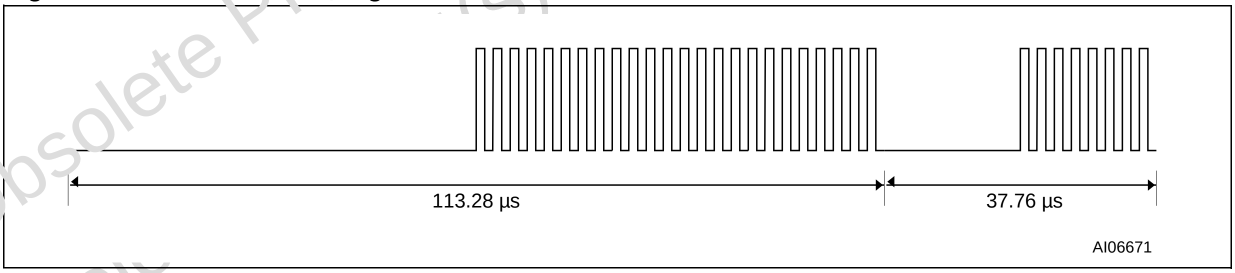
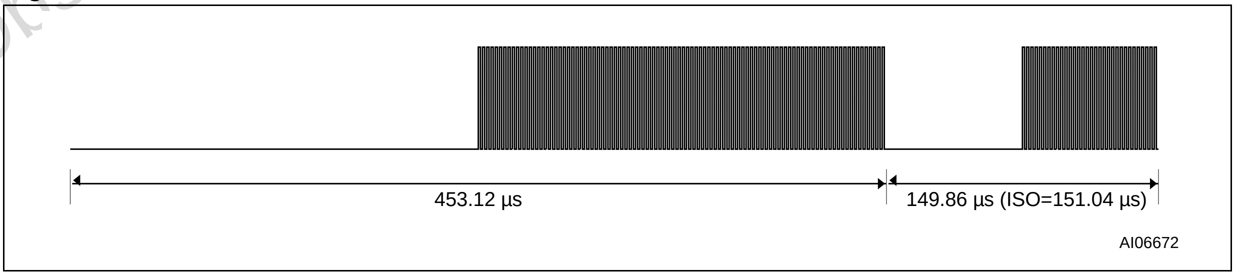


Figure 20. Start of frame, low data rate, one subcarrier



6.2 SOF when using two subcarriers

6.2.1 High data rate

SOF comprises 3 parts: (see *Figure 21*)

- 27 pulses of 484.28 kHz ($f_c/28$),
- 24 pulses of 423.75 kHz ($f_c/32$),
- a logic 1 which starts with 9 pulses of 484.28 kHz followed by 8 pulses of 423.75 kHz.

6.2.2 Low data rate

SOF comprises 3 parts: (see *Figure 22*)

- 108 pulses of 484.28 kHz ($f_c/28$),
- 96 pulses of 423.75 kHz ($f_c/32$),
- a logic 1 which starts with 36 pulses of 484.28 kHz followed by 32 pulses of 423.75 kHz.

Figure 21. Start of frame, high data rate, two subcarriers

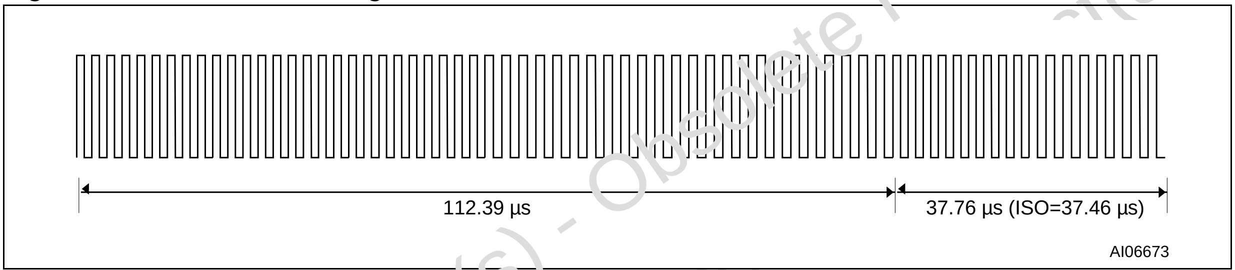
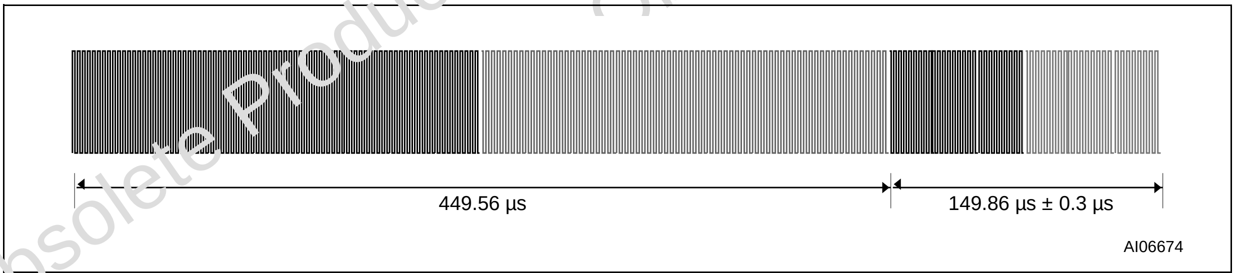


Figure 22. Start of frame, low data rate, two subcarriers



6.3 EOF when using one subcarrier

6.3.1 High data rate

EOF comprises 3 parts: (see *Figure 23*)

- a logic 0 which starts with 8 pulses of 423.75 kHz followed by an unmodulated time of 18.88 µs.
- 24 pulses of 423.75 kHz ($f_c/32$),
- an unmodulated time of 56.64 µs.

6.3.2 Low data rate

EOF comprises 3 parts: (see *Figure 24*)

- a logic 0 which starts with 32 pulses of 423.75 kHz followed by an unmodulated time of 75.52 µs.
- 96 pulses of 423.75 kHz (f_c/32),
- an unmodulated time of 226.56 µs.

Figure 23. End of frame, high data rate, one subcarrier

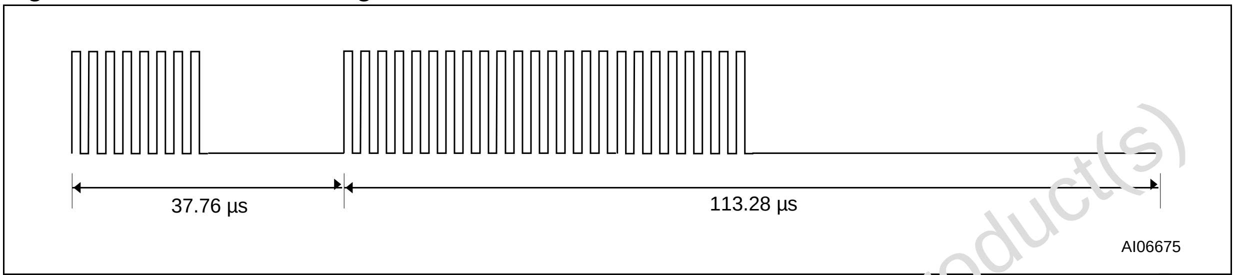
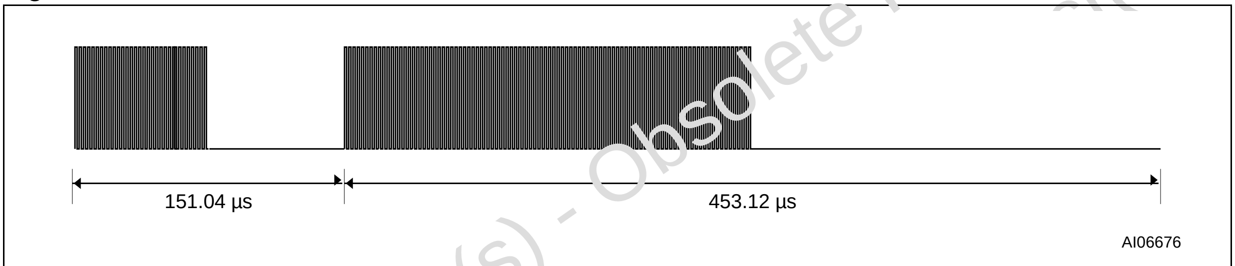


Figure 24. End of frame, low data rate, one subcarrier



6.4 EOF when using two subcarriers

6.4.1 High data rate

EOF comprises 3 parts: (see *Figure 25*)

- a logic 0 which starts with 8 pulses of 423.75 kHz followed by 9 pulses of 484.28 kHz,
- 24 pulses of 423.75 kHz (f_c/32),
- 27 pulses of 484.28 kHz (f_c/28).

6.4.2 Low data rate

EOF comprises 3 parts: (see *Figure 26*)

- a logic 0 which starts with 32 pulses of 423.75 kHz followed by 36 pulses of 484.28 kHz,
- 96 pulses of 423.75 kHz (f_c/32),
- 108 pulses of 484.28 kHz (f_c/28).

Figure 25. End of frame, high data rate, two subcarriers

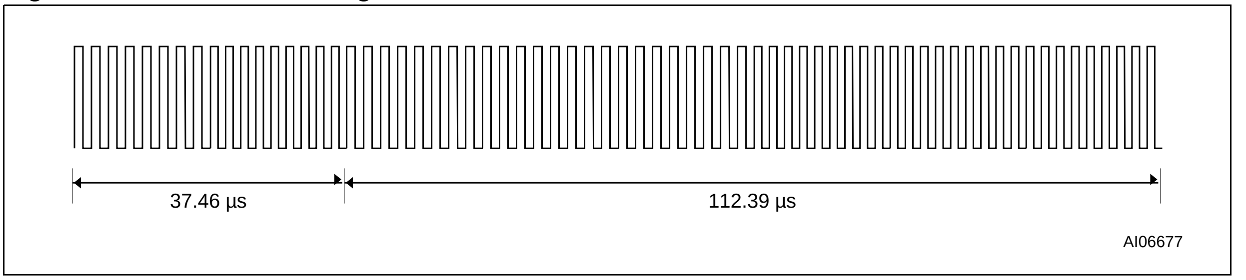
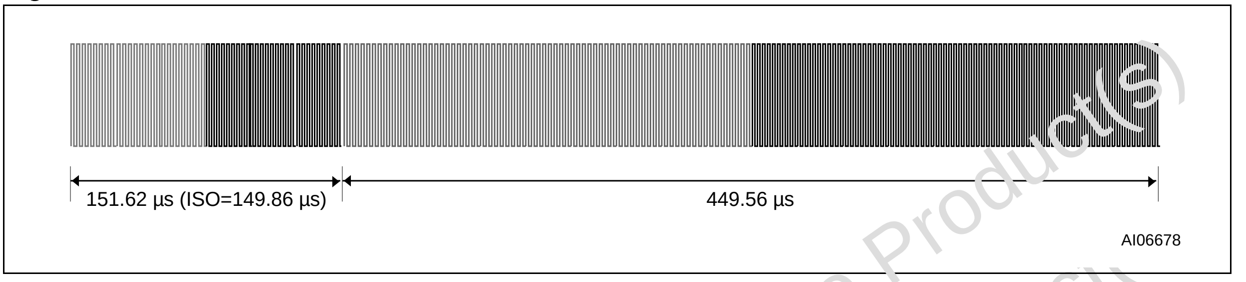


Figure 26. End of frame, low data rate, two subcarriers



7 Unique identifier (UID)

The LRI512s are uniquely identified by a 64-bit Unique Identifier (UID). This UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. The UID is a read only code, and comprises:

- The 8 MSB is E0h
- The IC Manufacturer code of ST 02h, on 8 bits (ISO/IEC 7816-6/AM1)
- A Unique Serial Number on 48 bits.

The UID is used for addressing each LRI512 uniquely and individually, during the anticollision loop and for one-to-one exchange between a VCD and a LRI512.

The UID format is shown below:

MSB **LSB**

63 56	55 48	47 0
E0h	02h	Unique serial number

8 Application family identifier (AFI)

The AFI (application family identifier) describes the type of application targeted by the VCD, and is used to extract from all the LRI512s present only the LRI512s meeting the required application criteria.

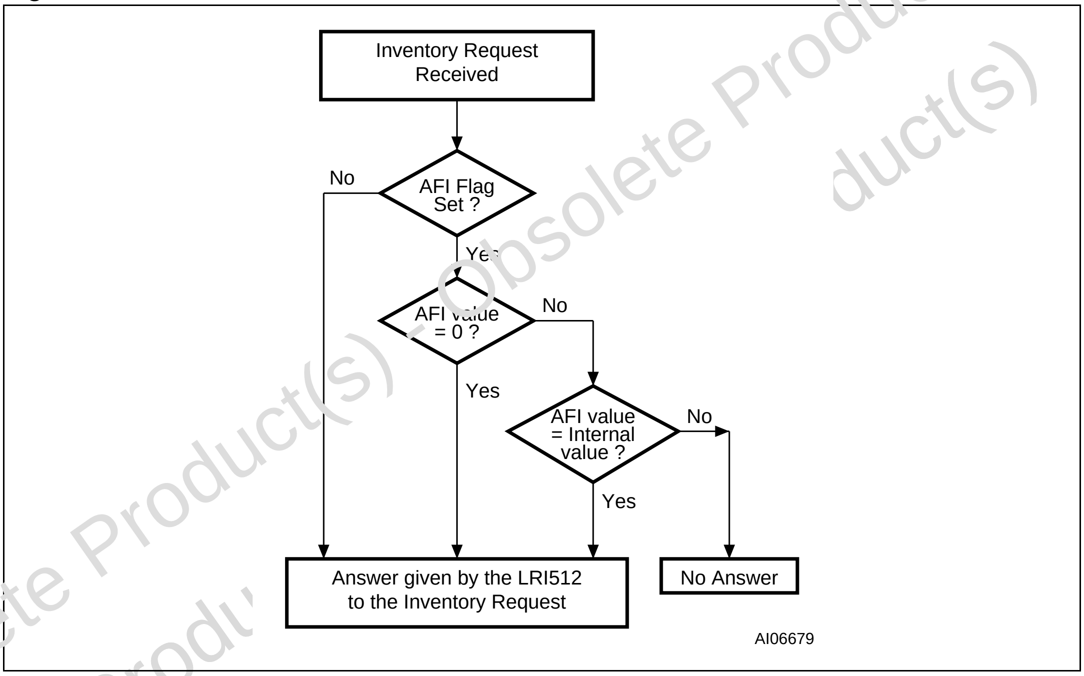
It is programmed by the LRI512 issuer in the AFI register. Once programmed and Locked, it cannot be modified.

The most significant nibble of AFI is used to code one specific or all application families.

The least significant nibble of AFI is used to code one specific or all application sub-families. Sub-family codes, other than 0, are proprietary.

(See ISO 15693-3 documentation)

Figure 27. LRI512 decision tree for AFI



9 CRC

The CRC used in the LRI512 is calculated as per the definition in ISO/IEC 13239.

The initial register content is all ones: FFFFh.

The 2-byte CRC is appended to each Request and each Response, within each frame, before the EOF. The CRC is calculated on all the bytes after the SOF up to the CRC field.

Upon reception of a Request from the VCD, the LRI512 verifies that the CRC value is valid. If it is invalid, it discards the frame, and does not answer the VCD.

Upon reception of a Response from the LRI512, it is recommended that the VCD verify that the CRC value is valid. If it is invalid, actions to be performed are left to the responsibility of the VCD designer.

The CRC is transmitted Least Significant Byte first. Each byte is transmitted Least Significant Bit first.

The CRC transmission rules are shown below:

LSByte		MSByte	
LSBit	MSBit	LSBit	MSBit
CRC 16 (8 bits)		CRC 16 (8 bits)	

10 LRI512 protocol description

The transmission protocol defines the mechanism to exchange instructions and data between the VCD and the LRI512, in both directions.

It is based on the concept of “VCD talks first”.

This means that any LRI512 does not start transmitting unless it has received and properly decoded an instruction sent by the VCD.

The protocol is based on an exchange of

- a request from the VCD to the LRI512
- a response from the LRI512 to the VCD

Each request and each response is contained in a frame. The frame delimiters (SOF, EOF) are described in the previous paragraphs.

Each request consists of

- Request SOF (see *Figure 8* and *Figure 9*)
- Flags
- A command code
- Parameters, depending on the command
- Application data
- 2-byte CRC
- Request EOF (see *Figure 10*)

Each Response consists of

- Answer SOF (see *Figure 19* to *Figure 22*)
- Flags
- Parameters, depending on the command
- Application data
- 2-byte CRC
- Answer EOF (see *Figure 23* to *Figure 26*)

The protocol is bit-oriented. The number of bits transmitted in a frame is a multiple of eight (8) – that is, an integer number of bytes.

A single-byte field is transmitted Least Significant Bit (LSBit) first.

A multiple-byte field is transmitted Least Significant Byte (LSByte) first, each byte is transmitted Least Significant Bit (LSBit) first.

The setting of the flags indicates the presence of the optional fields. When the flag is set (to one), the field is present. When the flag is reset (to zero), the field is absent.

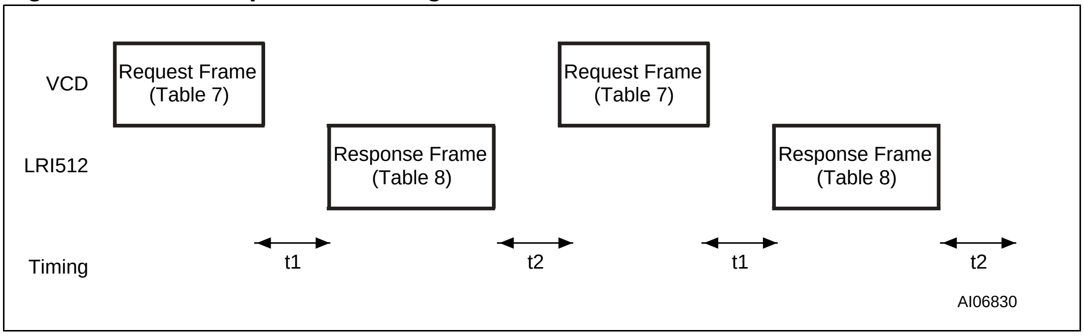
Table 5. VCD request frame format

Request SOF	Request Flags	Command Code	Parameters	Data	2 byte CRC	Request EOF

Table 6. LRI512 response frame format

Response SOF	Response Flags	Parameters	Data	2 byte CRC	Response EOF

Figure 28. LRI512 protocol timing



11 LRI512 states

A LRI512 can be in one of four states:

- Power-off
- Ready
- Quiet
- Selected

Transitions between these states are specified in *Figure 29* and *Table 7*.

11.1 Power-off state

The LRI512 is in the Power-off state when it does not receive enough energy from the VCD.

11.2 Ready state

The LRI512 is in the Ready state when it receives enough energy from the VCD. It shall answer any Request where the Select_Flag is not set.

11.3 Quiet state

When in the Quiet State, the LRI512 answers any Request other than an Inventory Request with the Address_Flag set.

11.4 Selected state

In the Selected State, the LRI512 answers to any Request in all modes:

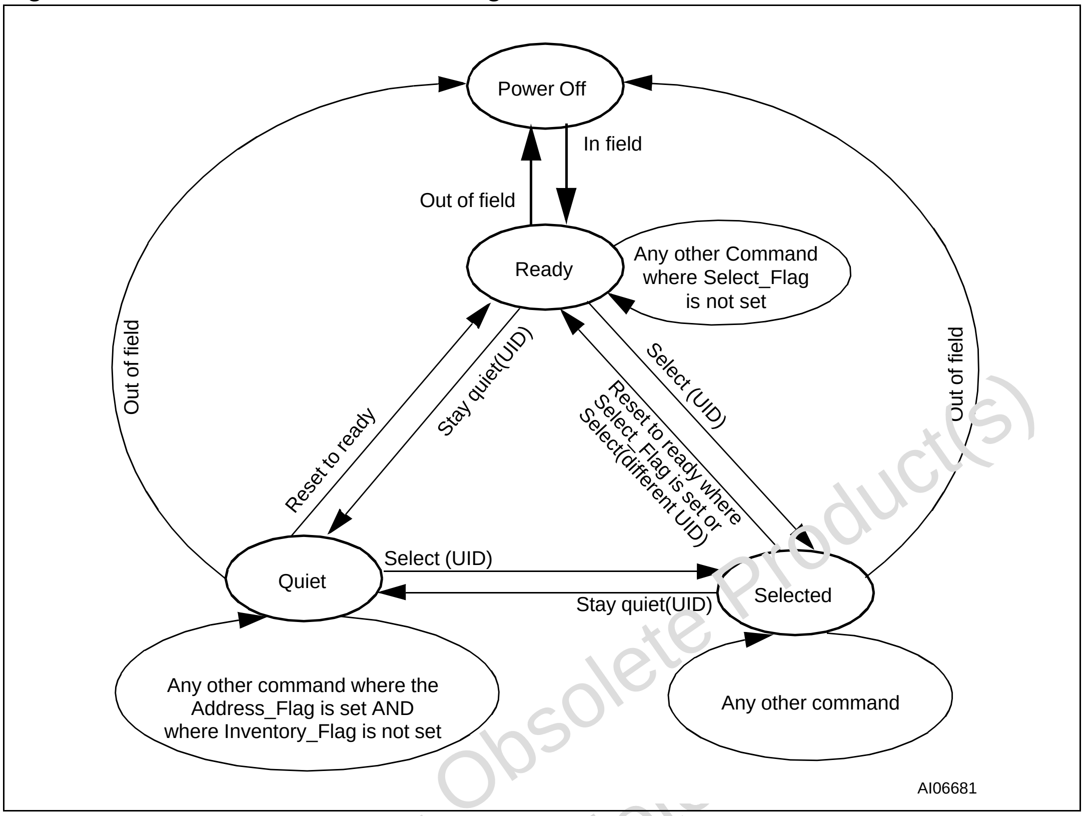
- Request in Select mode with the Select flag set
- Request in Addressed mode if the UID match.
- Request in Non-Addressed mode as it is general Request.

Table 7. LRI512 response, depending on the states of the request flags

Flags	Address_Flag		Select_Flag	
	1 Addressed	0 Non addressed	1 Selected	0 Non selected
LRI512 in Ready or Selected state (Devices in Quiet state do not answer)		X		X
LRI512 in Selected state		X	X	
LRI512 in Ready, Quiet or Selected state (the device which match the UID)	X			X
Error (03h)	X		X	

Obsolete Product(s) - Obsolete Product(s)

Figure 29. LRI512 state transition diagram



1. The intention of the state transition method is that only one LRI512 should be in the selected state at a time.

12 Modes

The set of LRI512s that can answer a given Request are those whose current “Mode” is the appropriate one for that request.

12.1 Addressed mode

When the Address_flag is set to 1 (addressed mode), the Request shall contain the Unique ID (UID) of the addressed LRI512.

Any LRI512 receiving a Request with the Address_flag set to 1 shall compare the received Unique ID to its own UID.

If it matches, it shall execute it (if possible) and return a Response to the VCD as specified by the command description.

If it does not match, it shall remain silent.

12.2 Non-addressed mode (general request)

When the Address_flag is set to 0 (non-addressed mode), the Request shall not contain a Unique ID. Any LRI512 receiving a Request with the Address_flag set to 0 executes it and returns a Response to the VCD as specified by the command description.

12.3 Select mode

When the Select_flag is set to 1 (select mode), the Request shall not contain a LRI512 Unique ID. The LRI512 in the Selected State receiving a Request with the Select_flag set to 1 executes it and returns a Response to the VCD as specified by the command description.

Only LRI512s in the Selected State answer to a Request having the Select Flag set to 1.

The system design ensures in theory that only one LRI512 can be in the Select state.

13 Request format

The request consists of

- SOF
- Flags
- A Command Code
- Parameters and Data
- CRC
- EOF

Table 8. General request format

SOF	Request Flags	Command Code	Parameters	Data	CRC	EOF

13.1 Request flags

In a request, the flags field specifies the actions to be performed by the LRI512, and whether corresponding fields are present or not.

It consists of eight bits.

The bit 3 (Inventory_flag) of the request flag defines the content of the 4 MSBs (bits 5 to 8).

When bit 3 is reset (0), bits 5 to 8 define the LRI512 selection criteria.

When bit 3 is set (1), bits 5 to 8 define the LRI512 Inventory parameters.

Table 9. Request flags 1 to 4 definition

Bit	Request flag	Level	Definition
Bit 1	Subcarrier flag(1)	0	A single subcarrier frequency shall be used by the LRI512
		1	Two subcarriers shall be used by the LRI512
Bit 2	Data_rate flag(2)	0	Low data rate is used
		1	High data rate is used
Bit 3	Inventory flag	0	Flags 5 to 8 meaning are according to *Table 10*
		1	Flags 5 to 8 meaning are according to *Table 11*
Bit 4	Protocol extension flag	0	No Protocol format extension

1. Subcarrier_flag refers to the LRI512-to-VCD communication.
2. Data_rate_flag refers to the LRI512-to-VCD communication

Table 10. Request flags 5 to 8 when bit 3 = 0

Bit	Request flag	Level	Definition
Bit 5	Select flag[(1)]	0	Request shall be executed by any LRI512 according to the setting of Address_flag
		1	Request shall be executed only by LRI512 in Selected State
Bit 6	Address flag	0	Request is not addressed. UID field is not present. It shall be executed by all LRI512.
		1	Request is addressed. UID field is present. It shall be executed only by the LRI512 whose UID matches the UID specified in the Request.
Bit 7	Option flag	0	
Bit 8	RFU	0	

1. if the Select_flag is set to 1, the Address_flag shall be set to 0 and the UID field shall not be present in the Request.

Table 11. Request flags 5 to 8 when Bit 3 = 1

Bit	Request flag	Level	Definition
Bit 5	AFI flag	0	AFI field is not present
		1	AFI field is present
Bit 6	Nb_slots flag	0	16 slots
		1	1 slot
Bit 7	Option flag	0	
Bit 8	RFU	0	

14 Response format

The Response consists of

– SOF
– Flags
– Parameters and Data
– CRC
– EOF

Table 12. General response format

SOF	Response Flags	Parameters	Data	CRC	EOF

14.1 Response flags

In a Response, the flags field indicates how actions have been performed by the LRI512 and whether corresponding fields are present or not. It consists of eight bits.

Table 13. Response Flags 1 to 8 definition

Bit	Request flag	Level	Definition
Bit 1	Error flag	0	No error
		1	Error detected. Error code is in the "Error" field.
Bit 2	RFU	0	
Bit 3	RFU	0	
Bit 4	Extension flag	0	No extension
Bit 5	RFU	0	
Bit 6	RFU	0	
Bit 7	RFU	0	
Bit 8	RFU	0	

14.2 Response error code

If the Error Flag is set by the LRI512 in the Response, the Error Code field is present and provides information about the error that occurred.

The following error codes are specified. Other codes are reserved for future use.

Table 14. Response error code definition

Error code	Meaning
03h	The option is not supported
10h	The specified block is not available
11h	The specified block is already locked and thus cannot be locked again
12h	The specified block is locked and its content cannot be changed.

15 Anticollision

The purpose of the anticollision sequence is to inventory the LRI512s present in the VCD field by their unique ID (UID).

The VCD is the master of the communication with one or multiple LRI512s. It initiates LRI512 communication by issuing the Inventory Request.

The LRI512 sends its Response in the slot determined, or might not respond.

15.1 Request parameters

When issuing the Inventory Command, the VCD shall:

- set the Nb_slots_flag to the desired setting,
- add after the Command Field the Mask Length and the Mask Value,
- The Mask Length is the number of significant bits of the Mask Value.
- The Mask Value is contained in an integer number of bytes. The Mask Length indicates the number of significant bits. LSB shall be transmitted first.
- If the Mask Length is not a multiple of 8 bits, the Mask Value MSB shall be padded with the required number of null bits (set to 0) so that the Mask Value is contained in an integer number of bytes.
- The next field starts on the next byte boundary.

The inventory request formats are shown below.

MSB LSB

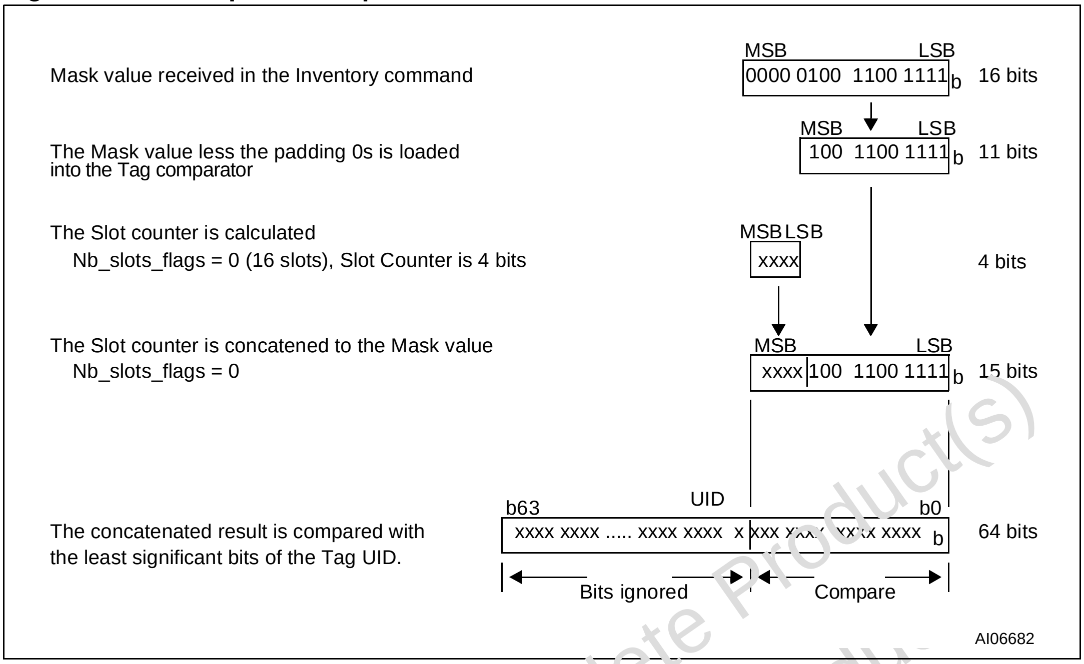
SOF	Request Flags	Command	Optional AFI	Mask length	Mask 1	CRC	EOF
	8 bits	8 bits	8 bits	8 bits	0 to 8 bytes	16 bits	

In the example of the *Table 15* and *Figure 30*, the Mask Length is 11 bits. The Mask Value MSB is padded with five bits set to 0. The 11 bits Mask plus the current slot number is compared to the UID.

Table 15. Example of the padding of an 11 bit mask value

(b_{15}) MSB	**LSB (b_0)**
0000 0	100 1100 1111
Pad	11 bits Mask Value

Figure 30. Principle of comparison between the mask, slot number and UID



The AFI field shall be present if the AFI_flag is set.

The pulse shall be generated according to the definition of the EOF in ISO/IEC 15693-2.

The first slot starts immediately after the reception of the Request EOF.

To switch to the next slot, the VCD sends an EOF.

The following rules and restrictions apply:

- if no LRI512 answer is detected, the VCD may switch to the next slot by sending an EOF
- if one or more LRI512 answers are detected, the VCD shall wait until the complete frame has been received before sending an EOF for switching to the next slot.

16 Request processing by the LRI512

Upon reception of a valid Request, the LRI512 performs the following algorithm, where:

- NbS is the total number of slots (1 or 16)
- SN is the current slot number (0 to 15)
- LSB (value, n) function returns the n least significant bits of the value
- MSB (value, n) function returns the n most significant bits of the value
- “&” is the concatenation operator
- Slot_Frame is either a SOF or an EOF

```
SN = 0
if (Nb_slots_flag)
   then  NbS = 1
         SN_length = 0
         endif
   else  NbS = 16
         SN_length = 4
         endif

label1:
if LSB(UID, SN_length + Mask_length) =
  LSB(SN,SN_length)&LSB(Mask,Mask_length)
   then  answer to inventory request
         endif

wait (Slot_Frame)

if Slot_Frame = SOF
   then  Stop Anticollision
         decode/process request
         exit
         endif

if Slot_Frame = EOF
   if SN < NbS-1
      then  SN = SN + 1
            goto label1
            exit
            endif
   endif
```

17 Explanation of the possible cases

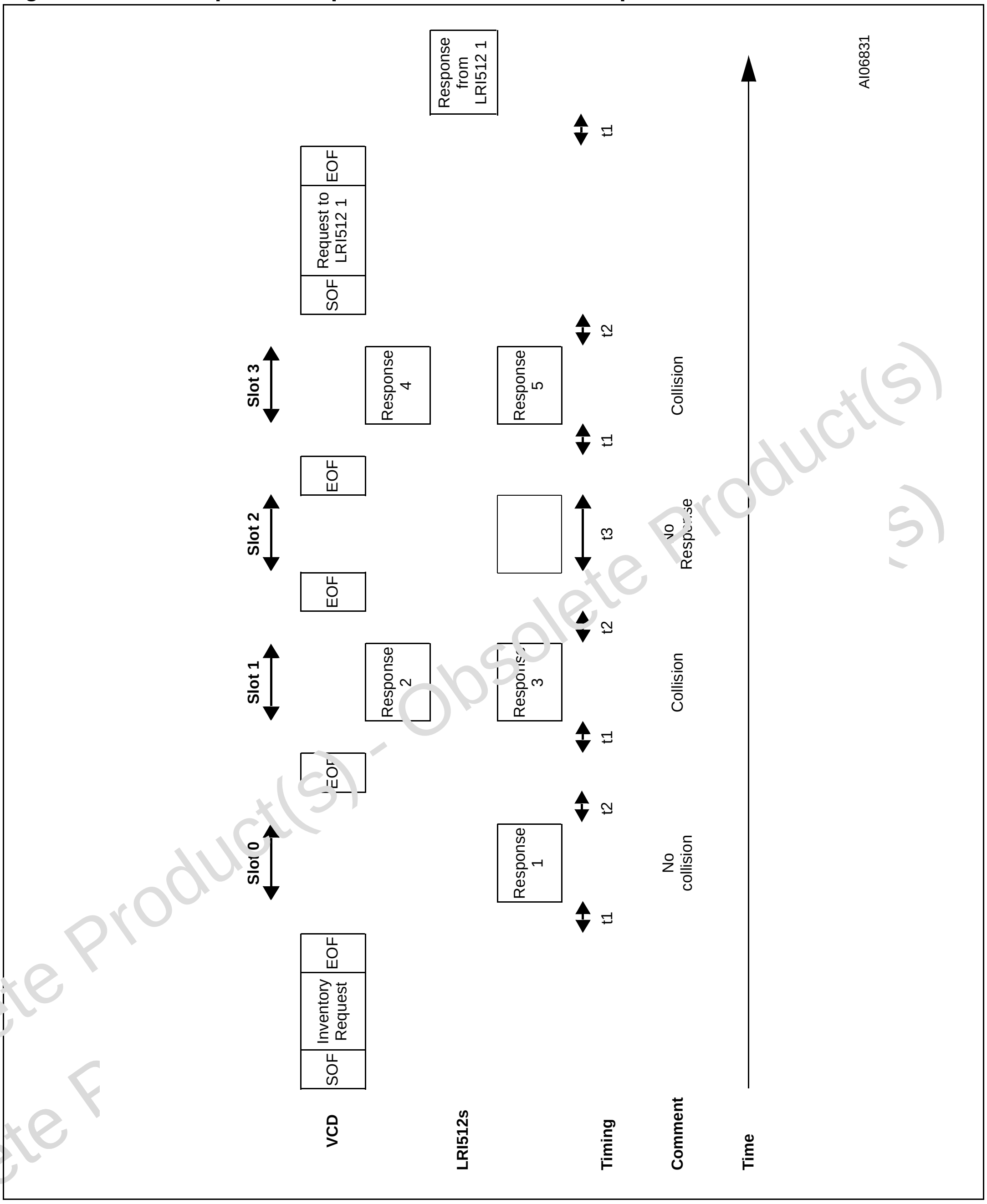
Figure 31 summarizes the main possible cases that can occur during an anticollision sequence when the slot number is 16.

The different steps are:

- The VCD sends an Inventory Request, in a frame, terminated by an EOF. The number of slots is 16.
- LRI512 #1 transmits its Response in Slot 0. It is the only one to do so, therefore no collision occurs and its UID is received and registered by the VCD;
- The VCD sends an EOF, meaning to switch to the next slot.
- In slot 1, two LRI512s, #2 and #3, transmit their Responses. This generates a collision. The VCD records it, and remembers that a collision was detected in Slot 1.
- The VCD sends an EOF, meaning to switch to the next slot.
- In Slot 2, no LRI512 transmits a Response. Therefore the VCD does not detect a LRI512 SOF and decides to switch to the next slot by sending an EOF.
- In slot 3, there is another collision caused by Responses from LRI512 #4 and #5
- The VCD then decides to send a Request (for instance a Read Block) to LRI512 #1, whose UID was already correctly received.
- All LRI512s detect a SOF and exit the anticollision sequence. They process this Request and since the Request is addressed to LRI512 #1, only LRI512 #1 transmits its Response.
- All LRI512s are ready to receive another Request. If it is an Inventory command, the slot numbering sequence restarts from 0.

Note: the decision to interrupt the anticollision sequence is up to the VCD. It could have continued to send EOFs until Slot 15 and then send the Request to LRI512 #1.

Figure 31. Description of a possible anticollision sequence



18 Timing definition

18.1 t_1: LRI512 response delay

t_1 is as defined in *Table 16*.

Upon detection of the rising edge of the EOF received from the VCD, the LRI512 wait for a time equal to

$t_1(typ) = 4352/f_C$ (see *Table 54*)

before starting to transmit its response to a VCD request or switch to the next slot when in an inventory process.

The EOF is defined in *Figure 10: EOF for either data coding mode*.

18.2 t_2: VCD new request delay

t_2 is the time after which the VCD may send an EOF to switch to the next slot when one or more LRI512 responses have been received during an inventory command. It starts from the reception of the EOF received from the LRI512s.

The EOF sent by the VCD may be either 10% or 100% modulated independent of the modulation index used for transmitting the VCD request to the LRI512.

t_2 is also the time after which the VCD may send a new request to the LRI512 as described in *Figure 28: LRI512 protocol timing*.

$t_2(min) = 4192/f_C$ (see *Table 54*)

18.3 t3: VCD new request delay when no LRI512 response

t_3 is the time after which the VCD may send an EOF to switch to the next slot when no LRI512 response has been received.

The EOF sent by the VCD may be either 10% or 100% modulated independent of the modulation index used for transmitting the VCD request to the LRI512.

From the time the VCD has generated the rising edge of an EOF:

- If this EOF is 100% modulated, the VCD shall wait a time at least equal to $t_{3minimum}$ before sending a subsequent EOF.
- If this EOF is 10% modulated, the VCD shall wait a time at least equal to the sum of $t_{3minimum}$ + the nominal response time of a LRI512, which depend on the LRI512 data rate and subcarrier modulation mode before sending a subsequent EOF.

Table 16. Timing values (see *Table 54*)(1)

	Min.	Nominal	Max.
t_1	t_1(min)	t_1(typ)	t_1(max)
t_2	t_2(min)	—	—
t_3	t_1(max) + t_{SOF} (2) (3)	—	—

1. The tolerance of specific timings is ± $32/f_C$.
2. t_{SOF} is the duration for the LRI512 to transmit an SOF to the VCD. t_{SOF} is dependant on the current data rate: High data rate or Low data rate.
3. t_1(max) does not apply for write alike requests. Timing conditions for write alike requests are defined in the command description.

19 Command codes

The LRI512 supports the following command codes:

Table 17. Command codes

Command code	Function
0x01	Inventory
0x02	Stay Quiet
0x20	Read Single Block
0x21	Write Single Block
0x22	Lock Block
0x25	Select
0x26	Reset to Ready
0x27	Write AFI
0x28	Lock AFI
0xA0	Activate EAS
0xA1	Deactivate EAS
0xA2	POOL EAS

20 Inventory

Command Code = 0x01

When receiving the Inventory request, the LRI512 performs the anticollision sequence. The Inventory_flag shall be set to 1. The Meaning of Flags 5 to 8 is according to *Figure 11: Request flags 5 to 8 when Bit 3 = 1*. The Request (*Table 18*) contains:

- Flags,
- Inventory Command code
- AFI if the AFI flag is set
- Mask Length
- Mask Value
- CRC

The Response (Table 19) contains:

- Flags
- DSFID (always 00h)
- Unique ID

20.0.1 Note on inventory operation

In the current LRI512 device, it is not possible to use the full range of Mask Length capability to covert the complete INVENTORY sequence. Values above the ones mentioned are not allowed:

- 16 slots mode (Request flag b_6=0): Mask Length must be in the range 0 to 27.
- 1 slot mode (Request flag b_6=1): Mask Length must be in the range 0 to 20.

STMicroelectronics programs the UID in such a way that it guarantees that the anticollision sequence is able to detect all LRI512 in the reader field.

Table 18. Inventory request format

Request SOF	Request Flags	Inventory	Optional AFI	Mask Length	Mask Value	CRC16	Request EOF
	8 bits	0x01	8 bits	8 bits	0 - 64 bits	16 bits	

Table 19. Inventory response format

Response SOF	Response Flags	DSFID	UID	CRC16	Response EOF
	8 bits	0x00	64 bits	16 bits	

21 Stay Quiet

Command Code = 0x02

When receiving the Stay Quiet command, the LRI512 enters the Quiet State, and does *not* send back a Response. There is *no* response to the Stay Quiet Command.

When in the Quiet State:

– the LRI512 does not process any Request if Inventory_flag is set,
– the LRI512 processes any addressed Request

The LRI512 exits the Quiet State when:

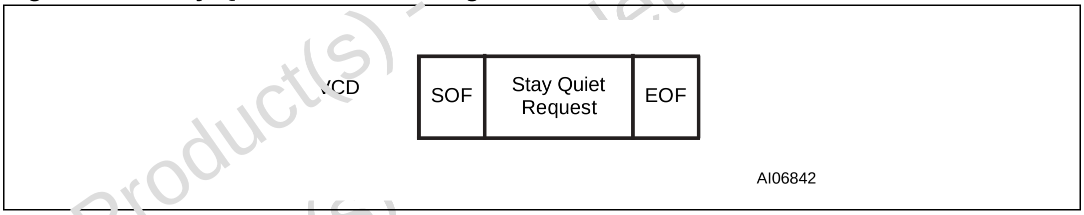
– reset (power off)
– receiving a Select request. It then goes to the Selected state
– receiving a Reset to Ready request. It then goes to the Ready state.

The Stay Quiet Command (*Table 20*) shall always be executed in Addressed Mode (Select_Flag is set to 0 and Address_Flag is set to 1).

Table 20. Stay Quiet request format

Request SOF	Request Flags	Stay Quiet	UID	CRC16	Request EOF
	8 bits	0x02	64 bits	16 bits	

Figure 32. Stay Quiet frame exchange between VCD and LRI512



22 Read Single Block

Command Code = 0x20

When receiving the Read Single Block Command, the LRI512 read the requested block and send back its 32 bits value in the Response.The Option_Flag is supported.

Request parameter (*Table 21*):

- Option_Flag
- UID (Optional)
- Block Number

Response parameter (*Table 22*):

- Block Locking Status if Option_Flag is set
- 4 bytes of Block Data

Response parameter (*Table 24*):

- Error Code as Error_Flag is set

Table 21. Read Single Block request format

Request SOF	Request Flags	Read Single Block	UID	Block number	CRC16	Request EOF
	8 bits	0x20	64 bits	8 bits	16 bits	

Table 22. Read Single Block response format when Error_Flag is NOT set

Response SOF	Response Flags	Block Locking Status	Data	CRC16	Response EOF
	8 bits	8 bits	32 bits	16 bits	

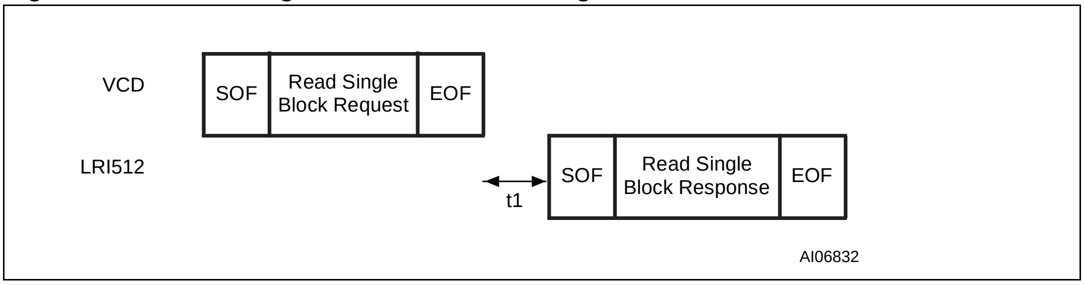
Table 23. Block locking status

b_7 (bit b_0 for ISO)	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0: Current block not locked 1: Current block locked	Reserved for future use. All at 0						

Table 24. Read Single Block response format when Error_Flag is set

Response SOF	Response_Flags	Error Code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 33. READ Single Block frame exchange between VCD and LRI512



23 Write Single Block

Command Code = 0x21

When receiving the Write Single Block Command, the LRI512 writes the requested block with the data contained in the Request, and reports the success of the operation in the Response. The Option_Flag is not supported.

During the write cycle, t_W, no modulation (neither 100% nor 10%) shall occur, otherwise the LRI512 may program the data incorrectly in the memory. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 25*):

- UID (Optional)
- Block Number
- Data

Response parameter (*Table 26*):

- No parameter. The response is sent back after the write cycle

Response parameter (*Table 27*):

- Error Code as Error_Flag is set

Table 25. Write Single Block request format

Request SOF	Request Flags	Write Single Block	UID	Block number	Data	CRC16	Request EOF
	8 bits	0x21	64 bits	8 bits	32 bits	16 bits	

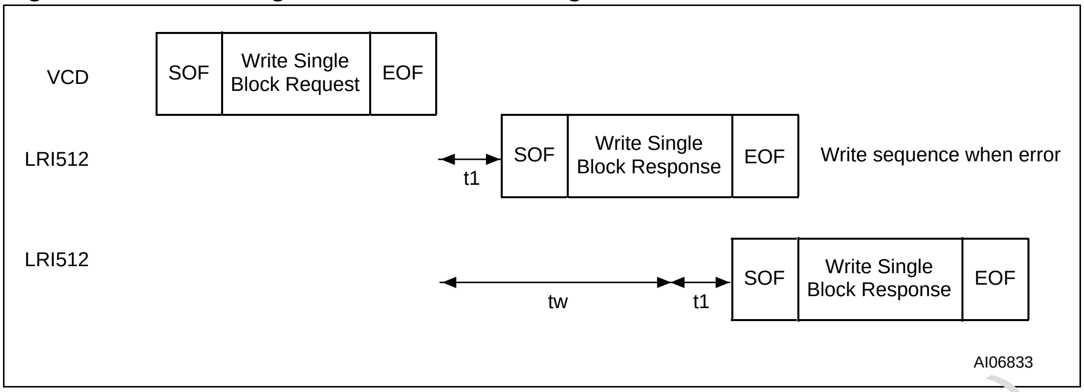
Table 26. Write Single Block response format when error flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 27. Write Single Block response format when error flag is set

Response SOF	Response_Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 34. Write Single Block frame exchange between VCD and LRI512



24 Lock Block

Command Code = 0x22

When receiving the Lock Block Command, the LRI512 lock permanently the requested block. The Option_Flag is not supported.

During the write cycle t_W, no modulation (never 100% nor 10%) shall occur. If so, the LRI512 may not lock correctly the memory block. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 28*):

- (Optional) UID
- Block Number

Response parameter (*Table 29*):

- No parameter.

Response parameter (*Table 30*):

- Error Code as Error_Flag is set

Table 28. Lock Single Block request format

Request SOF	Request Flags	Lock Block	UID	Block number	CRC16	Request EOF
	8 bits	0x22	64 bits	8 bits	16 bits	

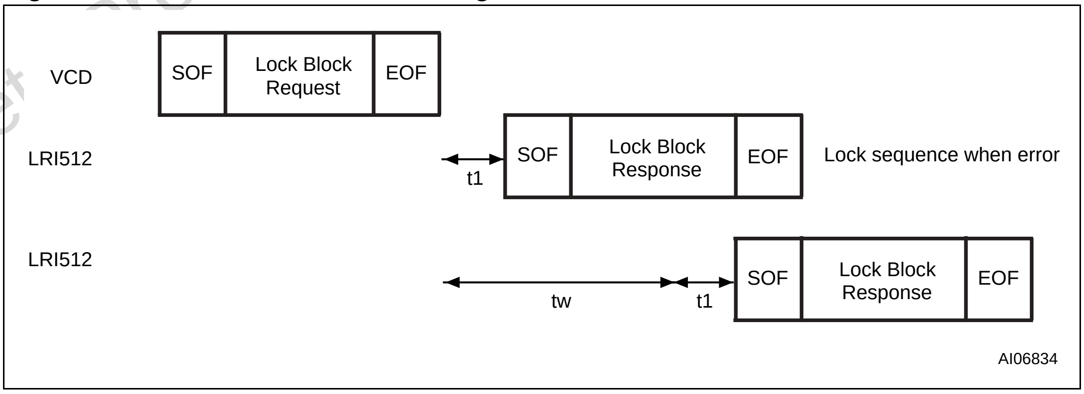
Table 29. Lock Block response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 30. Lock Block response format when Error Flag is set

Response SOF	Response_ Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 35. Lock Block frame exchange between VCD and LRI512



25 Select

Command Code = 0x25

When receiving the Select Command:

- if the UID is equal to its own UID, the LRI512 enter or stay in the Selected state and send a Response.
- if it is different, the selected LRI512 return to the Ready state and do not send a Response.

Request parameter (*Table 31*):

– UID

Response parameter (*Table 32*):

– No parameter.

Response parameter (*Table 33*):

– Error Code as Error_Flag is set

Table 31. Select request format

Request SOF	Request Flags	Select	UID	CRC16	Request EOF
	8 bits	0x25	64 bits	16 bits	

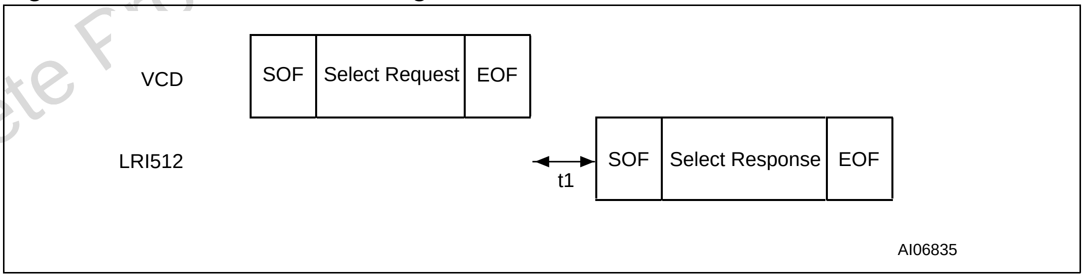
Table 32. Select Block response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 33. Select response format when Error Flag is set

Response SOF	Response_Flags	Error Code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 36. Select frame exchange between VCD and LRI512



26 Reset to Ready

Command Code = 0x26

When receiving a Reset to Ready Command, the LRI512 return to the Ready state.

Request parameter (*Table 34*):

– UID (Optional)

Response parameter (*Table 35*):

– No parameter.

Response parameter (*Table 36*):

– Error Code as Error_Flag is set

Table 34. Reset to Ready request format

Request SOF	Request Flags	Reset to Ready	UID	CRC16	Request EOF
	8 bits	0x26	64 bits	16 bits	

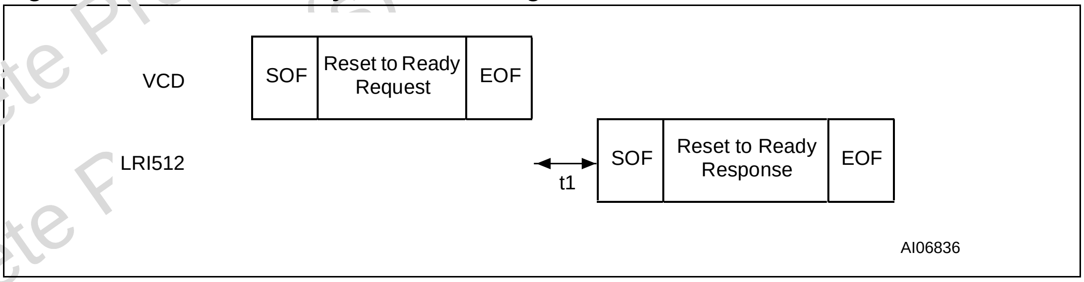
Table 35. Reset to Ready response format when error flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 36. Reset to Ready response format when error flag is set

Response SOF	Response_Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 37. Reset to Ready frame exchange between VCD and LRI512



27 Write AFI

Command Code = 0x27

When receiving the Write AFI Request, the LRI512 write the AFI byte value into its memory. The Option_Flag is not supported.

During the write cycle t_W, no modulation (never 100% nor 10%) shall occur. If so, the LRI512 may not Write correctly the AFI value into the memory. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 37*):

– UID (Optional)

– AFI

Response parameter (*Table 38*):

– No parameter.

Response parameter (*Table 39*):

– Error Code as Error_Flag is set

Table 37. Write AFI request format

Request SOF	Request Flags	Write AFI	UID	AFI	CRC16	Request EOF
	8 bits	0x27	64 bits	8 bits	16 bits	

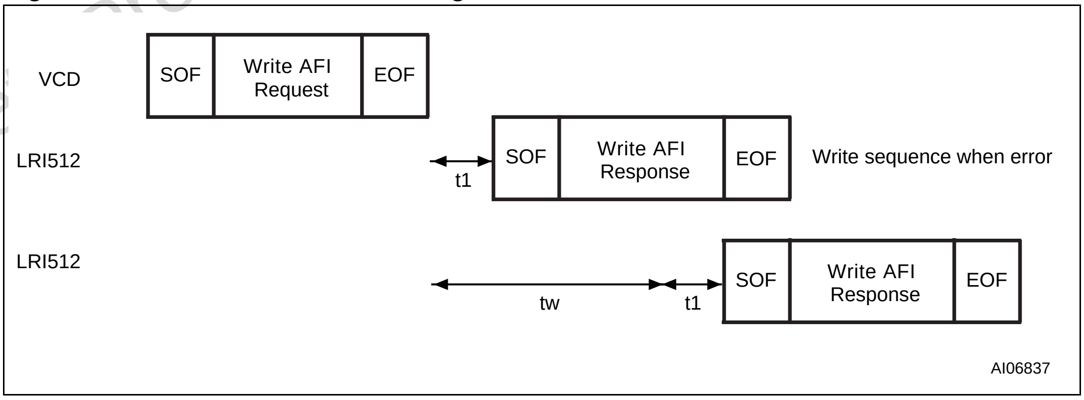
Table 38. Write AFI response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 39. Write AFI response format when Error Flag is set

Response SOF	Response_Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 38. Write AFI frame exchange between VCD and LRI512



28 Lock AFI

Command code = 0x28

When receiving the Lock AFI Request, the LRI512 lock the AFI value permanently. The Option_Flag is not supported.

During the write cycle t_W, no modulation (never 100% nor 10%) shall occur. If so, the LRI512 may not Lock correctly the AFI value into the memory. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 40*):

– UID (Optional)

Response parameter (*Table 41*):

– No parameter.

Response parameter (*Table 42*):

– Error Code as Error_Flag is set

Table 40. Lock AFI request format

Request SOF	Request Flags	Lock AFI	UID	CRC16	Request EOF
	8 bits	0x28	64 bits	16 bits	

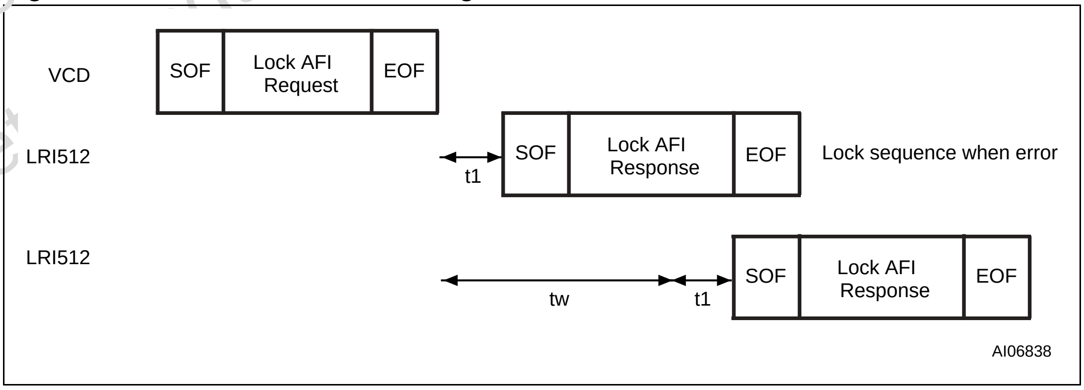
Table 41. Lock AFI response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 42. Lock AFI response format when Error Flag is set

Response SOF	Response_ Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 39. LOCK AFI frame exchange between VCD and LRI512



29 Activate EAS

Command Code = 0xA0

When receiving the Activate EAS Request, the LRI512 set the non-volatile EAS bit. The Option_Flag is not supported.

During the write cycle t_W, no modulation (never 100% nor 10%) shall occur. If so, the LRI512 may not set correctly the EAS bit. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 43*):

– UID (Optional)

Response parameter (*Table 44*):

– No parameter.

Response parameter (*Table 45*):

– Error Code as Error_Flag is set

Table 43. Activate EAS request format

Request SOF	Request Flags	Activate EAS	IC Mfg code	UID	CRC16	Request EOF
	8 bits	0xA0	0x02	64 bits	16 bits	

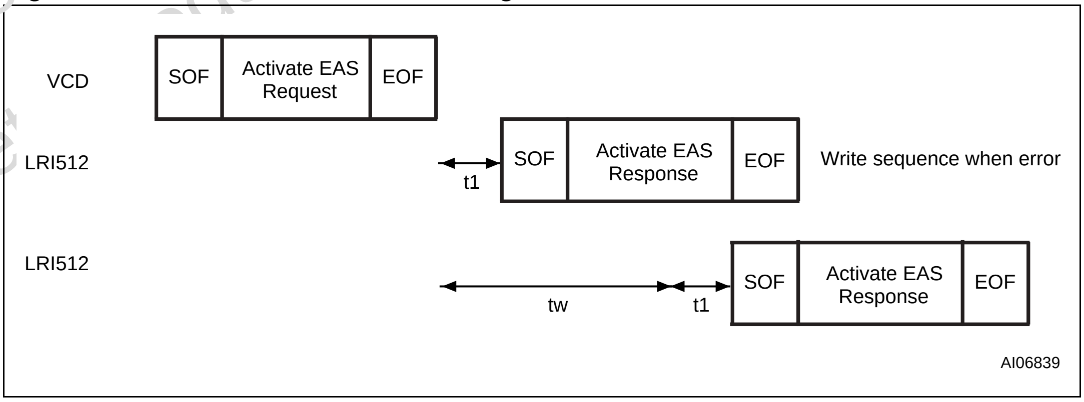
Table 44. Activate EAS response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 45. Activate EAS response format when Error Flag is set

Response SOF	Response_Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 40. Activate EAS frame exchange between VCD and LRI512



30 Deactivate EAS

Command Code = 0xA1

When receiving the Deactivate EAS Request, the LRI512 reset the non-volatile EAS bit. The Option_Flag is not supported.

During the write cycle t_W, no modulation (never 100% nor 10%) shall occur. If so, the LRI512 may not reset correctly the EAS bit. The t_W delay is a multiple of $t_{1nominal}$.

Request parameter (*Table 46*):

– UID (Optional)

Response parameter (*Table 47*):

– No parameter.

Response parameter (*Table 48*):

– Error Code as Error_Flag is set

Table 46. Deactivate EAS request format

Request SOF	Request Flags	Deactivate EAS	IC Mfg code	UID	CRC16	Request EOF
	8 bits	0xA1	0x02	64 bits	16 bits	

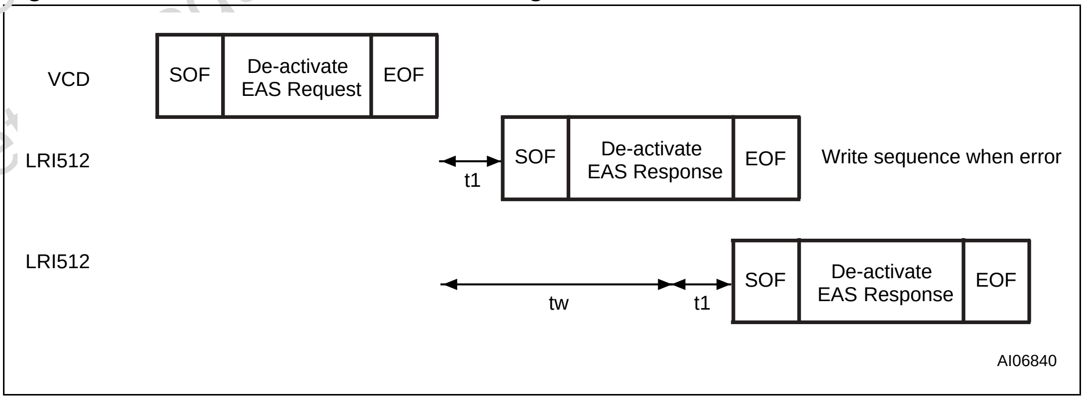
Table 47. Deactivate EAS response format when Error Flag is NOT set

Response SOF	Response_Flags	CRC16	Response EOF
	8 bits	16 bits	

Table 48. Deactivate EAS response format when Error Flag is set

Response SOF	Response_Flags	Error code	CRC16	Response EOF
	8 bits	8 bits	16 bits	

Figure 41. Deactivate EAS frame exchange between VCD and LRI512



31 Pool EAS

Command Code = 0xA2

When receiving the POOL EAS Request, all LRI512 with the non-volatile EAS bit set generate the EAS signal.

Request parameter (*Table 49* or *Table 50*):

– No parameter

Table 49. Pool EAS request format for one subcarrier modulation answer

Request SOF	Request_ Flags	Pool EAS	IC Mfg code	CRC16	Request EOF
	0x00	0xA2	0x02	16 bits	

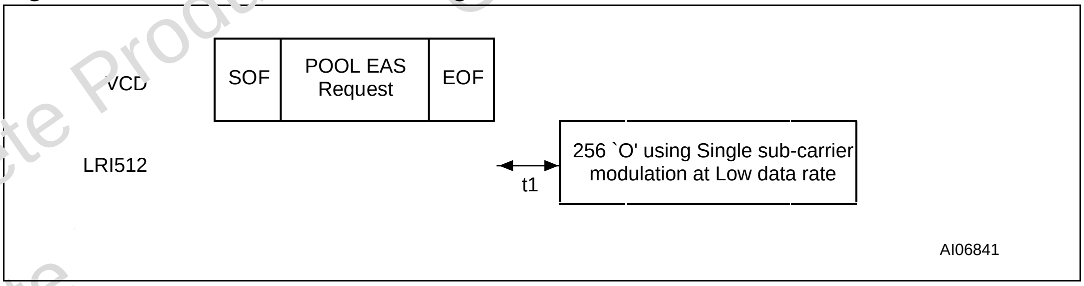
Table 50. Pool EAS request format for two subcarrier modulation answer

Request SOF	Request_ Flags	Pool EAS	IC Mfg code	CRC16	Request EOF
	0x01	0xA2	0x02	16 bits	

31.1 Pool EAS response format when the request frame is correctly received

The LRI512 generates a continuous stream of 256 bits at ‘0’ using the One or Two subcarrier modulation at Low data rate ended by 2 CRC bytes.

Figure 42. Pool EAS frame exchange between VCD and LRI512



32 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 51. Absolute maximum ratings

Symbol	Parameter		Condition	Min.	Max.	Unit
T_{STG}	Storage temperature	W4	ST antistatic bag, max 23 months	15	25	°C
		SB	Mounted wafer in a wafer-sawing box (8"), max 25 wafers	15	25	°C
		A1	40-60% RH, max 2 years	15	25	°C
V_{MAX}	Maximum input voltage on AC0 / AC1			–7	7	V
V_{ESD}	Electrostatic discharge voltage(1)	A1	ISO 10373-7	–7000	7000	V

1. ESD test: ISO10373-7 specification

33 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 52. Operating conditions

Symbol	Parameter		Min.	Max.	Unit
T_A	Ambient operating temperature	A1	–20	85	°C

Figure 43. LRI512 synchronous timing, transmit and receive

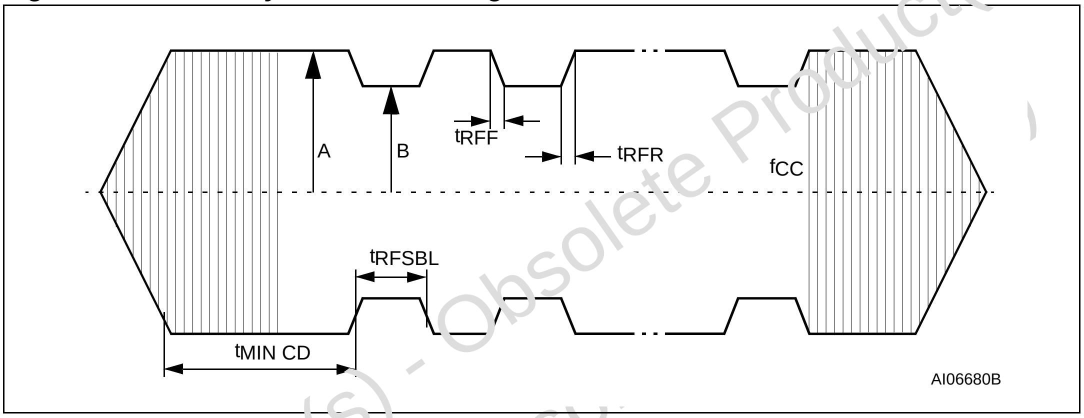


Figure 43 shows an ASK modulated signal, from the VCD to the LRI512. The test condition for the AC/DC parameters are:

- Close coupling condition with tester antenna (1mm)
- Gives LRI512 performance on tag antenna

Table 53. DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 52*)	Min.	Typ.	Max.	Unit
V_{CC}	Regulated voltage		1.5		3.0	V
V_{RET}	Back-scattering induced voltage A1	ISO10373-7	10			mV
I_{CC}	Supply current (active in Read)	V_{CC} = 3.0 V			150	µA
I_{CC}	Supply current (active in Write)	V_{CC} = 3.0 V			400	µA
C_{TUN}	Internal tuning capacitor	f = 13.56 MHz for W4/22		18.5		pF
C_{TUN}	Internal tuning capacitor	f = 13.56 MHz for W4/30		26		pF

Table 54. AC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 52*)	Min.	Typ.	Max.	Unit
f_{CC}	External RF signal frequency		13.553	13.56	13.567	MHz
$MI_{CARRIER}$	10% carrier modulation index	MI=(A-B)/(A+B)	10		30	%
t_{RFR}, t_{RFF}	10% rise and fall times		0		3.0	µs
t_{RFSBL}	10% minimum pulse width for bit		7.1		9.44	µs
$MI_{CARRIER}$	100% carrier modulation index	MI=(A-B)/(A+B)	95		100	%
t_{RFR}, t_{RFF}	100% rise and fall times		0		3.5	µs
t_{RFSBL}	100% minimum pulse width for bit		7.1		9.44	µs
t_{JIT}	Bit pulse jitter		-2		+2	µs
t_{MINCD}	Minimum time from carrier generation to first data	From H-field min		0.1	1	ms
f_{SH}	Subcarrier frequency High	$F_{CC}/32$		423.75		kHz
f_{SL}	Subcarrier frequency Low	$F_{CC}/28$		484.28		kHz
t_1	Time for LRI512 response	$4224/F_S$	313	320.9	322	µs
t_2	Time between commands	$4224/F_S$			309	µs
P_A[1]	H-field energy on LRI512 Antenna	A1	0.15		5	A/m
t_W	Programming time				5	ms

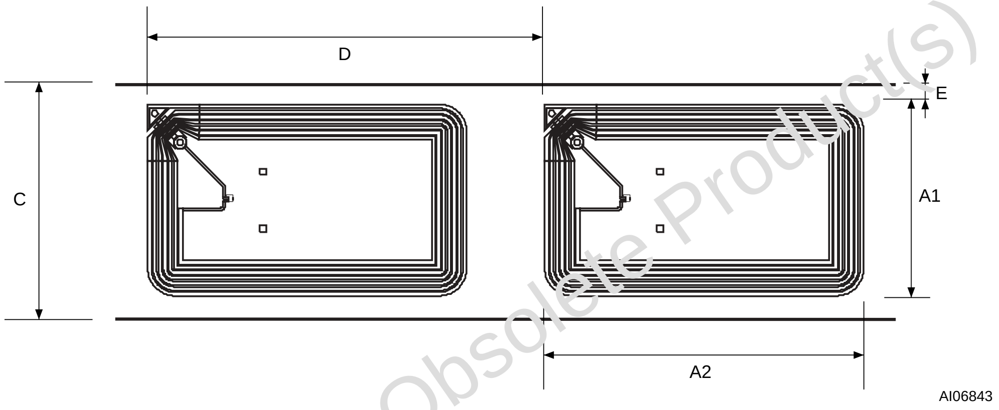
1. P_A Min is the minimum H-field required to communicate with the LRI512
P_A Max is the maximum H-field that the device can support before clamping the incoming signal

34 Package mechanical

In order to meet environmental requirements, ST offers the LRI512 in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 44. A1T – copper antenna, package outline

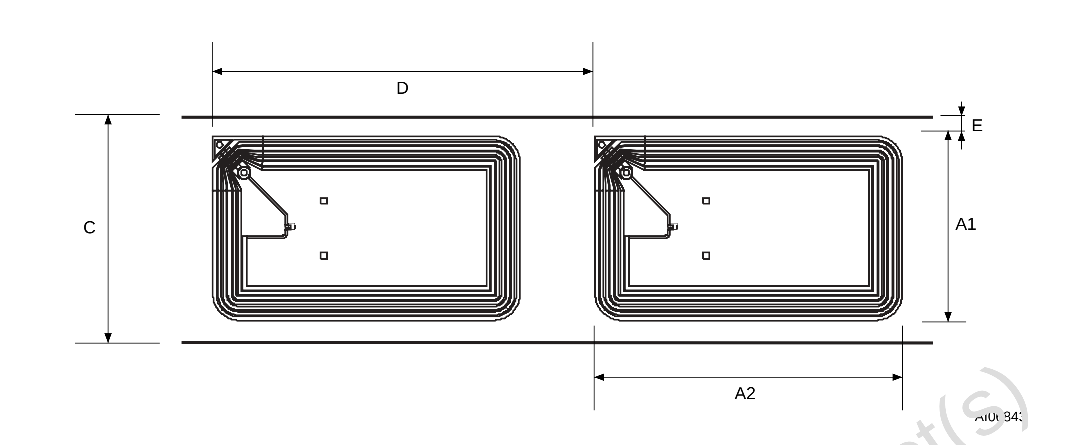


1. Drawing is not to scale.

Table 55. A1T – copper antenna, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A1 (Coil width)	45	44.5	45.5	1.772	1.752	1.791
A2 (Coil Length)	76	75.5	76.5	2.992	2.972	3.012
C (Web width)	48	47.5	48.5	1.890	1.870	1.909
D (Pitch)	96	95.5	96.5	3.780	3.760	3.800
E (Coil distance from web edge)	1.5	1	2	0.059	0.039	0.079
(Overall thickness of copper antenna coil)	0.110	0.090	0.130	0.004	0.003	0.005
(Silicon thickness)	0.180	0.165	0.195	0.007	0.006	0.008
Q (Unloaded Q value)	35			35		
F_{NOM} (Unloaded free-air resonance)	14.6 MHz			14.6 MHz		

Figure 45. A1S – copper antenna, package outline



1. Drawing is not to scale.

Table 56. A1S – copper antenna, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A1 (Coil width)	45	44.5	45.5	1.772	1.752	1.791
A2 (Coil length)	76	75.5	76.5	2.992	2.972	3.012
C (Web width)	48	47.5	48.5	1.890	1.870	1.909
D (Pitch)	96	95.5	96.5	3.780	3.760	3.800
E (Coil distance from web edge)	1.5	1	2	0.059	0.039	0.079
(Overall thickness of copper antenna coil)	0.110	0.090	0.130	0.004	0.003	0.005
(Silicon thickness)	0.180	0.165	0.195	0.007	0.006	0.008
Q (Unloaded Q value)	35			35		
F_{NOM} (Unloaded free-air resonance)	14.6 MHz			14.6 MHz		

35 Part numbering

Table 57. Ordering information scheme

Example: LRI512 - W4/22

Delivery form

W4/22	180 µm ± 15 µm unsawn wafer, 18.5 pF tuning capacitor
W4/30	180 µm ± 15 µm unsawn wafer, 26 pF tuning capacitor
SBN18/22	180 µm ± 15 µm sawn wafer with bumps, 18.5 pF tuning capacitor, 8 inch frame
A1T	ISO copper antenna on tape
A1S	ISO copper adhesive antenna on tape

The notation used for the device number is as shown in *Table 57*. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Appendix A Inventory algorithm example

The following pseudocode describes how the anticollision could be implemented on the VCD, using recursive functions.

A.1 Algorithm for pulsed slots

```
function push (mask, address); pushes on private stack
function pop (mask, address); pops from private stack
function pulse_next_pause; generates a power pulse
function store(LRI512_UID); stores LRI512_UID

function poll_loop (sub_address_size as integer)
   pop (mask, address)
   mask = address & mask; generates new mask
               ; send the Request
   mode = anticollision
   send_Request (Request_cmd, mode, mask length, mask value)
   for sub_address = 0 to (2^sub_address_size - 1)
      pulse_next_pause
      if no_collision_is_detected ; LRI512 is inventoried
         then
            store (LRI512_UID)
         else  ; remember a collision was detected
            push(mask,address)
         endif
      next sub_address

   if stack_not_empty ; if some collisions have been detected and
      then     ; not yet processed, the function calls itself
         poll_loop (sub_address_size); recursively to process the last stored
collision
      endif
end poll_loop

main_cycle:
   mask = null
   address = null
   push (mask, address)
   poll_loop(sub_address_size)
end_main_cycle
```

Appendix B CRC detection

B.1 CRC error detection method

The cyclic redundancy check (CRC) is calculated on all data contained in a message, from the start of the Flags through to the end of Data. This CRC is used from the VCD to the LRI512, and from the LRI512 to the VCD.

Table 58. CRC definition

CRC definition					
CRC type	**Length**	**Polynomial**	**Direction**	**Preset**	**Residue**
ISO/IEC 13239	16 bits	$X^{16} + X^{12} + X^5 + 1$ = Ox8408	Backward	0xFFFF	0xF0B8

To add extra protection against shift errors, a further transformation on the calculated CRC is made. The One's Complement of the calculated CRC is the value attached to the message for transmission.

For checking of received messages the two CRC bytes are often also included in the re-calculation, for ease of use. In this case, given the expected value for the generated CRC is the residue of F0B8h

B.2 CRC calculation example

This example in C language illustrates one method of calculating the CRC on a given set of bytes comprising a message.

B.3 C-Example to calculate or check the CRC16 according to ISO/IEC 13239

```
#define  POLYNOMIAL0x8408//  x^16 + x^12 + x^5 + 1
#define  PRESET_VALUE0xFFFF
#define  CHECK_VALUE0xF0B8

#define  NUMBER_OF_BYTES4// Example: 4 data bytes
#define  CALC_CRC1
#define  CHECK_CRC0

void main()
{
  unsigned int  current_crc_value;
  unsigned char array_of_databytes[NUMBER_OF_BYTES + 2] = {1, 2, 3, 4, 0x91, 0x39};
  int           number_of_databytes = NUMBER_OF_BYTES;
  int           calculate_or_check_crc;
  int           i, j;
  calculate_or_check_crc = CALC_CRC;
// calculate_or_check_crc = CHECK_CRC;// This could be an other example
  if (calculate_or_check_crc == CALC_CRC)
  {
      number_of_databytes = NUMBER_OF_BYTES;
  }
  else    // check CRC
```

```
    {
        number_of_databytes = NUMBER_OF_BYTES + 2;
    }

    current_crc_value = PRESET_VALUE;

    for (i = 0; i < number_of_databytes; i++)
    {
        current_crc_value = current_crc_value ^ ((unsigned int)array_of_databytes[i]);

        for (j = 0; j < 8; j++)
        {
            if (current_crc_value & 0x0001)
            {
                current_crc_value = (current_crc_value >> 1) ^ POLYNOMIAL;
            }
            else
            {
                current_crc_value = (current_crc_value >> 1);
            }
        }
    }

    if (calculate_or_check_crc == CALC_CRC)
    {
        current_crc_value = ~current_crc_value;

        printf ("Generated CRC is 0x%04X\n", current_crc_value);

        // current_crc_value is now ready to be appended to the data stream
        // (first LSByte, then MSByte)
    }
    else   // check CRC
    {
        if (current_crc_value == CHECK_VALUE)
        {
            printf ("Checked CRC is ok (0x%04X)\n", current_crc_value);
        }
        else
        {
            printf ("Checked CRC is NOT ok (0x%04X)\n", current_crc_value);
        }
    }
}
```

Appendix C Application family identifier (AFI)

The AFI (Application Family Identifier) represents the type of application targeted by the VCD and is used to extract from all the LRI512 present only the LRI512 meeting the required application criteria.

It is programmed by the LRI512 issuer (the purchaser of the LRI512). Once locked, it cannot be modified.

The most significant nibble of AFI is used to code one specific or all application families, as defined in *Table 59*.

The least significant nibble of AFI is used to code one specific or all application sub-families. Sub-family codes other than 0 are proprietary.

Table 59. AFI coding

AFI most significant nibble	AFI least significant nibble	Meaning VICCs respond from	Examples / Note
0	0	All families and sub-families	No applicative preselection
'X'	0	All sub-families of family X	Wide applicative preselection
'X'	'Y'	Only the Yth sub-family of family X	
0	'Y'	Proprietary sub-family Y only	
1	0, 'Y'	Transport	Mass transit, Bus, Airline,...
2	0, 'Y'	Financial	IEP, Banking, Retail,...
3	0, 'Y'	Identification	Access Control,...
4	0, 'Y'	Telecommunication	Public Telephony, GSM,...
5	0, 'Y'	Medical	
6	0, 'Y'	Multimedia	Internet services....
7	0, 'Y'	Gaming	
8	0, 'Y'	Data Storage	Portable Files, ...
9	0, 'Y'	Item Management	
A	0, 'Y'	Express Parcels	
B	0, 'Y'	Postal Services	
C	0, 'Y'	Airline Bags	
D	0, 'Y'	RFU	
E	0, 'Y'	RFU	
F	0, 'Y'	RFU	

1. X = 1h to Fh, Y = 1h to Fh

Revision history

Table 60. Document revision history

Date	Revision	Changes
16-Jul-2002	1.0	Document written
08-Nov-2007	2	Document reformatted. Small text changes. Document status changed from Datasheet to Not For New Design. A2, A1T/ISOR and C40 packages removed. t_{MAX} removed from *Figure 43: LRI512 synchronous timing, transmit and receive* and *Table 54: AC characteristics*. r_L removed and T_2 timing changed in *Table 54: AC characteristics*. All antennas are ECOPACK® compliant.