SHARP®

Integrated Circuits Group

LRS1382

Stacked Chip

32M Flash and 8M SRAM

(Model No.: LRS1382)

Spec No.: MFM2-J13222

Issue Date: March 1, 2001

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Description

The LRS1382 is a combination memory organized as 2,097,152 x16 bit flash memory and 524.288 x16 bit static RAM in one package.

Features

- Power supply • • • • 2.7V to 3.3V
- Operating temperature • • • • -25°C to +85°C
- Not designed or rated as radiation hardened
- 72pin CSP (LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and SRAM has P-type bulk silicon

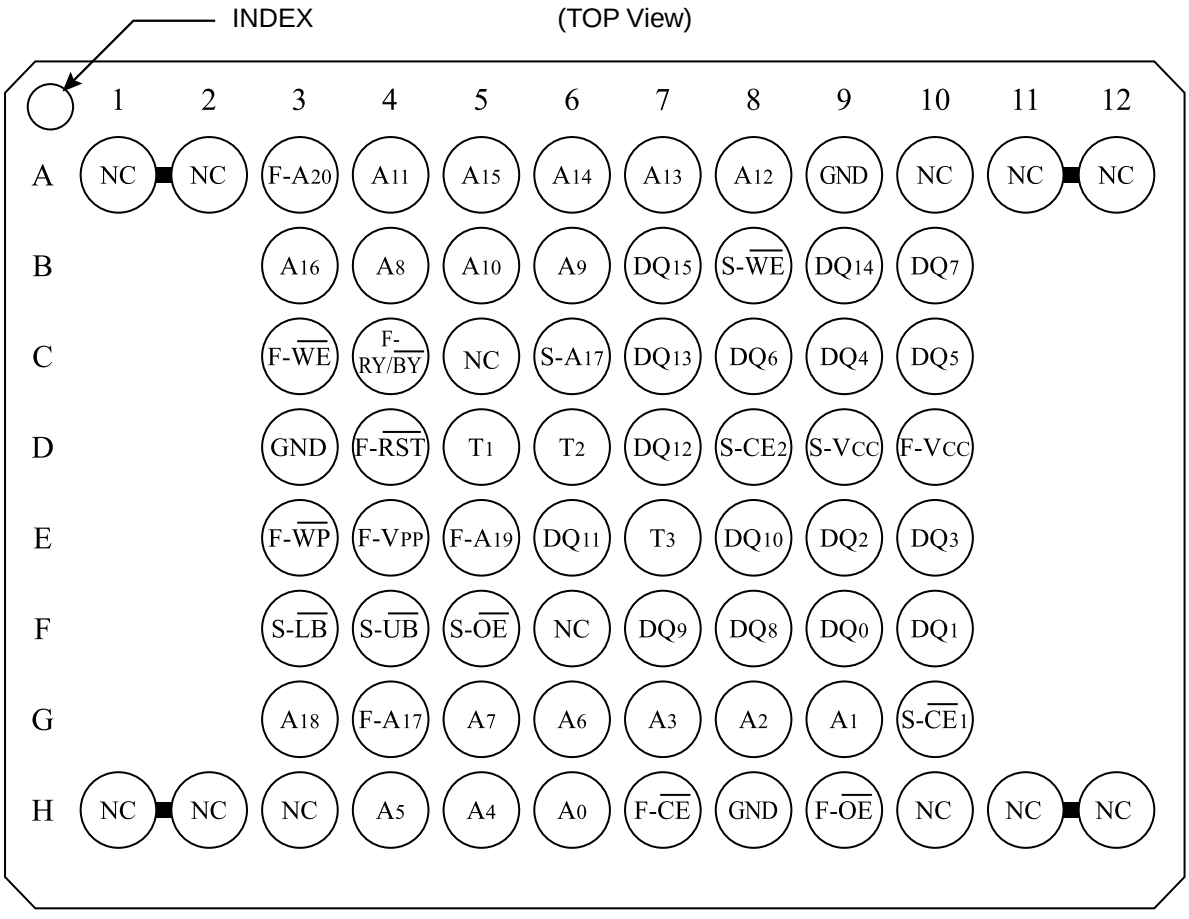
Flash Memory

- Access Time • • • • 85 ns (Max.)
- Power supply current (The current for F-V_{CC} pin and F-V_{PP} pin)
  - Read • • • • 25 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
  - Word write • • • • 60 mA (Max.)
  - Block erase • • • • 30 mA (Max.)
  - Reset Power-Down • • • • 25 µA (Max. F-$\overline{RST}$ = GND ± 0.2V, I_{OUT} (F-RY/$\overline{BY}$) = 0mA)
  - Standby • • • • 25 µA (Max. F-$\overline{CE}$ = F-$\overline{RST}$ = F-V_{CC} ± 0.2V)
- Optimized Array Blocking Architecture
  - Eight 4K-word Parameter Blocks
  - Sixty-Three 32K-word Main Blocks
  - Top Parameter Location
- Extended Cycling Capability
  - 100,000 Block Erase Cycles (F-V_{PP} = 2.7V to 3.3V)
  - 1,000 Block Erase Cycles and total 80 hours (F-V_{PP} = 11.7V to 12.3V)
- Enhanced Automated Suspend Options
  - Word Write Suspend to Read
  - Block Erase Suspend to Word Write
  - Block Erase Suspend to Read
- OTP Block
  - 4 Word + 4 Word Array

SRAM

- Access Time • • • • 70 ns (Max.)
- Power Supply current
  - Operating current • • • • 50 mA (Max. t_{RC}, t_{WC} = Min.)
  - • • • • 8 mA (Max. t_{RC}, t_{WC} = 1µs, CMOS Input)
  - Standby current • • • • 25 µA (Max.)
  - Data retention current • • • • 25 µA (Max. S-V_{CC} = 3.0V)

2. Pin Configuration



Note) From T1 to T3 pins are needed to be open.
Two NC pins at the corner are connected.
Do not float any GND pins.

Pin	Description	Type
A_0 to A_{16}, A_{18}	Address Inputs (Common)	Input
F-A_{17}, F-A_{19}, F-A_{20}	Address Inputs (Flash)	Input
S-A_{17}	Address Input (SRAM)	Input
F-$\overline{CE}$	Chip Enable Inputs (Flash)	Input
S-$\overline{CE}_1$, S-CE_2	Chip Enable Inputs (SRAM)	Input
F-$\overline{WE}$	Write Enable Input (Flash)	Input
S-$\overline{WE}$	Write Enable Input (SRAM)	Input
F-$\overline{OE}$	Output Enable Input (Flash)	Input
S-$\overline{OE}$	Output Enable Input (SRAM)	Input
S-$\overline{LB}$	SRAM Byte Enable Input (DQ_0 to DQ_7)	Input
S-$\overline{UB}$	SRAM Byte Enable Input (DQ_8 to DQ_{15})	Input
F-$\overline{RST}$	Reset Power Down Input (Flash) Block erase and Write : V_{IH} Read : V_{IH} Reset Power Down : V_{IL}	Input
F-$\overline{WP}$	Write Protect Input (Flash) When F-$\overline{WP}$ is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When F-$\overline{WP}$ is V_{IH}, lock-down is disabled.	Input
F-RY/$\overline{BY}$	Ready/Busy Output (Flash) During an Erase or Write operation : V_{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ_0 to DQ_{15}	Data Inputs and Outputs (Common)	Input / Output
F-V_{CC}	Power Supply (Flash)	Power
S-V_{CC}	Power Supply (SRAM)	Power
F-V_{PP}	Monitoring Power Supply Voltage (Flash) Block Erase and Write : F-V_{PP} = $V_{PPH1/2}$ All Blocks Locked : F-V_{PP} < V_{PPLK}	Input
GND	GND (Common)	Power
NC	Non Connection (Should be all open)	-
T_1 to T_3	Test pins (Should be all open)	-

3. Truth Table

3.1 Bus operation(1)

Flash	SRAM	Notes	F-$\overline{CE}$	F-$\overline{RST}$	F-$\overline{OE}$	F-$\overline{WE}$	S-$\overline{CE}_1$	S-CE_2	S-$\overline{OE}$	S-$\overline{WE}$	S-$\overline{LB}$	S-$\overline{UB}$	DQ_0 to DQ_{15}
Read	Standby	3,5	L	H	L	H	(8)		X	X	(8)		(7)
Output Disable		5			H								High-Z
Write		2,3,4,5				L							D_{IN}
Standby	Read	5	H	H	X	X	L	H	L	H	(9)		
	Output Disable	5							H	H	X	X	High-Z
									X	X	H	H	
	Write	5							X	L	(9)		
Reset Power Down	Read	5,6	X	L	X	X	L	H	L	H	(9)		
	Output Disable	5,6							H	H	X	X	High-Z
									X	X	H	H	
	Write	5,6							X	L	(9)		
Standby	Standby	5	H	H	X	X	(8)		X	X	(8)		High-Z
Reset Power Down		5,6	X	L									

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L. High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when F-V_{PP} = $V_{PPH1/2}$ and F-V_{CC} = 2.7V to 3.3V.
   Block erase, full chip erase, (page buffer) program or OTP program with F-V_{PP} < $V_{PPH1/2}$ (Min.) produce spurious results and should not be attempted.
3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
4. Refer Section 5. Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. F-$\overline{WP}$ set to V_{IL} or V_{IH}.
6. Electricity consumption is lowest when F-$\overline{RST}$ = GND ±0.2V.

7. Flash Read Mode

Mode	Address	DQ_0 to DQ_{15}
Read Array	X	D_{OUT}
Read Identifier Codes/OTP	See 5.2, 5.3	See 5.2, 5.3
Read Query	Refer to the Appendix	Refer to the Appendix

8. SRAM Standby Mode

S-$\overline{CE}_1$	S-CE_2	S-$\overline{LB}$	S-$\overline{UB}$
H	X	X	X
X	L	X	X
X	X	H	H

9. S-$\overline{UB}$, S-$\overline{LB}$ Control Mode

S-$\overline{LB}$	S-$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}
L	L	D_{OUT}/D_{IN}	D_{OUT}/D_{IN}
L	H	D_{OUT}/D_{IN}	High-Z
H	L	High-Z	D_{OUT}/D_{IN}

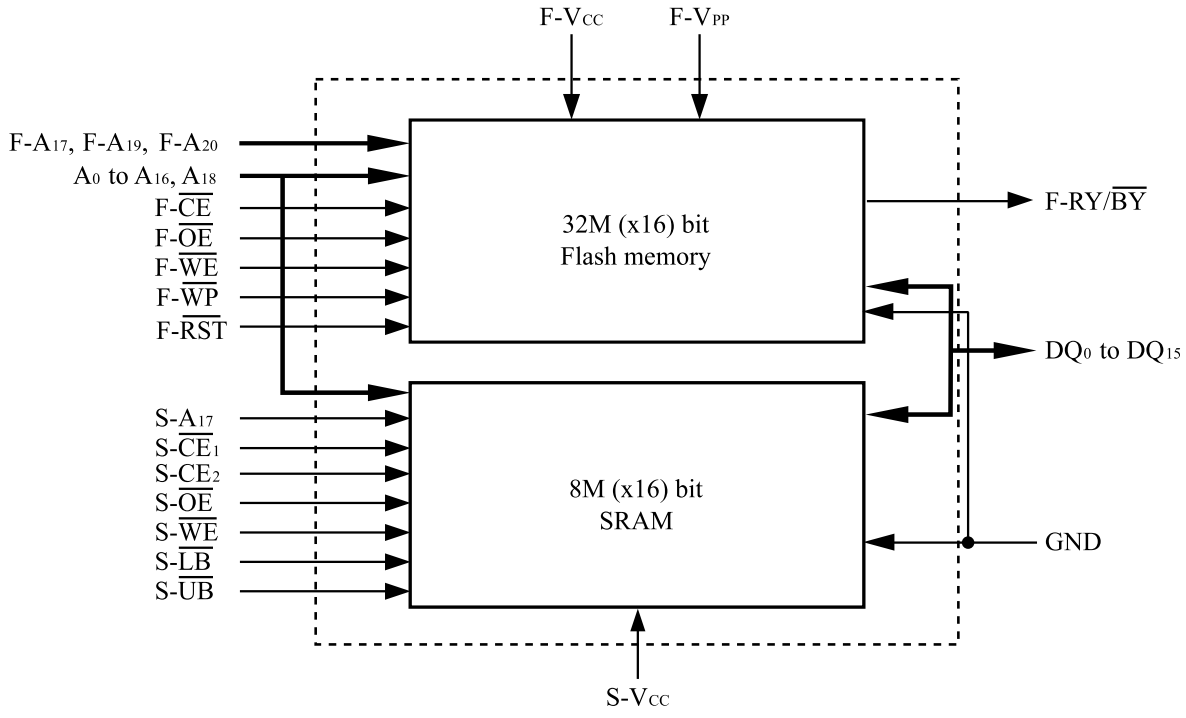
3.2 Simultaneous Operation Modes Allowed with Four Planes[1, 2]

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

Notes:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
   Only one partition can be erased or programmed at a time - no command queuing except page buffer program.
   Commands must be written to an address within the block targeted by that command.

4. Block Diagram



5. Command Definitions for Flash Memory(11)

5.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Address(2)	Data(3)	Oper(1)	Address(2)	Data(3)
Read Array	1	2	Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	2,3,4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	2,3,4	Write	PA	98H	Read	QA	QD
Read Status Register	2	2,3	Write	PA	70H	Read	PA	SRD
Clear Status Register	1	2	Write	PA	50H			
Block Erase	2	2,3,5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	2,5,9	Write	X	30H	Write	X	D0H
Program	2	2,3,5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	2,3,5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	2,8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	2,8,9	Write	PA	D0H			
Set Block Lock Bit	2	2	Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	2,10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2	2	Write	BA	60H	Write	BA	2FH
OTP Program	2	2,3,9	Write	OA	C0H	Write	OA	OD
Set Partition Configuration Register	2	2,3	Write	PCRC	60H	Write	PCRC	04H

Notes:

1. Bus operations are defined in 3.1 Bus operation.
2. First bus cycle command address should be the same as the second cycle address.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See 5.2, 5.3).
   QA=Query codes address. Refer to the LH28F320BX, LH28F640BX series Appendix for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See 5.4 OTP Block Address Map).
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes. (See 5.2, 5.3).
   QD=Data read from query database. Refer to the LH28F320BX, LH28F640BX series Appendix for details.
   SRD=Data read from status register. See 6. Status Register Definition for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   OD=Data to be programmed at location OA. Data is latched on the rising edge of F-$\overline{WE}$ or F-$\overline{CE}$ (whichever goes high first).
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code and the data within OTP block (See 5.2, 5.3).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when F-$\overline{RST}$ is V_{IH}.

6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to the LH28F320BX, LH28F640BX series Appendix for details.
8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when F-$\overline{WP}$ is V_{IL}.
    When F-$\overline{WP}$ is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

5.2 Identifier Codes and OTP Address for Read Operation

	Code	Address $[A_{15}\text{-}A_0]$(1)	Data $[DQ_{15}\text{-}DQ_0]$	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	
Device Code	32M TopParameter Device Code	0001H	00B4H	2
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	3
	Block is Locked		$DQ_0 = 1$	3
	Block is not Locked-Down		$DQ_1 = 0$	3
	Block is Locked-Down		$DQ_1 = 1$	3
Device Configuration Code	Partition Configuration Register	0006H	PCRC	4
OTP	OTP Lock	0080H	OTP-LK	5
	OTP	0081-0088H	OTP	6

Notes:

1. The address A_{20}-A_{16} to read the manufacturer, device, lock configuration, device configuration code and OTP data are shown in below table.
2. Top parameter device has its parameter blocks in the plane 3 (The highest address).
3. DQ_{15}-DQ_2 is reserved for future implementation.
4. PCRC=Partition Configuration Register Code.
5. OTP-LK=OTP Block Lock configuration.
6. OTP=OTP Block data.

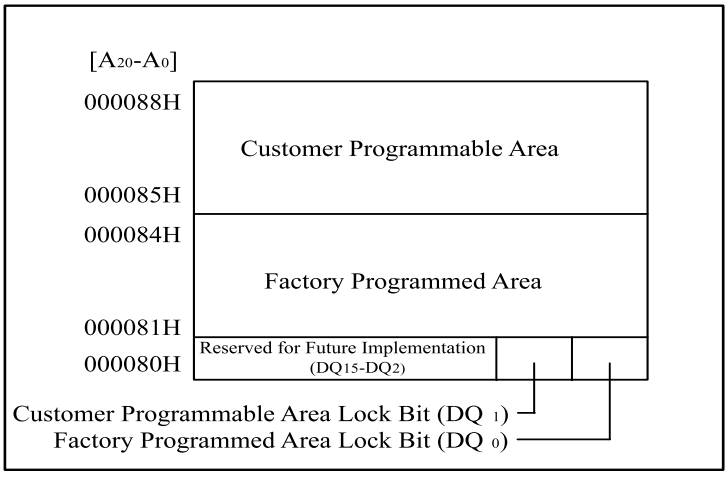
5.3 Identifier Codes and OTP Address for Read Operation on Partition Configuration(1)

Partition Configuration Register			Address (32M-bit device)
PCR.10	PCR.9	PCR.8	$[A_{20}\text{-}A_{16}]$
0	0	0	00H
0	0	1	00H or 08H
0	1	0	00H or 10H
1	0	0	00H or 18H
0	1	1	00H or 08H or 10H
1	1	0	00H or 10H or 18H
1	0	1	00H or 08H or 18H
1	1	1	00H or 08H or 10H or 18H

Notes:

1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).

5.4 OTP Block Address Map



OTP Block Address Map for OTP Program
(The area outside 80H - 88H cannot be used.)

5.5 Functions of Block Lock(1) and Block Lock-Down

Current State					Erase/Program Allowed (3)
State	F-$\overline{WP}$	DQ_1(2)	DQ_0(2)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](4)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](4)	1	0	1	Locked	No
[110](5)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Note:

1. OTP (One Time Program) block has the lock function which is different from those described above.
2. DQ_0 = 1: a block is locked; DQ_0 = 0: a block is unlocked.
   DQ_1 = 1: a block is locked-down; DQ_1 = 0: a block is not locked-down.
3. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
4. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (F-$\overline{WP}$ = 0) or [101] (F-$\overline{WP}$ = 1), regardless of the states before power-off or reset operation.
5. When F-$\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

5.6 Block Locking State Transitions upon Command Write(4)

Current State				Result after Lock Command Written (Next State)		
State	F-$\overline{WP}$	DQ_1	DQ_0	Set Lock(1)	Clear Lock(1)	Set Lock-down(1)
[000]	0	0	0	[001]	No Change	[011](2)
[001]	0	0	1	No Change(3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111](2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111](2)
[111]	1	1	1	No Change	[110]	No Change

Note:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0 = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that F-$\overline{WP}$ is not changed and fixed V_{IL} or V_{IH}.

5.7 Block Locking State Transitions upon F-$\overline{WP}$ Transition(4)

Previous State	Current State				Result after F-$\overline{WP}$ Transition (Next State)	
	State	F-$\overline{WP}$	DQ_1	DQ_0	F-$\overline{WP}$ = 0→1(1)	F-$\overline{WP}$ = 1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

Note:

1. "F-$\overline{WP}$ = 0→1" means that F-$\overline{WP}$ is driven to V_{IH} and "F-$\overline{WP}$ = 1→0" means that F-$\overline{WP}$ is driven to V_{IL}
2. State transition from the current state [011] to the next state depends on the previous state.
3. When F-$\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

6. Status Register Definition

Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
1 = Ready
0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
1 = Block Erase Suspended
0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
1 = Error in Block Erase or Full Chip Erase
0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
1 = Error in (Page Buffer) Program or OTP Program
0 = Successful (Page Buffer) Program or OTP Program

SR.3 = F-V_{PP} STATUS (VPPS)
1 = F-V_{PP} LOW Detect, Operation Abort
0 = F-V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
1 = (Page Buffer) Program Suspended
0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
1 = Erase or Program Attempted on a Locked Block, Operation Abort
0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 or F-RY/$\overline{BY}$ to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, page buffer program, set/clear block lock bit, set block lock-down bit or set read/partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of F-V_{PP} level. The WSM interrogates and indicates the F-V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when F-$V_{PP} \neq V_{PPH1/2}$ or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
1 = Page Buffer Program available
0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

After issue a Page Buffer Program command (E8H), XSR.7=1 indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

000 = No partitioning. Dual Work is not allowed.

001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)

010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.

100 = Plane 0-2 are merged into one partition. (default in a top parameter device)

011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

1. After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.
2. See the table below for more details.
3. PCR.15-11 and PCR.7-0 bits are reserved for future use. If these bits are read via the Read Identifier Codes/OTP command, the device may output "1" or "0" on these bits.

Partition Configuration

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	PARTITION0: PLANE3, PLANE2, PLANE1, PLANE0	0 1 1	PARTITION2: PLANE3, PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0
0 0 1	PARTITION1: PLANE3, PLANE2, PLANE1; PARTITION0: PLANE0	1 1 0	PARTITION2: PLANE3; PARTITION1: PLANE2, PLANE1; PARTITION0: PLANE0
0 1 0	PARTITION1: PLANE3, PLANE2; PARTITION0: PLANE1, PLANE0	1 0 1	PARTITION2: PLANE3; PARTITION1: PLANE2, PLANE1; PARTITION0: PLANE0
1 0 0	PARTITION1: PLANE3; PARTITION0: PLANE2, PLANE1, PLANE0	1 1 1	PARTITION3: PLANE3; PARTITION2: PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0

7. Memory Map for Flash Memory

Top Parameter

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (PARAMETER PLANE)	70	4K-WORD	1FF000h - 1FFFFFh
	69	4K-WORD	1FE000h - 1FEFFFh
	68	4K-WORD	1FD000h - 1FDFFFh
	67	4K-WORD	1FC000h - 1FCFFFh
	66	4K-WORD	1FB000h - 1FBFFFh
	65	4K-WORD	1FA000h - 1FAFFFh
	64	4K-WORD	1F9000h - 1F9FFFh
	63	4K-WORD	1F8000h - 1F8FFFh
	62	32K-WORD	1F0000h - 1F7FFFh
	61	32K-WORD	1E8000h - 1EFFFFh
	60	32K-WORD	1E0000h - 1E7FFFh
	59	32K-WORD	1D8000h - 1DFFFFh
	58	32K-WORD	1D0000h - 1D7FFFh
	57	32K-WORD	1C8000h - 1CFFFFh
	56	32K-WORD	1C0000h - 1C7FFFh
	55	32K-WORD	1B8000h - 1BFFFFh
	54	32K-WORD	1B0000h - 1B7FFFh
	53	32K-WORD	1A8000h - 1AFFFFh
	52	32K-WORD	1A0000h - 1A7FFFh
	51	32K-WORD	198000h - 19FFFFh
	50	32K-WORD	190000h - 197FFFh
	49	32K-WORD	188000h - 18FFFFh
	48	32K-WORD	180000h - 187FFFh
PLANE2 (UNIFORM PLANE)	47	32K-WORD	178000h - 17FFFFh
	46	32K-WORD	170000h - 177FFFh
	45	32K-WORD	168000h - 16FFFFh
	44	32K-WORD	160000h - 167FFFh
	43	32K-WORD	158000h - 15FFFFh
	42	32K-WORD	150000h - 157FFFh
	41	32K-WORD	148000h - 14FFFFh
	40	32K-WORD	140000h - 147FFFh
	39	32K-WORD	138000h - 13FFFFh
	38	32K-WORD	130000h - 137FFFh
	37	32K-WORD	128000h - 12FFFFh
	36	32K-WORD	120000h - 127FFFh
	35	32K-WORD	118000h - 11FFFFh
	34	32K-WORD	110000h - 117FFFh
	33	32K-WORD	108000h - 10FFFFh
	32	32K-WORD	100000h - 107FFFh

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	31	32K-WORD	0F8000h - 0FFFFFh
	30	32K-WORD	0F0000h - 0F7FFFh
	29	32K-WORD	0E8000h - 0EFFFFh
	28	32K-WORD	0E0000h - 0E7FFFh
	27	32K-WORD	0D8000h - 0DFFFFh
	26	32K-WORD	0D0000h - 0D7FFFh
	25	32K-WORD	0C8000h - 0CFFFFh
	24	32K-WORD	0C0000h - 0C7FFFh
	23	32K-WORD	0B8000h - 0BFFFFh
	22	32K-WORD	0B0000h - 0B7FFFh
	21	32K-WORD	0A8000h - 0AFFFFh
	20	32K-WORD	0A0000h - 0A7FFFh
	19	32K-WORD	098000h - 09FFFFh
	18	32K-WORD	090000h - 097FFFh
	17	32K-WORD	088000h - 08FFFFh
	16	32K-WORD	080000h - 087FFFh
PLANE0 (UNIFORM PLANE)	15	32K-WORD	078000h - 07FFFFh
	14	32K-WORD	070000h - 077FFFh
	13	32K-WORD	068000h - 06FFFFh
	12	32K-WORD	060000h - 067FFFh
	11	32K-WORD	058000h - 05FFFFh
	10	32K-WORD	050000h - 057FFFh
	9	32K-WORD	048000h - 04FFFFh
	8	32K-WORD	040000h - 047FFFh
	7	32K-WORD	038000h - 03FFFFh
	6	32K-WORD	030000h - 037FFFh
	5	32K-WORD	028000h - 02FFFFh
	4	32K-WORD	020000h - 027FFFh
	3	32K-WORD	018000h - 01FFFFh
	2	32K-WORD	010000h - 017FFFh
	1	32K-WORD	008000h - 00FFFFh
	0	32K-WORD	000000h - 007FFFh

8. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply voltage	1,2	-0.2 to +3.9	V
V_{IN}	Input voltage	1,2,3,4	-0.2 to V_{CC} +0.3	V
T_A	Operating temperature		-25 to +85	°C
T_{STG}	Storage temperature		-55 to +125	°C
F-V_{PP}	F-V_{PP} voltage	1,3,5	-0.2 to +12.6	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. Except F-V_{PP}.
3. -2.0V undershoot and V_{CC} +2.0V overshoot are allowed when the pulse width is less than 20 nsec.
4. V_{IN} should not be over V_{CC} +0.3V.
5. Applying 12V ±0.3V to F-V_{PP} during erase/write can only be done for a maximum of 1000 cycles on each block. F-V_{PP} may be connected to 12V ±0.3V for total of 80 hours maximum. +12.6V overshoot is allowed when the pulse width is less than 20 nsec.

9. Recommended DC Operating Conditions

(T_A = -25°C to +85°C)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3	2.7	3.0	3.3	V
V_{IH}	Input Voltage		V_{CC} -0.4 (2)		V_{CC} +0.2 (1)	V
V_{IL}	Input Voltage		-0.2		0.4	V

Notes:

1. V_{CC} is the lower of F-V_{CC} or S-V_{CC}.
2. V_{CC} is the higher of F-V_{CC} or S-V_{CC}.
3. V_{CC} includes both F-V_{CC} and S-V_{CC}.

10. Pin Capacitance(1)

(T_A = 25°C, f = 1MHz)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Condition
C_{IN}	Input capacitance				15	pF	V_{IN} = 0V
$C_{I/O}$	I/O capacitance				25	pF	$V_{I/O}$ = 0V

Note:

1. Sampled but not 100% tested.

11. DC Electrical Characteristics(1)

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
I_{LI}	Input Load Current				±2	µA	$V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current				±2	µA	$V_{OUT} = V_{CC}$ or GND
I_{CCS}	F-V_{CC} Standby Current	2		4	20	µA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = F-$\overline{RST}$ = F-V_{CC} ±0.2V, F-$\overline{WP}$ = F-V_{CC} or GND
I_{CCAS}	F-V_{CC} Automatic Power Savings Current	2,5		4	20	µA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = GND ±0.2V, F-$\overline{WP}$ = F-V_{CC} or GND
I_{CCD}	F-V_{CC} Reset Power-Down Current	2		4	20	µA	F-$\overline{RST}$ = GND ±0.2V I_{OUT}(F-RY/$\overline{BY}$) = 0mA
I_{CCR}	Average F-V_{CC} Read Current Normal Mode	2		15	25	mA	F-V_{CC} = F-V_{CC} Max., F-$\overline{CE}$ = V_{IL}, F-$\overline{OE}$ = V_{IH}, f = 5MHz I_{OUT} = 0mA
	Average F-V_{CC} Read Current Page Mode (8 Word Read)	2		5	10	mA	
I_{CCW}	F-V_{CC} (Page Buffer) Program Current	2,6		20	60	mA	F-V_{PP} = V_{PPH1}
		2,6		10	20	mA	F-V_{PP} = V_{PPH2}
I_{CCE}	F-V_{CC} Block Erase, Full Chip Erase Current	2,6		10	30	mA	F-V_{PP} = V_{PPH1}
		2,6		5	15	mA	F-V_{PP} = V_{PPH2}
I_{CCWS} I_{CCES}	F-V_{CC} (Page Buffer) Program or Block Erase Suspend Current	2,3		10	200	µA	F-$\overline{CE}$ = V_{IH}
I_{PPS} I_{PPR}	F-V_{PP} Standby or Read Current	2,7		2	5	µA	F-V_{PP} ≤ F-V_{CC}
I_{PPW}	F-V_{PP} (Page Buffer) Program Current	2,6,7		2	5	µA	F-V_{PP} = V_{PPH1}
		2,6,7		10	30	mA	F-V_{PP} = V_{PPH2}
I_{PPE}	F-V_{PP} Block Erase, Full Chip Erase Current	2,6,7		2	5	µA	F-V_{PP} = V_{PPH1}
		2,6,7		5	15	mA	F-V_{PP} = V_{PPH2}
I_{PPWS}	F-V_{PP} (Page Buffer) Program Suspend Current	2,7		2	5	µA	F-V_{PP} = V_{PPH1}
		2,7		10	200	µA	F-V_{PP} = V_{PPH2}
I_{PPES}	F-V_{PP} Block Erase Suspend Current	2,7		2	5	µA	F-V_{PP} = V_{PPH1}
		2,7		10	200	µA	F-V_{PP} = V_{PPH2}

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Typ.(1)	Max.	Unit	Conditions	
I_{SB}	S-V_{CC} Standby Current			2	25	µA	S-$\overline{CE}_1$, S-CE_2 ≥ S-V_{CC} - 0.2V or S-CE_2 ≤ 0.2V	
I_{SB1}	S-V_{CC} Standby Current				3	mA	S-CE_2 = V_{IL}	
I_{CC1}	S-V_{CC} Operation Current				50	mA	S-$\overline{CE}_1$ = V_{IL}, S-CE_2 = V_{IH} V_{IN} = V_{IL} or V_{IH}	t_{CYCL} = Min $I_{I/O}$ = 0mA
I_{CC2}	S-V_{CC} Operation Current				8	mA	S-$\overline{CE}_1$ ≤ 0.2V, S-CE_2 ≥ S-V_{CC} -0.2V, V_{IN} ≥ S-V_{CC} -0.2V or ≤ 0.2V	t_{CYCL} = 1µA $I_{I/O}$ = 0mA
V_{IL}	Input Low Voltage	6	-0.2		0.4	V		
V_{IH}	Input High Voltage	6	VCC -0.4		VCC +0.2	V		
V_{OL}	Output Low Voltage	6			0.4	V	I_{OL} = 0.5mA	
V_{OH}	Output High Voltage	6	V_{CC} -0.2			V	I_{OH} = -0.5mA	
V_{PPLK}	F-V_{PP} Lockout during Normal Operations	4,6,7			0.4	V		
V_{PPH1}	F-V_{PP} during Block Erase, Full Chip Erase, Word Write or Lock-Bit configuration Operations		1.65	3	3.3	V		
V_{PPH2}		7	11.7	12	12.3	V		
V_{LKO}	F-V_{CC} Lockout Voltage		1.5			V		

Notes:

1. V_{CC} includes both F-V_{CC} and S-V_{CC}.
2. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC} voltage and T_A=+25°C.
3. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program while in block erase suspend mode, the device's current draw is the sum of I_{CCWS} or I_{CCES} and I_{CCR} or I_{CCW}, respectively.
4. Block erase, full chip erase, (page buffer) program and OTP program are inhibited when F-V_{PP} ≤ V_{PPLK}, and not guaranteed in the range between V_{PPLK} (max.) and V_{PPH1} (min.) , between V_{PPH1} (max.) and V_{PPH2} (min.) and above V_{PPH2} (max.).
5. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
6. Sampled, not 100% tested.
7. F-V_{PP} is not used for power supply pin. With F-V_{PP} ≤ V_{PPLK}, block erase, full chip erase, (page buffer) program and OTP program cannot be executed and should not be attempted.
   Applying 12V ±0.3V to F-V_{PP} provides fast erasing or fast programming mode. In this mode, F-V_{PP} is power supply pin and supplies the memory cell current for block erasing and (page buffer) programming. Use similar power supply trace widths and layout considerations given to the V_{CC} power bus.
   Applying 12V ±0.3V to F-V_{PP} during erase/program can only be done for a maximum of 1000 cycles on each block.
   F-V_{PP} may be connected to 12V ±0.3V for a total of 80 hours maximum.

12. AC Electrical Characteristics for Flash Memory

12.1 AC Test Conditions

Input pulse level	0 V to 2.7 V
Input rise and fall time	5 ns
Input and Output timing Ref. level	1.35 V
Output load	1TTL + C_L (50pF)

12.2 Read Cycle

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		85		ns
t_{AVQV}	Address to Output Delay			85	ns
t_{ELQV}	F-$\overline{CE}$ to Output Delay	2		85	ns
t_{APA}	Page Address Access Time			30	ns
t_{GLQV}	F-$\overline{OE}$ to Output Delay	2		20	ns
t_{PHQV}	F-$\overline{RST}$ High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	F-$\overline{CE}$ or F-$\overline{OE}$ to Output in High - Z, Whichever Occurs First	1		20	ns
t_{ELQX}	F-$\overline{CE}$ to Output in Low - Z	1	0		ns
t_{GLQX}	F-$\overline{OE}$ to Output in Low - Z	1	0		ns
t_{OH}	Output Hold from First Occurring Address, F-$\overline{CE}$ or F-$\overline{OE}$ change	1	0		ns

Note:

1. Sampled, not 100% tested.
2. F-$\overline{OE}$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of F-$\overline{CE}$ without impact to t_{ELQV}.

12.3 Write Cycle (F-$\overline{WE}$ / F-$\overline{CE}$ Controlled)[1,2]

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PHWL} (t_{PHEL})	F-$\overline{RST}$ High Recovery to F-$\overline{WE}$ (F-$\overline{CE}$) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	F-$\overline{CE}$ (F-$\overline{WE}$) Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going Low	4	0		ns
t_{WLWH} (t_{ELEH})	F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width	4	60		ns
t_{DVWH} (t_{DVEH})	Data Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High	8	50		ns
t_{WHEH} (t_{EHWH})	F-$\overline{CE}$ (F-$\overline{WE}$) Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from F-$\overline{WE}$ (F-$\overline{CE}$) High		0		ns
t_{WHWL} (t_{EHEL})	F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width High	5	30		ns
t_{SHWH} (t_{SHEH})	F-$\overline{WP}$ High Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	F-V_{PP} Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVSL}	F-$\overline{WP}$ High Hold from Valid SRD, F-RY/$\overline{BY}$ High - Z	3, 6	0		ns
t_{QVVL}	F-V_{PP} Hold from Valid SRD, F-RY/$\overline{BY}$ High - Z	3, 6	0		ns
t_{WHR0} (t_{EHR0})	F-$\overline{WE}$ (F-$\overline{CE}$) High to SR.7 Going "0"	3, 7		t_{AVQV}+40	ns
t_{WHRL} (t_{EHRL})	F-$\overline{WE}$ (F-$\overline{CE}$) High to F-RY/$\overline{BY}$ Going Low	3		100	ns

Notes:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program and OTP program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
2. A write operation can be initiated and terminated with either F-$\overline{CE}$ or F-$\overline{WE}$.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last) to the rising edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first) to the falling edge of F-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. F-V_{PP} should be held at F-V_{PP}=$V_{PPH1/2}$ until determination of block erase, full chip erase, (page buffer) program or OTP program success (SR.1/3/4/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes/OTP command=t_{AVQV}+100ns.
8. See 5.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program, OTP program or lock bit configuration.

12.4 Block Erase, Full Chip Erase, (Page Buffer) Program and OTP Program Performance(4)

(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.3V)

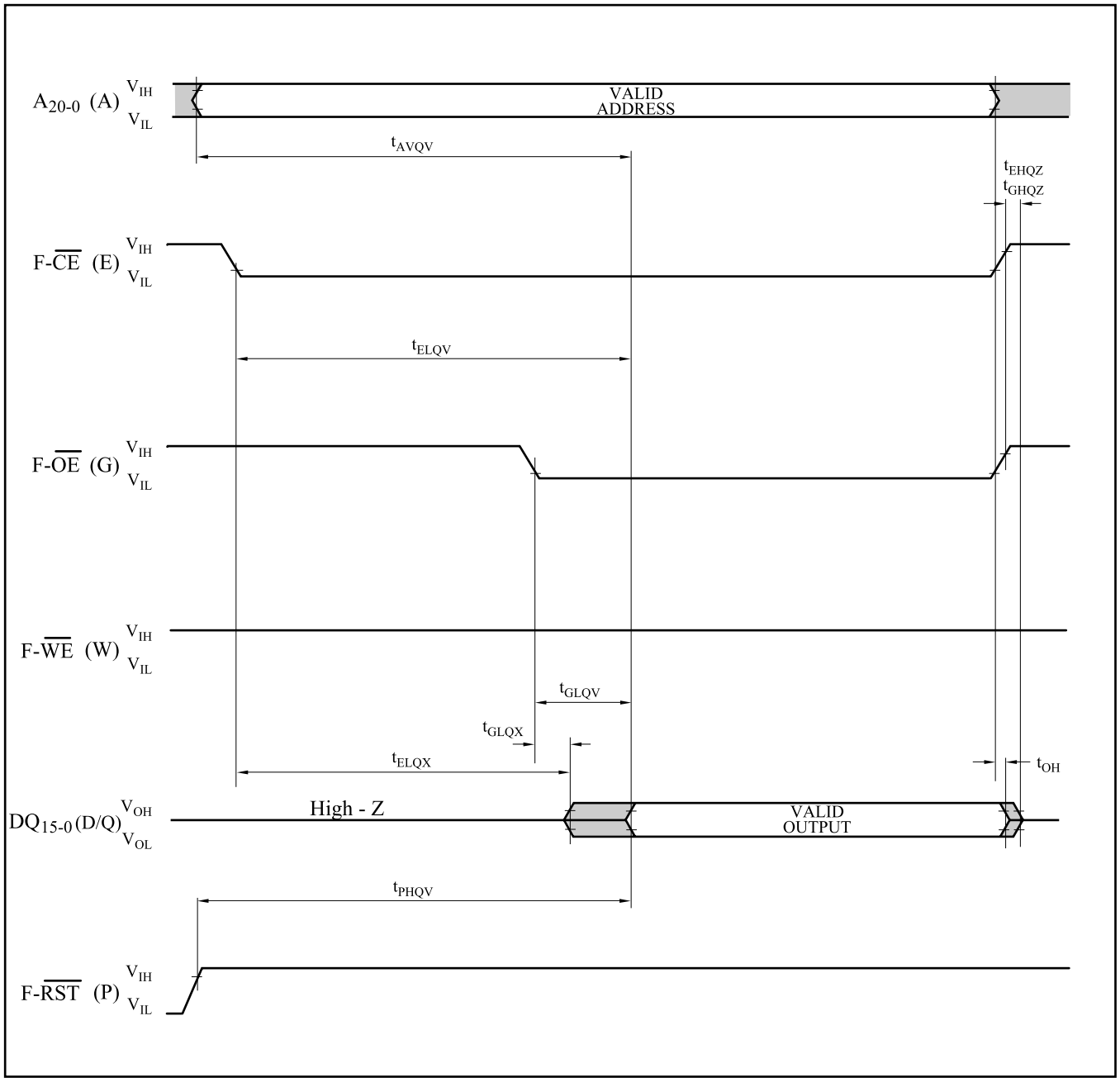
Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	F-V_{PP}=V_{PPH1} (In System)			F-V_{PP}=V_{PPH2} (In Manufacturing)			Unit
				Min.	Typ.(1)	Max.(2)	Min.	Typ.(1)	Max.(2)	
t_{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3		0.04	0.12	s
		2, 3	Used		0.03	0.12		0.02	0.06	s
t_{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4		0.31	1	s
		2, 3	Used		0.24	1		0.17	0.5	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	Not Used		11	200		9	185	µs
		2, 3	Used		7	100		5	90	µs
t_{WHOV1}/ t_{EHOV1}	OTP Program Time	2	Not Used		36	400		27	185	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4		0.2	4	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5		0.5	5	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	5	-		5	10		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	5	-		5	20		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	6	-	500			500			µs

Notes:

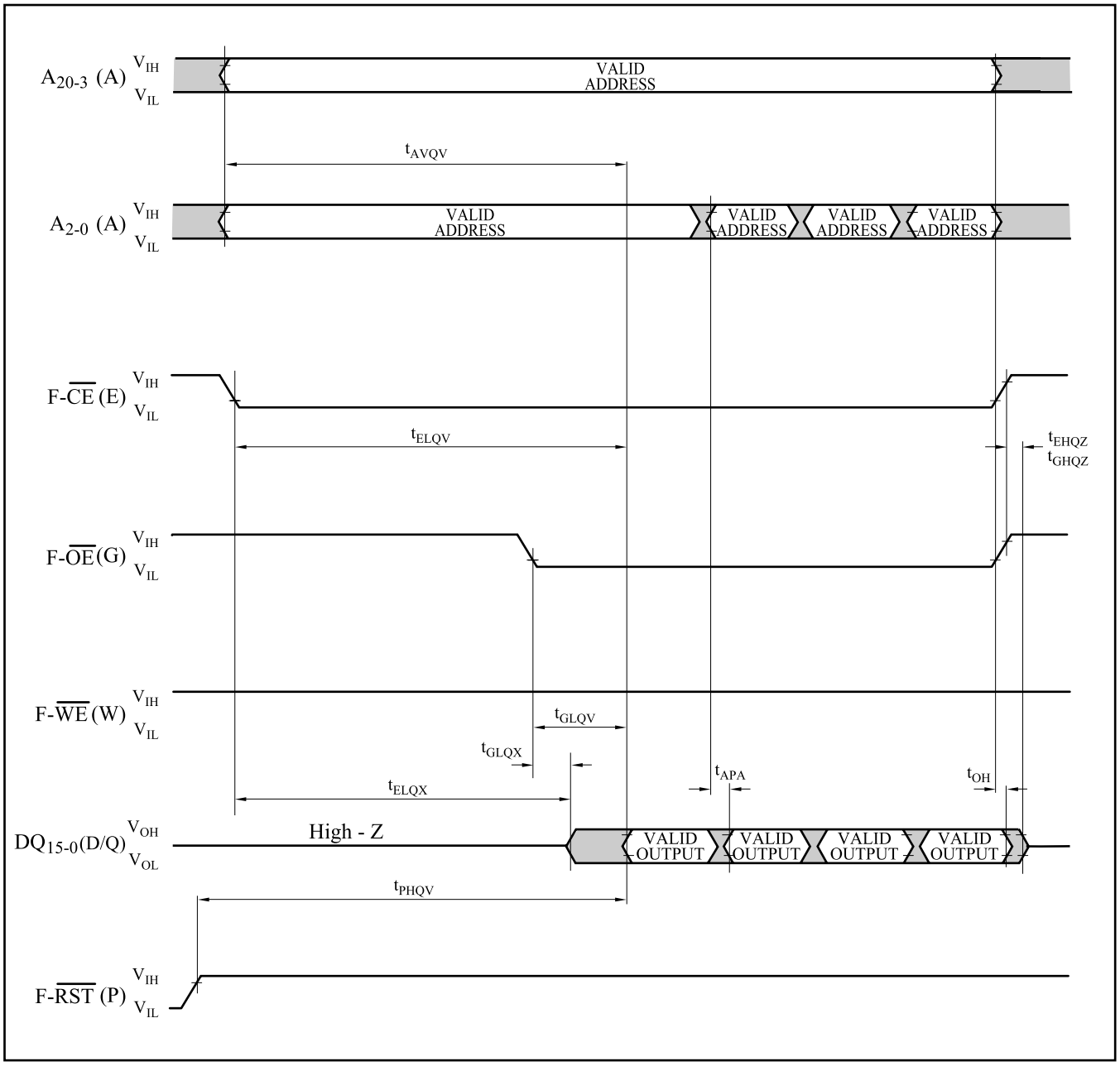
1. Typical values measured at T_A=+25°C and nominal voltages. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Every 16 words data are loaded alternatively into 2 page buffers.
4. Sampled, but not 100% tested.
5. A latency time is required from writing suspend command (F-$\overline{WE}$ or F-$\overline{CE}$ going high) until SR.7 going "1" or F-RY/$\overline{BY}$ going High-Z.
6. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

12.5 Flash Memory AC Characteristics Timing Chart

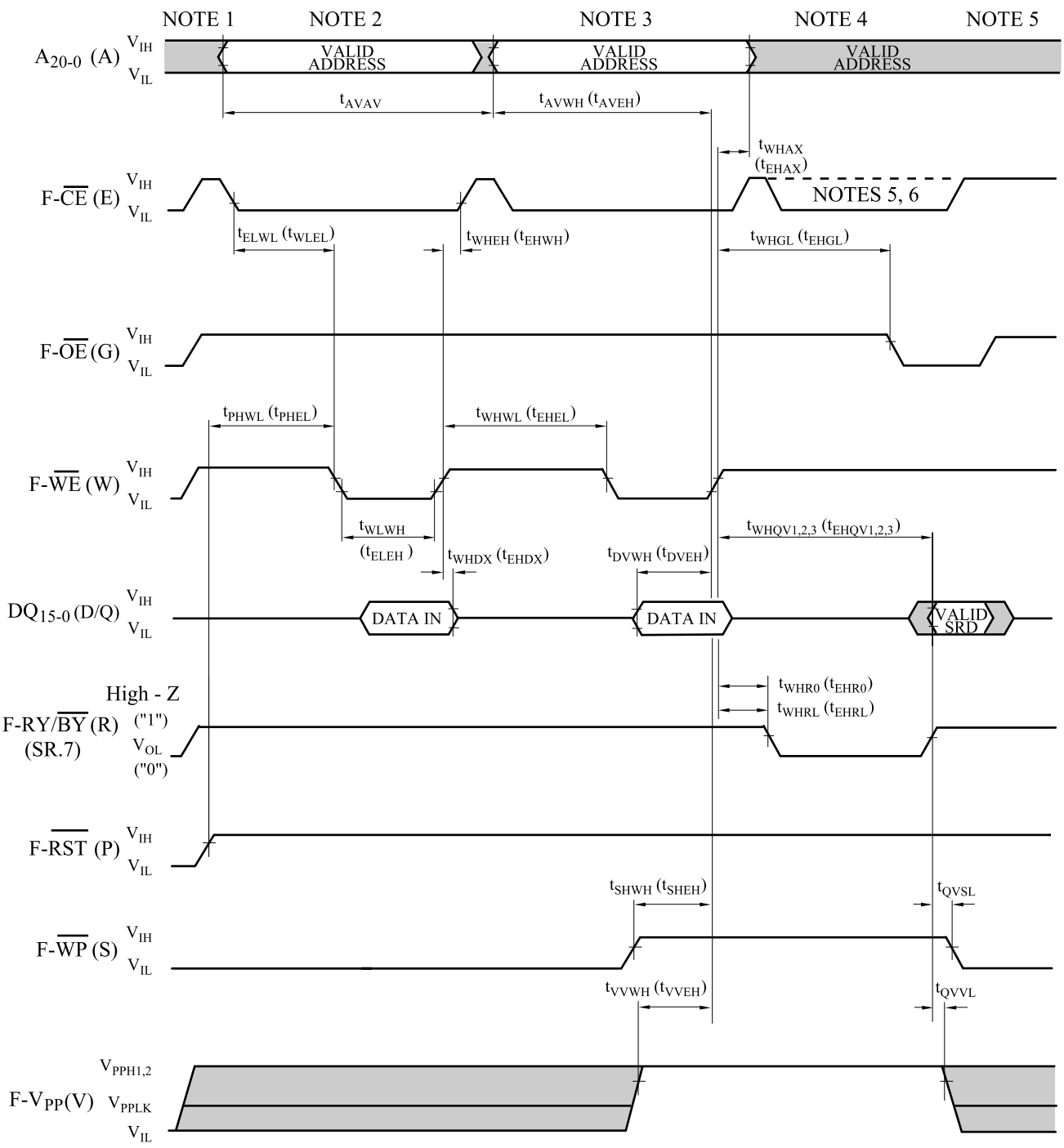
AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code



AC Waveform for Asynchronous Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Write Operations(F-$\overline{WE}$ / F-$\overline{CE}$ Controlled)



Notes:
1. F-VCC power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F-$\overline{OE}$ and F-$\overline{CE}$ must be driven active, and F-$\overline{WE}$ de-asserted.

12.6 Reset Operations[1,2]

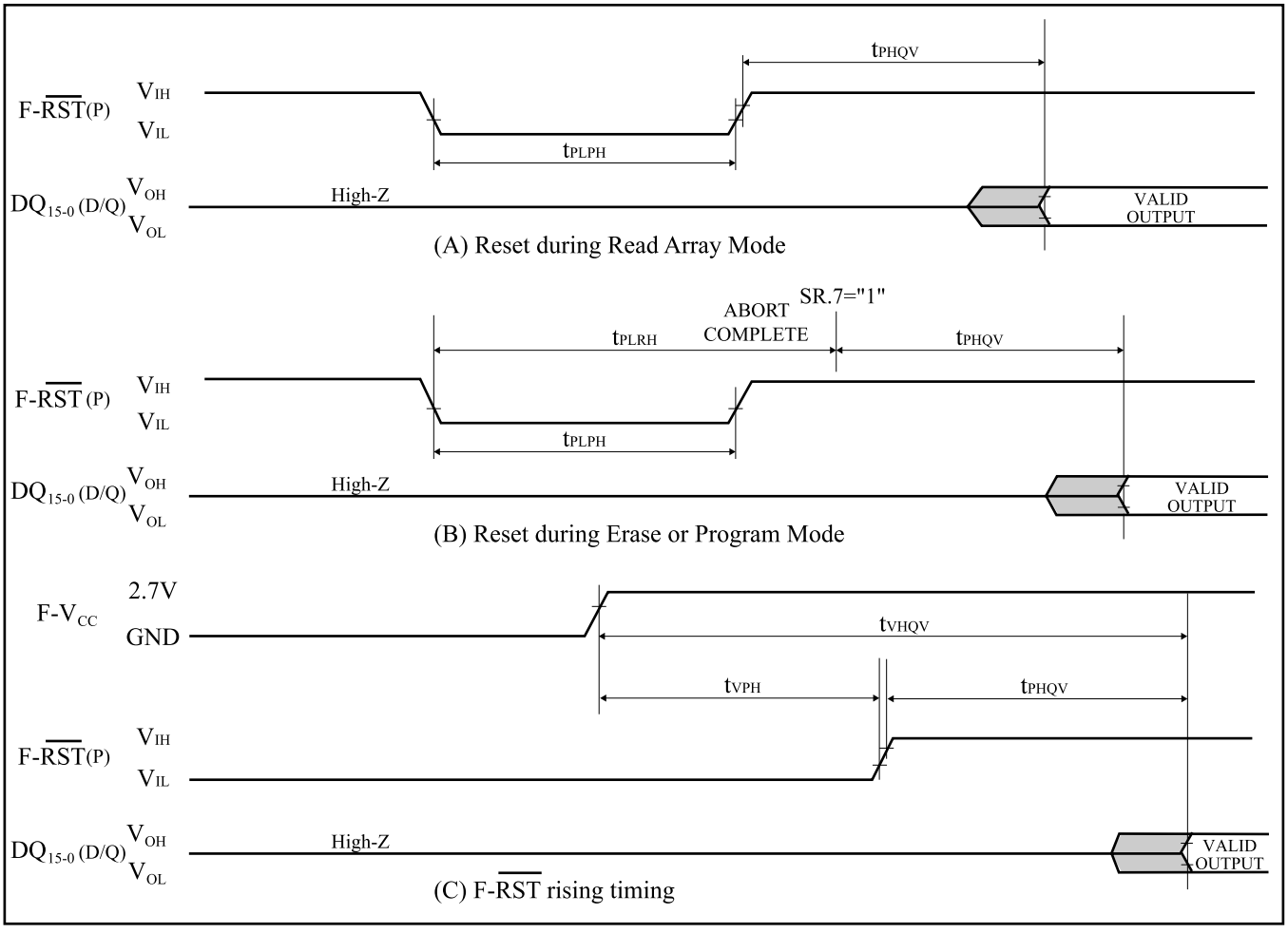
(T_A = -25°C to +85°C, F-V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	F-$\overline{RST}$ Low to Reset during Read (F-$\overline{RST}$ should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	F-$\overline{RST}$ Low to Reset during Erase or Program	1, 3, 4		22	µs
t_{VPH}	F-V_{CC} 2.7V to F-$\overline{RST}$ High	1, 3, 5	100		ns
t_{VHQV}	F-V_{CC} 2.7V to Output Delay	3		1	ms

Notes:

1. A reset time, t_{PHQV}, is required from the later of SR.7 (F-RY/$\overline{BY}$) going "1" (High-Z) or F-$\overline{RST}$ going high until outputs are valid. See the AC Characteristics - read cycle for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If F-$\overline{RST}$ asserted while a block erase, full chip erase, (page buffer) program or OTP program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding F-$\overline{RST}$ low minimum 100ns is required after F-V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



13. AC Electrical Characteristics for SRAM

13.1 AC Test Conditions

Input pulse level	0.4V to 2.2V
Input rise and fall time	5ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL + C_L (30pF)(1)

Note:

1. Including scope and socket capacitance.

13.2 Read Cycle

(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		70		ns
t_{AA}	Address access time			70	ns
t_{ACE1}	Chip enable access time (S-$\overline{CE}_1$)			70	ns
t_{ACE2}	Chip enable access time (S-CE_2)			70	ns
t_{BE}	Byte enable access time			70	ns
t_{OE}	Output enable to output valid			40	ns
t_{OH}	Output hold from address change		10		ns
t_{LZ1}	S-$\overline{CE}_1$ Low to output active	1	10		ns
t_{LZ2}	S-CE_2 High to output active	1	10		ns
t_{OLZ}	S-$\overline{OE}$ Low to output active	1	5		ns
t_{BLZ}	S-$\overline{UB}$ or S-$\overline{LB}$ Low to output active	1	5		ns
t_{HZ1}	S-$\overline{CE}_1$ High to output in High-Z	1	0	25	ns
t_{HZ2}	S-CE_2 Low to output in High-Z	1	0	25	ns
t_{OHZ}	S-$\overline{OE}$ High to output in High-Z	1	0	25	ns
t_{BHZ}	S-$\overline{UB}$ or S-$\overline{LB}$ High to output in High-Z	1	0	25	ns

Note:

1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.3 Write Cycle

(T_A = -25°C to +85°C, S-V_{CC} = 2.7V to 3.3V)

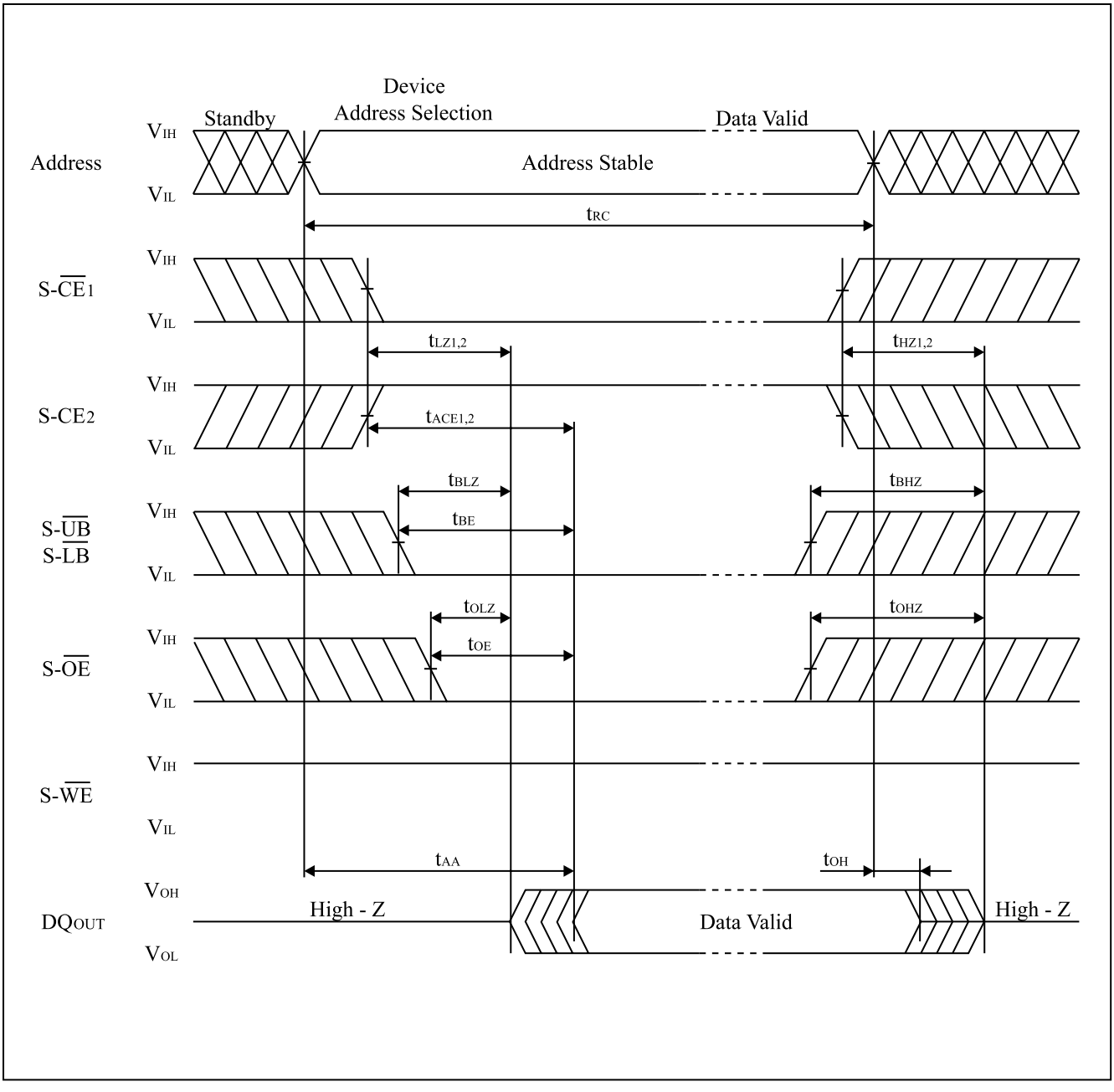
Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write cycle time		70		ns
t_{CW}	Chip enable to end of write		60		ns
t_{AW}	Address valid to end of write		60		ns
t_{BW}	Byte select time		55		ns
t_{AS}	Address setup time		0		ns
t_{WP}	Write pulse width		50		ns
t_{WR}	Write recovery time		0		ns
t_{DW}	Input data setup time		30		ns
t_{DH}	Input data hold time		0		ns
t_{OW}	S-$\overline{WE}$ High to output active	1	5		ns
t_{WZ}	S-$\overline{WE}$ Low to output in High-Z	1	0	25	ns

Note:

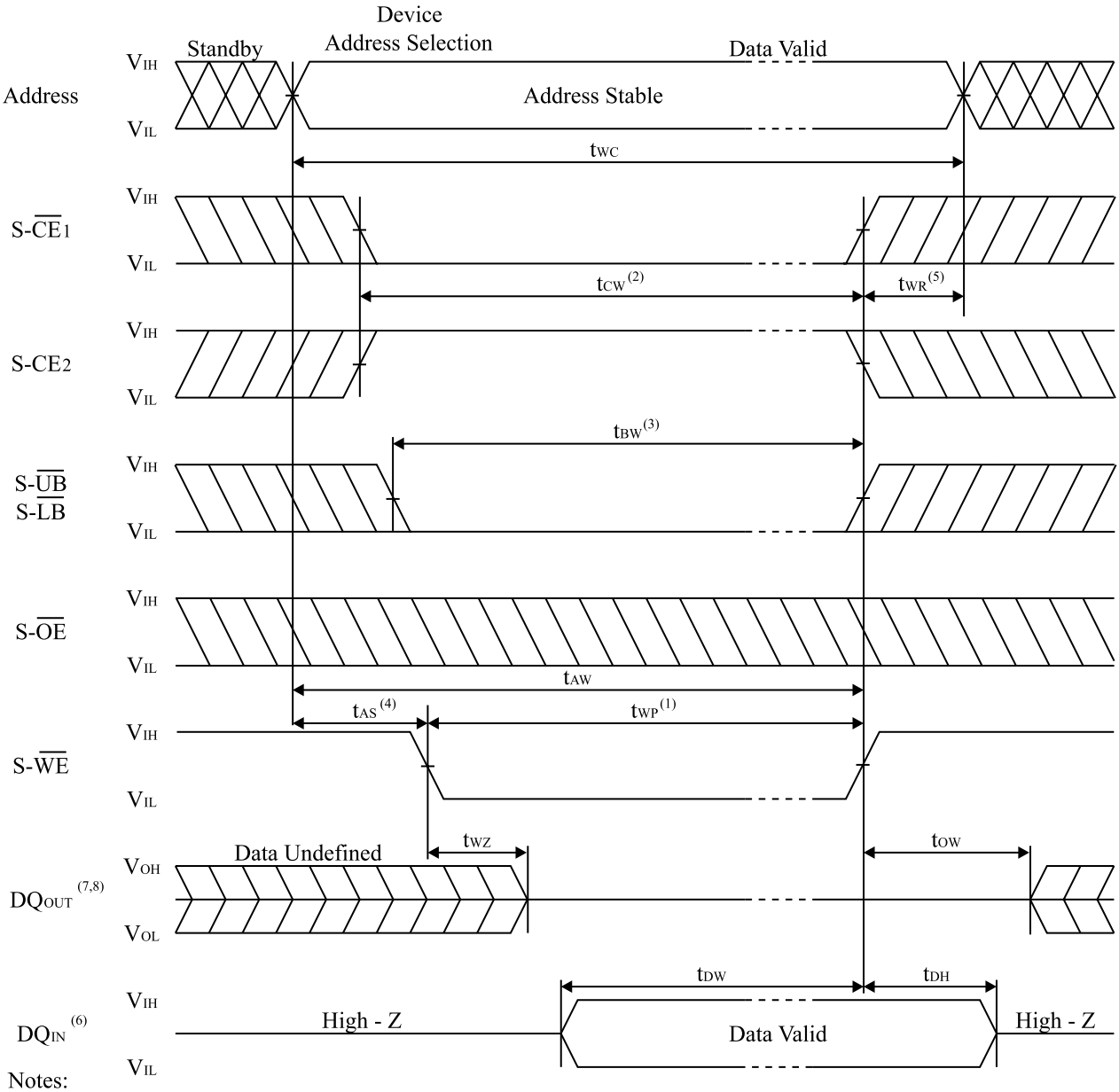
1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

13.4 SRAM AC Characteristics Timing Chart

Read Cycle Timing Chart



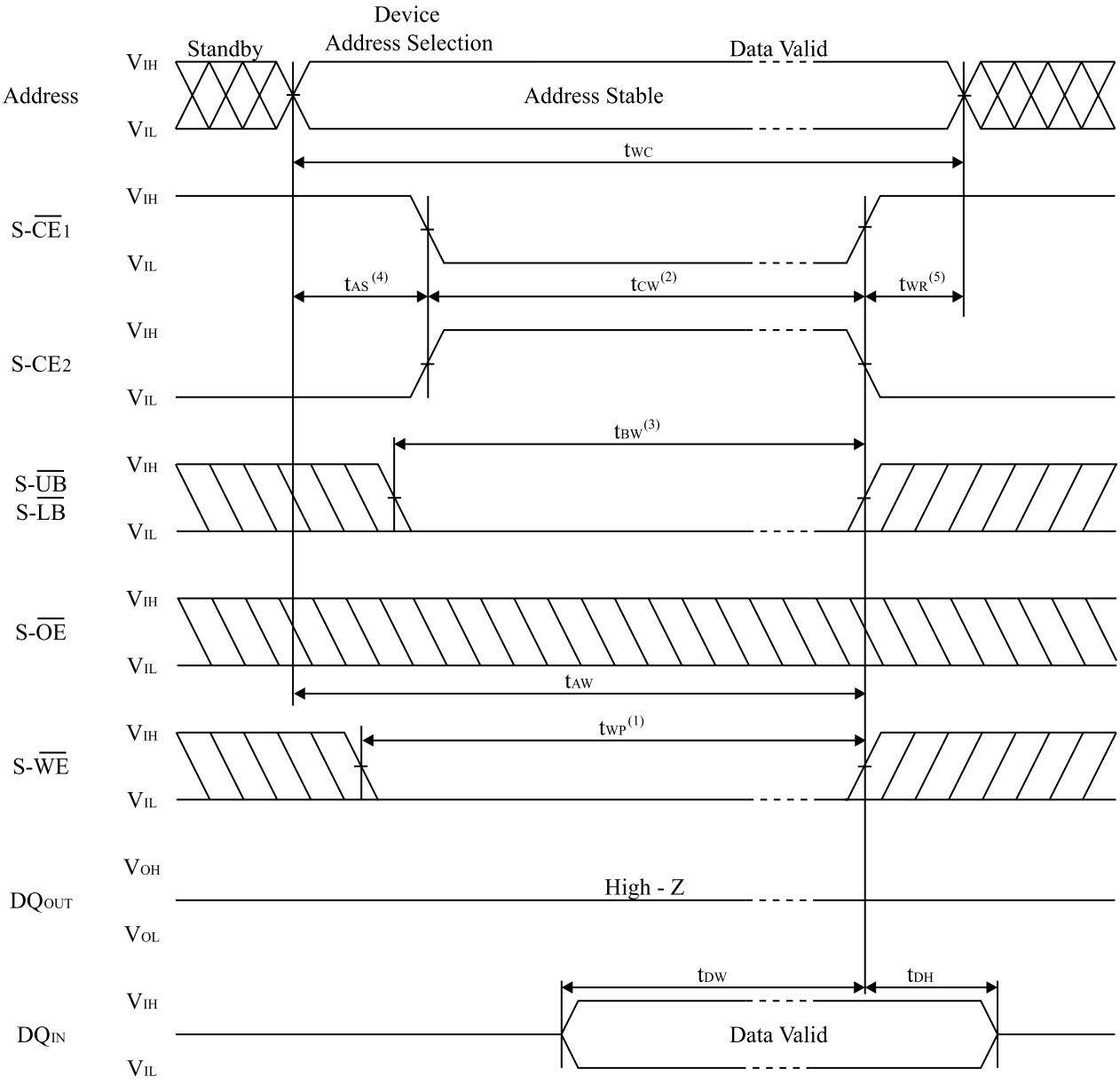
Write Cycle Timing Chart (S-$\overline{WE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S-$\overline{CE}_1$ goes low or S-CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
8. If S-$\overline{CE}_1$ goes high or S-CE_2 goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

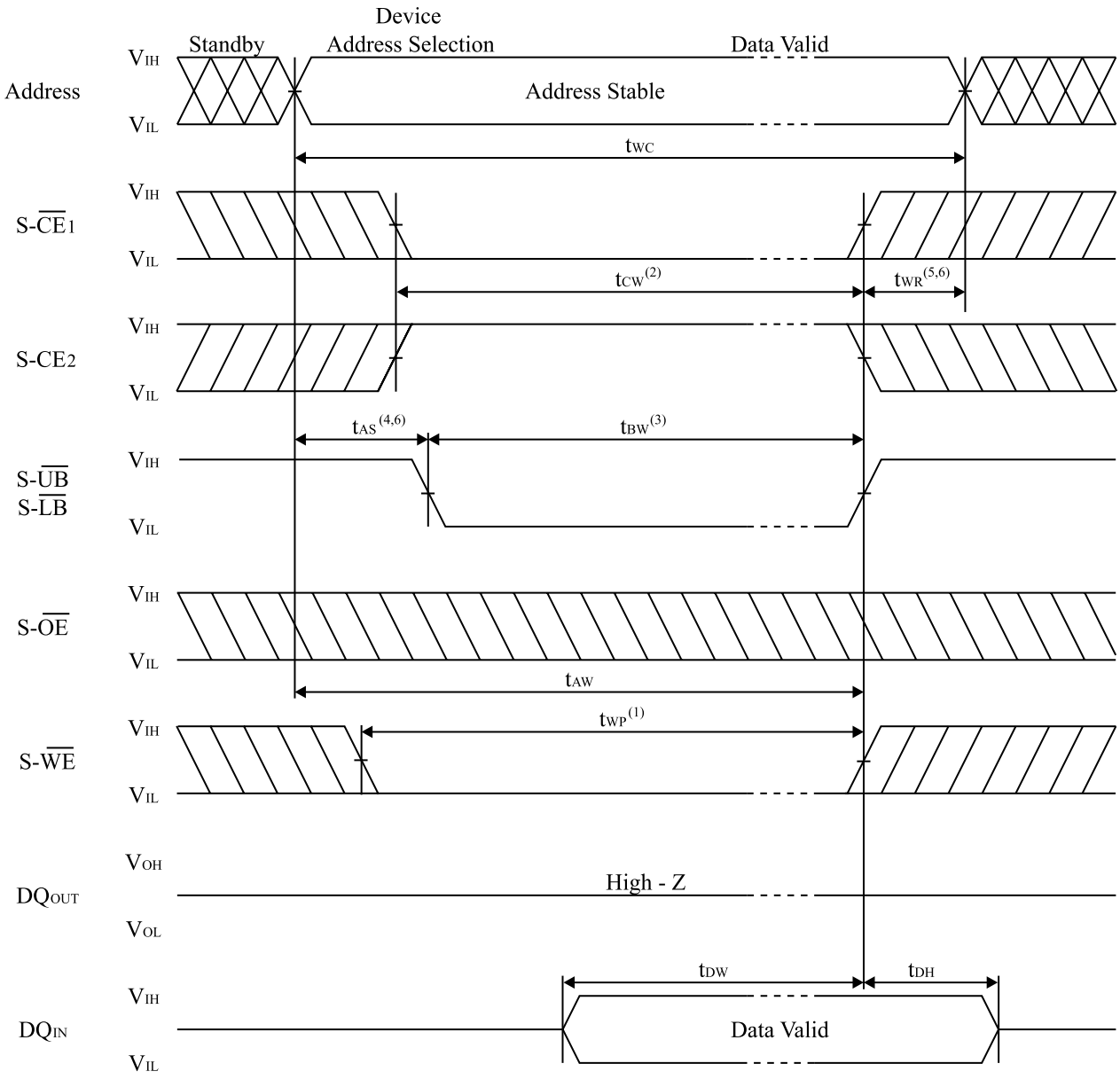
Write Cycle Timing Chart (S-$\overline{CE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.

Write Cycle Timing Chart (S-$\overline{UB}$, S-$\overline{LB}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high S-CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, S-CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, S-CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or S-CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low S-$\overline{UB}$ or low S-$\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, S-CE_2 going low or S-$\overline{WE}$ going high.
6. S-$\overline{UB}$ and S-$\overline{LB}$ need to make the time of start of a cycle, and an end "high" level for reservation of t_{AS} and t_{WR}.

14. Data Retention Characteristics for SRAM

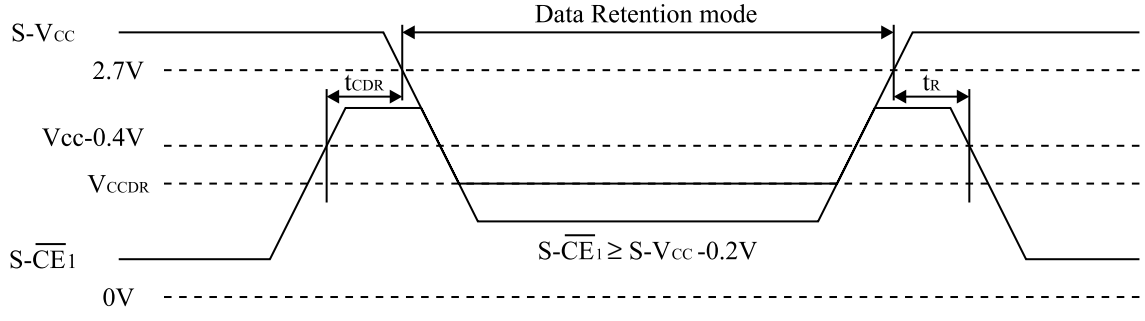
(T_A = -25°C to +85°C)

Symbol	Parameter	Note	Min.	Typ.(1)	Max.	Unit	Conditions
V_{CCDR}	Data Retention Supply voltage	2	1.5		3.3	V	S-CE_2 ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V
I_{CCDR}	Data Retention Supply current	2		2	25	µA	S-V_{CC} = 3.0V S-CE_2 ≤ 0.2V or S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V
t_{CDR}	Chip enable setup time		0			ns	
t_R	Chip enable hold time		t_{RC}			ns	

Notes

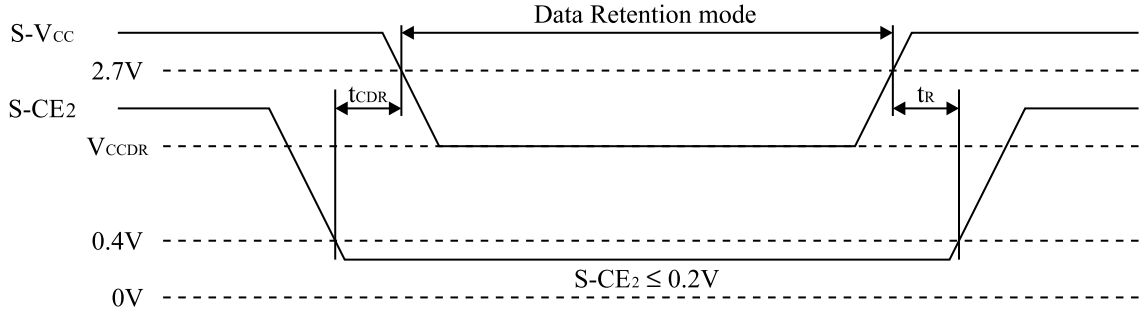
1. Reference value at T_A = 25°C, S-V_{CC} = 3.0V.
2. S-$\overline{CE}_1$ ≥ S-V_{CC} - 0.2V, S-CE_2 ≥ S-V_{CC} - 0.2V (S-$\overline{CE}_1$ controlled) or S-CE_2 ≤ 0.2V (S-CE_2 controlled).

Data Retention timing chart (S-$\overline{CE}_1$ Controlled)(1)



Note:
1. To control the data retention mode at S-$\overline{CE}_1$, fix the input level of S-CE_2 between "V_{CCDR} and V_{CCDR}-0.2V" or "0V and 0.2V" during the data retention mode.

Data Retention timing chart (S-CE_2 Controlled)



15. Notes

This product is a stacked CSP package that a 32M (x16) bit Flash Memory and a 8M (x16) bit SRAM are assembled into.

- Supply Power

  Maximum difference (between F-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

- Power Supply and Chip Enable of Flash Memory and SRAM (F-$\overline{CE}$, S-$\overline{CE}_1$, S-CE_2)

  S-$\overline{CE}_1$ should not be “low” and S-CE_2 should not be “high” when F-$\overline{CE}$ is “low” simultaneously.

  If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

  Both F-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time expect SRAM data retention mode.

- Power Up Sequence

  When turning on Flash memory power supply, keep F-$\overline{RST}$ “low”. After F-V_{CC} reaches over 2.7V, keep F-$\overline{RST}$ “low” for more than 100nsec.

- Device Decoupling

  The power supply is needed to be designed carefully because one of the SRAM and the Flash Memory is in standby mode when the other is active. A careful decoupling of power supplies is necessary between SRAM and Flash Memory. Note peak current caused by transition of control signals (F-$\overline{CE}$, S-$\overline{CE}_1$, S-CE_2).

16. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{WE}$ signal or power supply, may be interpreted as false commands, causing undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate.

■ The below describes data protection method.

1. Protecting data in specific block
   - Any locked block by setting its block lock bit is protected against the data alternation. When F-$\overline{WP}$ is V_{IL}, any locked-down block by setting its block lock-down bit is protected from lock status changes. By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
   - For detailed block locking scheme, see Chapter 5. Command definitions for Flash Memory.

2. Data Protection through F-V_{PP}
   - When the level of F-V_{PP} is lower than V_{PPLK} (lockout voltage), write operation on the flash memory is disabled. All blocks are locked and the data in the blocks are completely write protected.
   - For the lockout voltage, refer to the specification. (See Chapter 11. DC Electrical Characteristics)

■ Data Protection during voltage transition

1. Data protection thorough F-$\overline{RST}$
   - When the F-$\overline{RST}$ is kept low during power up and power down sequence, write operation on the flash memory is disabled, write protecting all blocks.
   - For the details of F-$\overline{RST}$ control, refer to the specification.
     (See Chapter 12.6 AC Electrical Characteristics for Flash Memory)

17. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory power switching characteristics, each device should have a 0.1µF ceramic capacitor connected between its F-V_{CC} and GND and between its F-V_{PP} and GND.
Low inductance capacitors should be placed as close as possible to package leads.

2. F-V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the F-V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the F-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprograming “0” for the bit which has already been programed “0”. Overwrite operation may generate unerasable bit.

In case of reprograming “0” to the data which has been programed “1”.

- Program “0” for the bit in which you want to change data from “1” to “0”.
- Program “1” for the bit which has already been programed “0”.

For example, changing data from “1011110110111101” to “1010110110111100”
requires “1110111111111110” programing.

4. Power Supply

Block erase, full chip erase, word write and lock-bit configuration with an invalid F-V_{PP}
(See Chapter 11. DC Electrical Characteristics) produce spurious results and should not be attempted.
Device operations at invalid F-V_{CC} voltage (See Chapter 11. DC Electrical Characteristics) produce spurious results and should not be attempted.

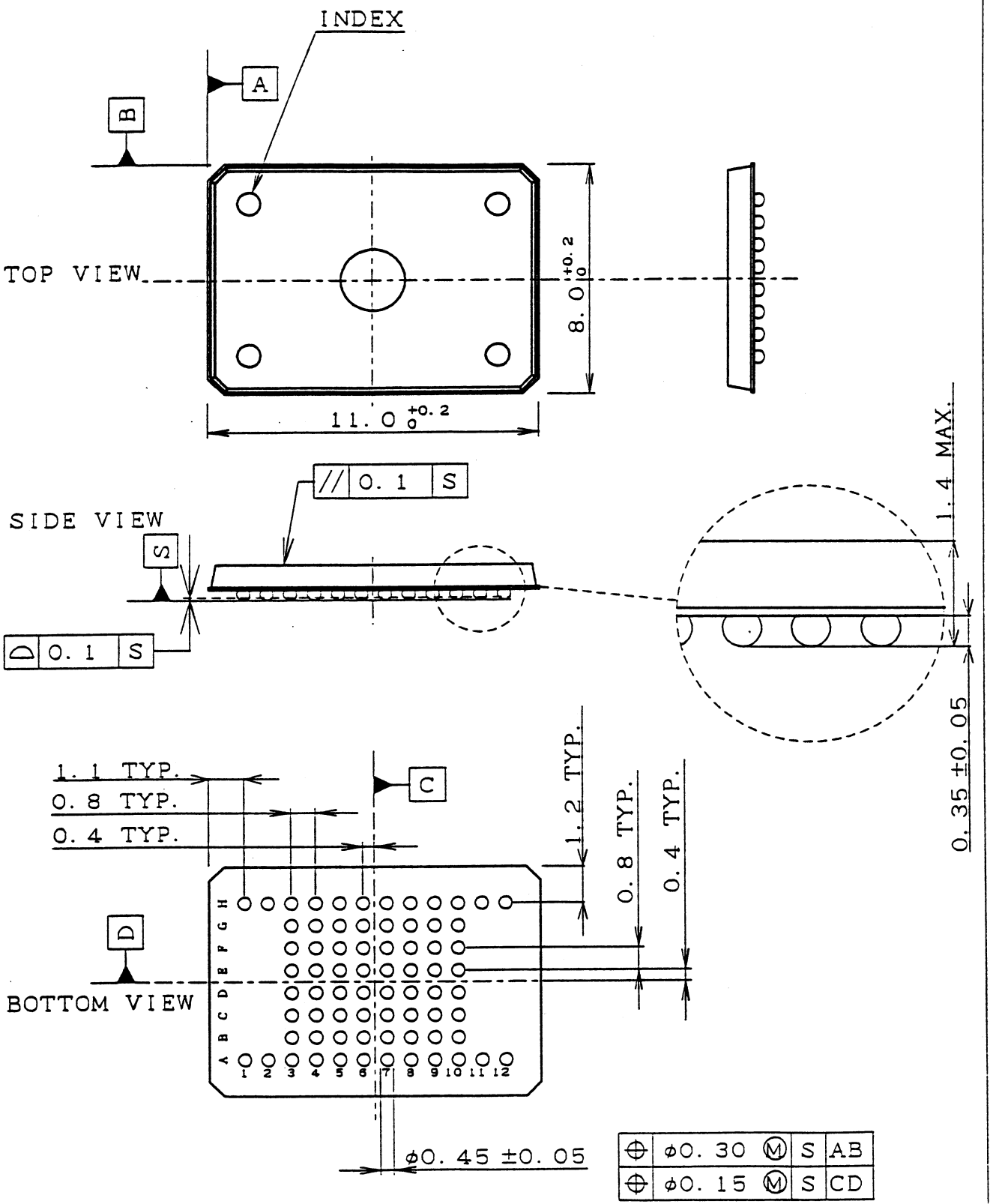
18. Related Document Information(1)

Document No.	Document Name
FUM00701	LH28F320BX, LH28F640BX Series Appendix

Note:

1. International customers should contact their local SHARP or distribution sales offices.

SHARP

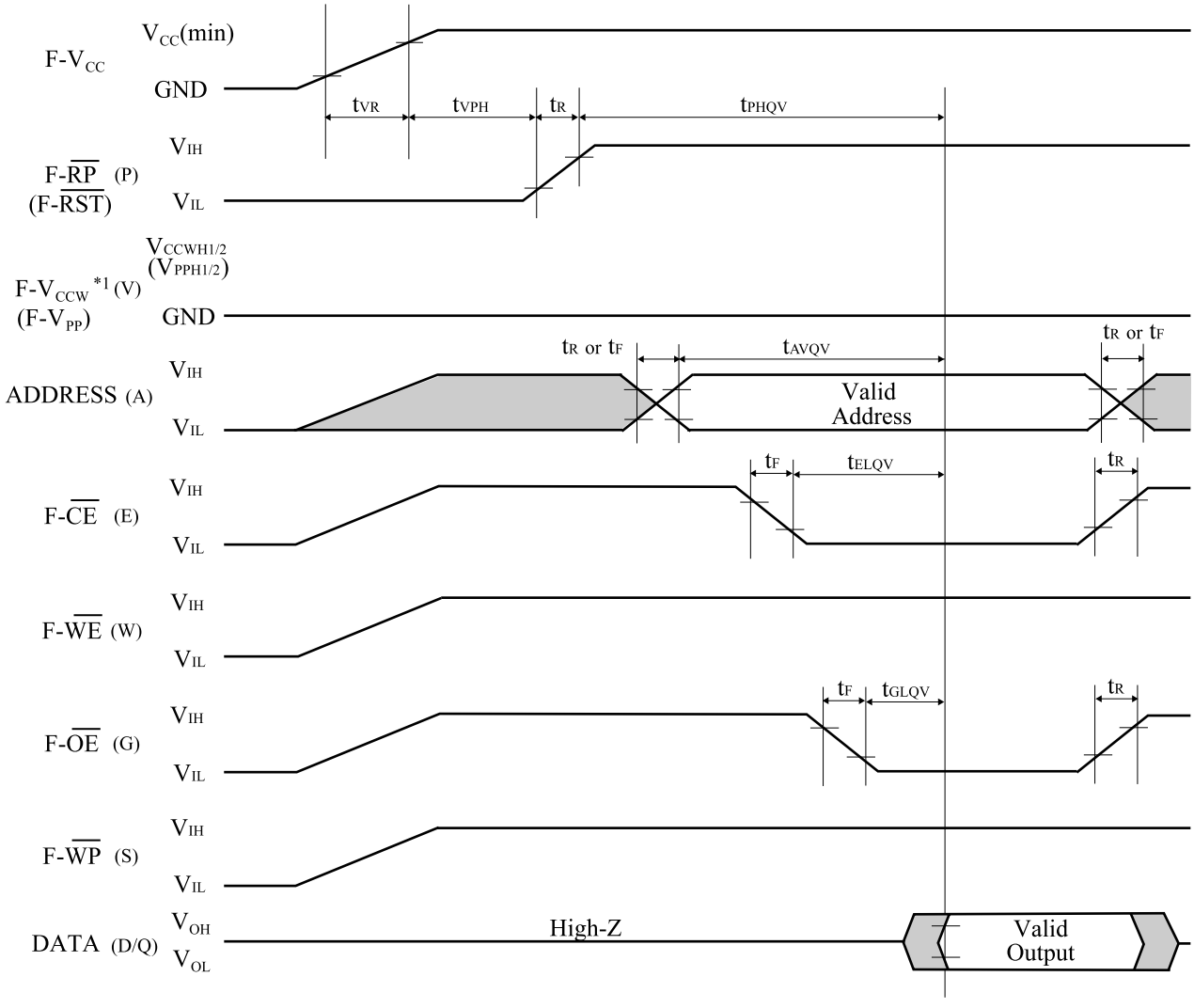


					尺度 SCALE	単位 UNIT	適用機種 APPLICABLE MODEL
					5/1	1=1/1mm	
					端子マトリクス MATRIX	12 × 8	名称 NAME: LCSP072-P-0811 (LFBGA072-P-0811)
					端子数 COUNTS	72	
改訂日 DATE	改訂記事 REVISE		担当 CHARGE		端子ピッチ PITCH	0.8	コード CODE: LCSP-GR-072-1-0811
日付 DATE	1998. 2. 10				シャープ株式会社 SHARP CORPORATION		
設計 DESIGN	製図 DRAW	写図 TRACE	検図 CHECK	承認 APPROVE	IC天理事業本部 TENRI IC GROUP		
SOTA	SOTA				超LSI開発研究所 VLSI DEVELOPMENT LABORATORIES		図番 DRAWING No.: AA2078
					生産技術開発部 PRODUCTION ENGINEERING DEPT.		

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the F-V_{CCW} (F-V_{PP}) switch, which connects F-V_{CCW} (F-V_{PP}) to GND during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the “AC Electrical Characteristics for Flash Memory“ described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	F-V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		TBD	
t_F	Input Signal Fall Time	1, 2		TBD	

NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.
   t_R (Max.) and t_F (Max.) for F-RP (F-RST) are TBD.

A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

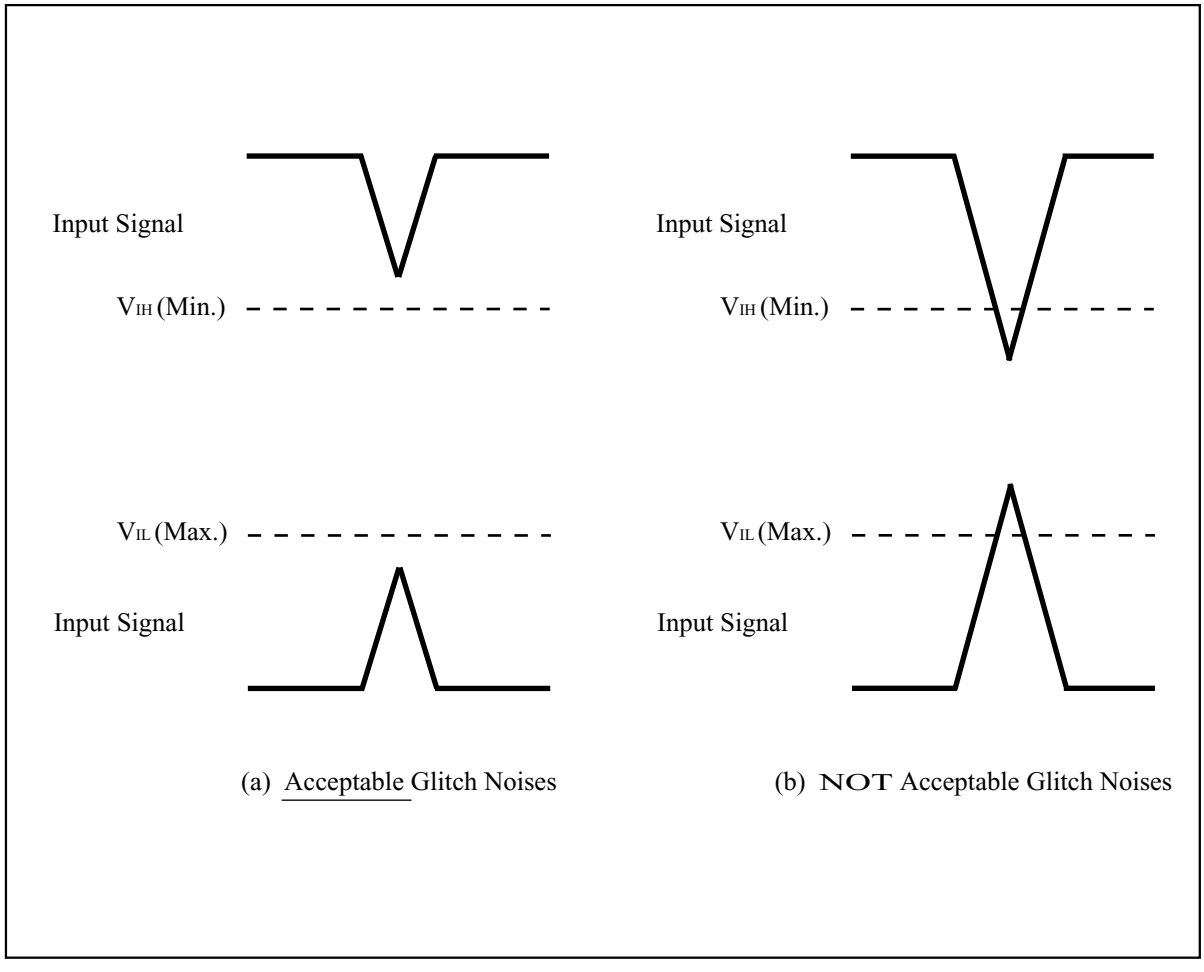


Figure A-2. Waveform for Glitch Noises

See the “DC Electrical Characteristics“ described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

A-2 RELATED DOCUMENT INFORMATION(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

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http://www.sharp.co.jp

SHARP

APPENDIX No.	FUM00701
ISSUE:	Jan. 18, 2001

Page Mode Dual Work Flash Memory

32M-bit, 64M-bit

LH28F320BX, LH28F640BX Series

Appendix

Rev. A

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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

  - Office electronics
  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliance
  - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

  - Aerospace equipment
  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
  - Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

••••• Synchronous burst mode will be available for future device.

1 Introduction

This appendix describes how to use the LH28F320BX/ LH28F640BX series, Synchronous/Page Mode Dual Work Flash memory. Section 1 outlines the LH28F320BX/LH28F640BX series. Sections 2, 3, 4 and 5 describe the memory organization and functionality. When designing a specific system, take into design considerations described in Section 5.

1.1 Features

Synchronous/Page Mode Dual Work Flash memory LH28F320BX/LH28F640BX series has the following features:

- Dual work operation
- Flexible partition configuration
- High performance asynchronous reads and synchronous burst reads
- Page buffer program
- Individual block locking and all blocks locked on power-up
- 8-word OTP (One Time Program) block
- Low power consumption
- Parameter block architecture

1.2 Definition of Block, Plane and Partition

Block, Plane and Partition are defined and used in this document as explained below.

- Block
  Main Block: 32K Words.
  Parameter Block: 4K Words.
  32M-bit device has 8 parameter blocks and 63 main blocks.
  64M-bit device has 8 parameter blocks and 127 main blocks.
- Plane: 32M-bit and 64M-bit devices are divided into four physical planes (see Table 1).
  Plane0 or Plane3 contains parameter blocks and main blocks. Plane1 and Plane2 consist of only main blocks.
- Partition: Read operation can be done in one partition while Program/Erase operation is being done in another partition. Partition contains at least one plane or up to four planes. Partition boundaries can be flexibly set to any plane boundary by the Set Partition Configuration Register command. If the partition configuration register is set to "111" (4 plane dual work mode), the partition is exactly the same as a plane. See Section 4.17 for more information.

Table 1. Address Range of Each Plane

Plane #	Contains the Blocks within the following Address	
	32M bit	64M bit
Plane 0	000000H-07FFFFH	000000H-0FFFFFH
Plane 1	080000H-0FFFFFH	100000H-1FFFFFH
Plane 2	100000H-17FFFFH	200000H-2FFFFFH
Plane 3	180000H-1FFFFFH	300000H-3FFFFFH

1.3 Product Overview

Synchronous/Page Mode Dual Work Flash memory LH28F320BX/LH28F640BX series is capable of dual work operation: erase or program operation on one partition and read operation on other partitions (see Table 2). The partition to be accessed is automatically identified according to the input address. Dual work operations can be achieved by dividing the memory array into four physical planes as shown in Figure 2.1 through Figure 3.2. Each plane is exactly one quarter of the entire memory array. The device has also virtual partitions. Several planes can be flexibly merged to one partition by writing the Set Partition Configuration Register command. This feature allows the user to read from one partition even though one of the other partitions is executing an erase or program operation. If the device is set to the 4 partitions configuration, each partition is exactly the same as each physical plane. After power-up or device reset, plane 0-2 are merged into one partition for top parameter devices and plane1-3 are merged into one partition for bottom parameter devices.

During dual work operation, read operations to the partition being erased or programmed access the status register which indicates whether the erase or program operation is successfully completed or not. Dual work operation cannot be executed during full chip erase and OTP program mode.

Memory array data can be read in two ways, that is, asynchronous 8-word page mode or synchronous burst mode. The default after power-up or device reset is the asynchronous read mode in which 8-word page mode is available. The user must set the read configuration register to enable the synchronous burst mode by writing the Set Read Configuration Register command. CLK is then used to increment the internal burst address generator, synchronize with the host, and deliver data every clock cycle. The WAIT# output pin is used to signal

••••• Synchronous burst mode will be available for future device.

that a burst is in progress. The synchronous burst feature cannot cross partition boundaries.

The LH28F320BX/LH28F640BX series contains a page buffer of 16-word × 2 plane. In the page buffer program mode, the data to be programmed is first stored into the page buffer before being transferred to the memory array. A page buffer program has high speed program performance. The page buffer program operation programs up to 16 word × 2 data at sequential addresses within one block. That is, this operation cannot be used to program data at addresses separated by something even in the same block, or divided into different blocks. Page buffer program cannot be applied to OTP block described later in this section.

For the parameter blocks and main blocks, individual block locking scheme that allows any block to be locked, unlocked or locked-down with no latency. The time required for block locking is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#). The block is locked via the Set Block Lock Bit command or Set Block Lock-down bit command. Block erase, full chip erase and (page buffer) program operation cannot be executed for locked block, to protect codes and data from unwanted operation due to noises, etc. When the WP# pin is at V_{IL}, the locked-down block cannot be unlocked. When WP# pin is at V_{IH}, lock-down bits are disabled and any block can be locked or unlocked through software. After WP# goes V_{IL}, any block previously marked lock-down revert to that state. At power-up or device reset, all blocks default to locked state and are not locked-down, regardless of the states before power-off or reset operation. This means that all write operations on any block are disabled.

Unauthorized use of cellular phone, communication device, etc. can be avoided by storing a security code into the 8-word OTP (One Time Program) block (see Figure 4) provided in addition to the parameter and main blocks. To ensure high reliability, a lock function for the OTP block is provided.

The LH28F320BX/LH28F640BX series has a V_{PP} pin which monitors the level of the power supply voltage. When $V_{PP} \leq V_{PPLK}$, memory contents cannot be altered and the data in all blocks are completely write protected (see Note 1). Note that the V_{PP} is used only for checking the supply voltage, not used for device power supply pin.

Automatic Power Savings (APS) is the low power features to help increase battery life in portable applications. APS mode is initiated shortly after read cycle completion. In this mode, its current consumption decreases to the value equivalent of that in the standby mode. Standard address access timings (t_{AVQV}) provide new data when addresses are changed. During dual work operation (one partition being erased or programmed, while other partitions are read modes), the device cannot enter the Automatic Power savings mode if the input address remains unchanged.

A CUI (Command User Interface) serves as the interface between the system processor and internal operation of the device. A valid command sequence written to the CUI initiates device automation. LH28F320BX/LH28F640BX series uses an advanced WSM (Write State Machine) to automatically execute erase and program operations within the memory array. The WSM is controlled through the CUI. By writing a valid command sequence to the CUI, the WSM is instructed to automatically handle the sequence of internal events and timings required to block erase, full chip erase, (page buffer) program or OTP program operations.

Status registers are prepared for each partition to indicate the status of the partition. Even if the WSM is occupied by executing erase or program operation in one partition, the status register of other partition reports that the device is not busy when the device is set to 2, 3 or 4 partitions configuration.

When the RST# pin is at V_{IL}, reset mode is enabled which minimizes power consumption and provides write protection. The RST# is also useful for resetting the WSM to read array mode and initializing the status register bits to "80H". During power-on/off or transitions, keep the RST# pin at V_{IL} level to protect the data from noises, and initialize the device's internal control circuit.

(Note 1) Please note following:
- For the lockout voltage V_{PPLK} to inhibit all write functions, refer to specifications.
- V_{PP} should be kept lower than V_{PPLK} (GND) during read operations to protect the data in all blocks.

A reset time (t_{PHQV}) is required from RST# switching high until outputs are valid. Likewise, the device has a wake time (t_{PHWL}, t_{PHEL}) from RST#-high until writes to the CUI are recognized.

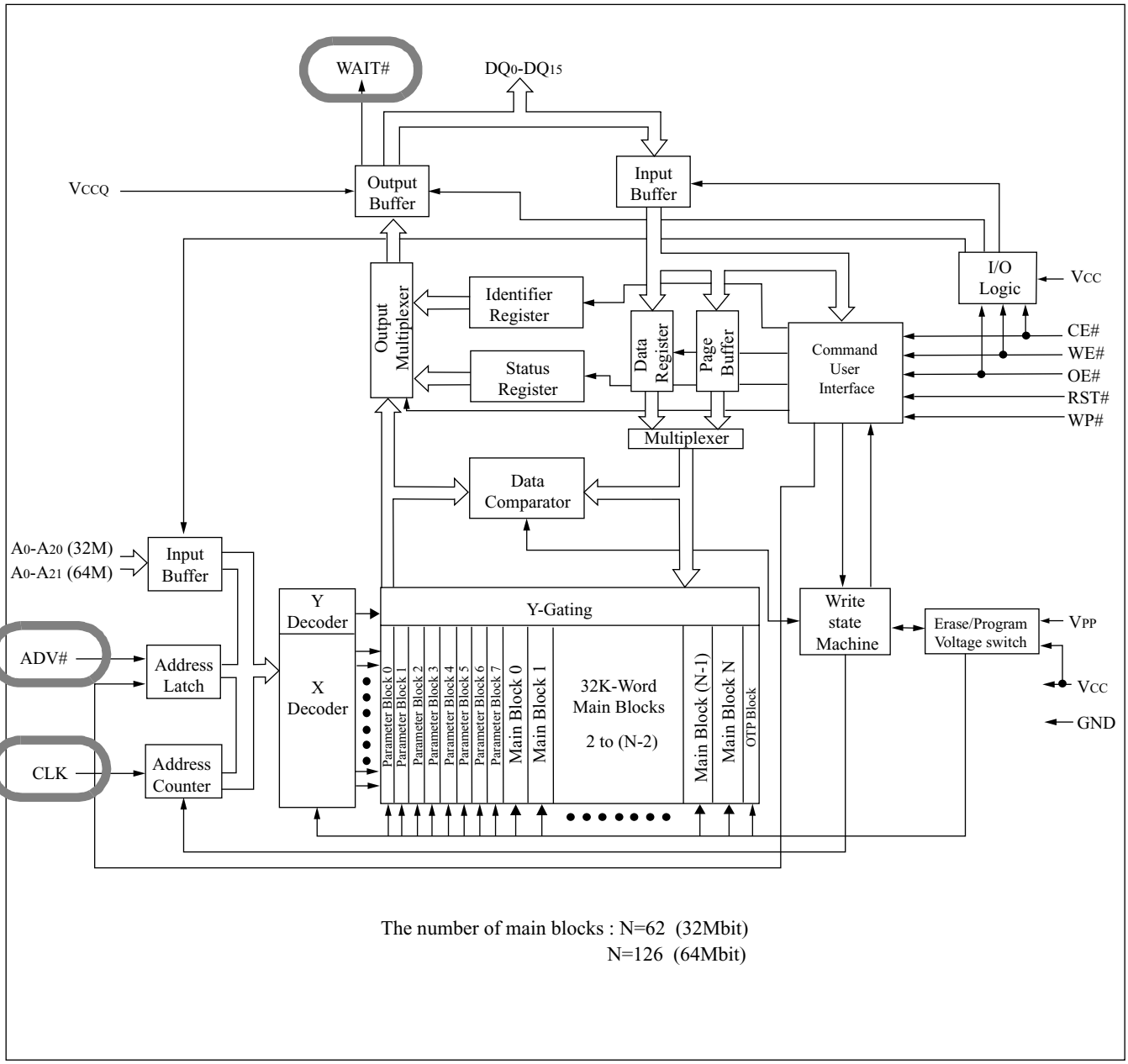
Erase operation erases one block or all blocks. Programming is executed in either one word increments or by page sized increments using the high speed program page buffers. These operations use an industry standard set of CUI command sequences. Suspend commands exist for both the erase and program operations to permit the system to interrupt an erase or program operation in progress to enable the access to another memory location in the same partition. Nested suspend is also supported. This allows the software to suspend an erase in one partition, start programming in a second partition, suspend programming in the second partition, then read from the second partition. After reading from the second partition, resume the suspended program in the second partition, then resume the suspended erase in the first partition.

Figure 1 shows the block diagram for LH28F320BX/ LH28F640BX series. The example of pin descriptions are explained in Table 3.1 and Table 3.2.

Table 2. Simultaneous Operation Modes Allowed with Four Planes(1, 2)

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:										
	Read Array	Read ID/OTP	Read Status	Read Query	Word Program	Page Buffer Program	OTP Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X		X		X	X
Read ID/OTP	X	X	X	X	X	X		X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X		X		X	X
Word Program	X	X	X	X							X
Page Buffer Program	X	X	X	X							X
OTP Program			X								
Block Erase	X	X	X	X							
Full Chip Erase			X								
Program Suspend	X	X	X	X							X
Block Erase Suspend	X	X	X	X	X	X				X	

NOTES:
1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM(Write State Machine) state - this allows a status register for each partition.
   Only one partition can be erased or programmed at a time - no command queuing except page buffer program.
   Commands must be written to an address within the block targeted by that command.
   It is not possible to do burst reads that cross partition boundaries.



The number of main blocks : N=62 (32Mbit)
N=126 (64Mbit)

Figure 1. Block Diagram

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••••• Synchronous burst mode will be available for future device.

Table 3.1. Pin Descriptions

Symbol	Type	Name and Function
A_0-A_{20}	INPUT	ADDRESS INPUTS: Inputs for addresses. 32M: A_0-A_{20}
A_0-A_{21}	INPUT	ADDRESS INPUTS: Inputs for addresses. 64M: A_0-A_{21}
DQ_0-DQ_{15}	INPUT/ OUTPUT	DATA INPUT/OUTPUTS: Inputs data and commands during CUI (Command User Interface) write cycles, outputs data during memory array, status register, query, identifier code and device configuration code reads. Data pins float to high-impedance (High Z) when the chip or outputs are deselected. Data is internally latched during an erase or program cycle.
CE#	INPUT	Chip Enable: Activates the device's control logic, input buffers, decoders and sense amplifiers. CE#-high (V_{IH}) deselects the device and reduces power consumption to standby levels.
CLK	INPUT	CLOCK: Synchronizes the memory to the system bus operating frequency in synchronous burst mode. The first rising (or falling if RCR.6 is "0") edge latches the address when ADV# is V_{IL} or upon a rising ADV# edge. This is used only for synchronous burst mode.
ADV#	INPUT	ADDRESS VALID: Addresses are input to the memory when ADV# is low (V_{IL}). Addresses are latched on ADV#'s rising edge during read and write operations.
RST#	INPUT	RESET: When low (V_{IL}), RST# resets internal automation and inhibits write operations which provides data protection. RST#-high (V_{IH}) enables normal operation. After power-up or reset mode, the device is automatically set to asynchronous read array mode. RST# must be low during power-up.
OE#	INPUT	OUTPUT ENABLE: Gates the device's outputs during a read cycle.
WE#	INPUT	WRITE ENABLE: Controls writes to the CUI and array blocks. Addresses and data are latched on the rising edge of CE# or WE# (whichever goes high first).
WP#	INPUT	WRITE PROTECT: When WP# is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When WP# is V_{IH}, lock-down is disabled.
WAIT#	OUTPUT	WAIT: Outputs data valid status in synchronous burst mode while OE# is asserted. When high (V_{OH}) during a burst mode, data is valid. WAIT# low (V_{OL}) indicates invalid data. WAIT# is pulled high (V_{OH}) by an internal resister. The WAIT# signals of the multiple devices can be tied together to drive one system WAIT# signal. WAIT# is used only for synchronous burst mode. It also works during a continuous burst mode or 4-, 8-word burst with no-wrap (RCR.3="1") mode

Table 3.2. Pin Descriptions (Continued)

V_{PP}	INPUT	MONITORING POWER SUPPLY VOLTAGE: V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program or OTP program cannot be executed and should not be attempted. Applying 12V±0.3V to V_{PP} provides fast erasing or fast programming mode. In this mode, V_{PP} is power supply pin. Applying 12V±0.3V to V_{PP} during erase/program can only be done for a maximum of 1000 cycles on each block. V_{PP} may be connected to 12V±0.3V for a total of 80 hours maximum. Use of this pin at 12V beyond these limits may reduce block cycling capability or cause permanent damage.
V_{CC}	SUPPLY	DEVICE POWER SUPPLY (see specifications): With $V_{CC} \leq V_{LKO}$, all write attempts to the flash memory are inhibited. Device operations at invalid V_{CC} voltage (see DC Characteristics) produce spurious results and should not be attempted.
V_{CCQ}	SUPPLY	INPUT/OUTPUT POWER SUPPLY (see specifications): Power supply for all input/output pins.
GND	SUPPLY	GROUND: Do not float any ground pins.
NC		NO CONNECT: Lead is not internally connected; it may be driven or floated.

1.4 Product Description

1.4.1 Memory Block Organization

The device is divided into four physical planes and the partitions can be flexibly configured by the Set Partition Configuration Register command. This allows dual work operations, that is, simultaneous read-while-erase and read-while-program operations. For the address locations of the blocks, see the memory map in Figure 2.1 through Figure 3.2.

1.4.2 Four Physical Planes

LH28F320BX/LH28F640BX series has four physical planes (one parameter plane and three uniform planes). Each plane consists of 8M-bit (32M-bit device) or 16M-bit (64M-bit device) Flash memory. The parameter plane consists of eight 4K-word parameter blocks and fifteen (32M-bit device) or thirty-one (64M-bit device) 32K-word main blocks. Each uniform plane consists of sixteen (32M-bit device) or thirty-two (64M-bit device) 32K-word main blocks. Each block can be erased independently up to 100,000 times.

1.4.3 Partition

Partition boundaries can be configured by the Set Partition Configuration Register command. Dual work operation can be done in two partitions. See partition configuration in Table 17 and Figure 17 for more detail. Only one partition can be erased or programmed at a time and burst reads cannot cross partition boundaries. Simultaneous operation modes are shown in Table 2.

1.4.4 Parameter Block

Eight 4K-word parameter blocks within the parameter partition are provided as the memory area to facilitate storage of frequently update small parameters that would normally be stored in EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated. The protection of the parameter block is controlled using a combination of the V_{PP}, RST#, WP#, block lock bit and block lock-down bit.

1.4.5 Main Block

32K-word main blocks can store code and/or data. The protection of the main block is also controlled using a combination of the V_{PP}, RST#, WP#, block lock bit and block lock-down bit.

1.4.6 OTP (One Time Program) block

The OTP block is a special block that cannot be erased in order to secure the high system reliability. This 8-word (128-bit) OTP block is independent of the 32M-bit or 64M-bit memory area. Figure 4 shows the OTP block address map.

The OTP block is divided into two areas. One is a factory programmed area where a unique number has been programmed in SHARP factory. This factory programmed area is "READ ONLY" (already locked). The other is a customer programmable area that can be available for customers. This customer programmable area can also be locked. After locking, this customer programmable area is protected permanently.

The data within the OTP block can be read by the Read Identifier Codes/OTP command (90H). To return to read array mode, write the Read Array command (FFH) to the CUI.

The OTP block bits are programmed by writing the OTP Program command (C0H) to the CUI. Write the OTP Program command (C0H) at the 1st command cycle and then write the address and the data at the 2nd cycle. If the OTP program operation is failed, the status register bit SR.4 is set to "1". If the OTP block is locked, the status register bits SR.4 and SR.1 are set to "1".

The OTP block can be locked using the OTP Program command (C0H). Write the OTP Program command (C0H) at the 1st command cycle and then write the data (FFFDH) to the lock location (80H) at the 2nd cycle. Read cycle from address (80H) indicates the lockout state of the OTP block. Bit 0 of address (80H) means the factory programmed area lock state ("1" is "NOT LOCKED" and "0" is "LOCKED"). Bit 1 of address (80H) means the customer programmable lock state. OTP block lockout state is not reversible. Unlike the main array block lock configuration, the lock state of the OTP block is kept unchanged even if the power is turned off or reset operation is performed.

The OTP Program command is only available for programming the OTP block. Page buffer program operations are available for the main array. OTP program cannot be suspended through the (Page Buffer) Program Suspend command (described later). Dual work operation cannot be executed during OTP program.

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (PARAMETER PLANE)	70	4K-WORD	1FF000h - 1FFFFFh
	69	4K-WORD	1FE000h - 1FEFFFh
	68	4K-WORD	1FD000h - 1FDFFFh
	67	4K-WORD	1FC000h - 1FCFFFh
	66	4K-WORD	1FB000h - 1FBFFFh
	65	4K-WORD	1FA000h - 1FAFFFh
	64	4K-WORD	1F9000h - 1F9FFFh
	63	4K-WORD	1F8000h - 1F8FFFh
	62	32K-WORD	1F0000h - 1F7FFFh
	61	32K-WORD	1E8000h - 1EFFFFh
	60	32K-WORD	1E0000h - 1E7FFFh
	59	32K-WORD	1D8000h - 1DFFFFh
	58	32K-WORD	1D0000h - 1D7FFFh
	57	32K-WORD	1C8000h - 1CFFFFh
	56	32K-WORD	1C0000h - 1C7FFFh
	55	32K-WORD	1B8000h - 1BFFFFh
	54	32K-WORD	1B0000h - 1B7FFFh
	53	32K-WORD	1A8000h - 1AFFFFh
	52	32K-WORD	1A0000h - 1A7FFFh
	51	32K-WORD	198000h - 19FFFFh
	50	32K-WORD	190000h - 197FFFh
	49	32K-WORD	188000h - 18FFFFh
	48	32K-WORD	180000h - 187FFFh
PLANE2 (UNIFORM PLANE)	47	32K-WORD	178000h - 17FFFFh
	46	32K-WORD	170000h - 177FFFh
	45	32K-WORD	168000h - 16FFFFh
	44	32K-WORD	160000h - 167FFFh
	43	32K-WORD	158000h - 15FFFFh
	42	32K-WORD	150000h - 157FFFh
	41	32K-WORD	148000h - 14FFFFh
	40	32K-WORD	140000h - 147FFFh
	39	32K-WORD	138000h - 13FFFFh
	38	32K-WORD	130000h - 137FFFh
	37	32K-WORD	128000h - 12FFFFh
	36	32K-WORD	120000h - 127FFFh
	35	32K-WORD	118000h - 11FFFFh
	34	32K-WORD	110000h - 117FFFh
	33	32K-WORD	108000h - 10FFFFh
	32	32K-WORD	100000h - 107FFFh

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	31	32K-WORD	0F8000h - 0FFFFFh
	30	32K-WORD	0F0000h - 0F7FFFh
	29	32K-WORD	0E8000h - 0EFFFFh
	28	32K-WORD	0E0000h - 0E7FFFh
	27	32K-WORD	0D8000h - 0DFFFFh
	26	32K-WORD	0D0000h - 0D7FFFh
	25	32K-WORD	0C8000h - 0CFFFFh
	24	32K-WORD	0C0000h - 0C7FFFh
	23	32K-WORD	0B8000h - 0BFFFFh
	22	32K-WORD	0B0000h - 0B7FFFh
	21	32K-WORD	0A8000h - 0AFFFFh
	20	32K-WORD	0A0000h - 0A7FFFh
	19	32K-WORD	098000h - 09FFFFh
	18	32K-WORD	090000h - 097FFFh
	17	32K-WORD	088000h - 08FFFFh
	16	32K-WORD	080000h - 087FFFh
PLANE0 (UNIFORM PLANE)	15	32K-WORD	078000h - 07FFFFh
	14	32K-WORD	070000h - 077FFFh
	13	32K-WORD	068000h - 06FFFFh
	12	32K-WORD	060000h - 067FFFh
	11	32K-WORD	058000h - 05FFFFh
	10	32K-WORD	050000h - 057FFFh
	9	32K-WORD	048000h - 04FFFFh
	8	32K-WORD	040000h - 047FFFh
	7	32K-WORD	038000h - 03FFFFh
	6	32K-WORD	030000h - 037FFFh
	5	32K-WORD	028000h - 02FFFFh
	4	32K-WORD	020000h - 027FFFh
	3	32K-WORD	018000h - 01FFFFh
	2	32K-WORD	010000h - 017FFFh
	1	32K-WORD	008000h - 00FFFFh
	0	32K-WORD	000000h - 007FFFh

Figure 2.1. Memory Map for LH28F320BX series (Top Parameter)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	70	32K-WORD	1F8000h - 1FFFFFh
	69	32K-WORD	1F0000h - 1F7FFFh
	68	32K-WORD	1E8000h - 1EFFFFh
	67	32K-WORD	1E0000h - 1E7FFFh
	66	32K-WORD	1D8000h - 1DFFFFh
	65	32K-WORD	1D0000h - 1D7FFFh
	64	32K-WORD	1C8000h - 1CFFFFh
	63	32K-WORD	1C0000h - 1C7FFFh
	62	32K-WORD	1B8000h - 1BFFFFh
	61	32K-WORD	1B0000h - 1B7FFFh
	60	32K-WORD	1A8000h - 1AFFFFh
	59	32K-WORD	1A0000h - 1A7FFFh
	58	32K-WORD	198000h - 19FFFFh
	57	32K-WORD	190000h - 197FFFh
	56	32K-WORD	188000h - 18FFFFh
	55	32K-WORD	180000h - 187FFFh
PLANE2 (UNIFORM PLANE)	54	32K-WORD	178000h - 17FFFFh
	53	32K-WORD	170000h - 177FFFh
	52	32K-WORD	168000h - 16FFFFh
	51	32K-WORD	160000h - 167FFFh
	50	32K-WORD	158000h - 15FFFFh
	49	32K-WORD	150000h - 157FFFh
	48	32K-WORD	148000h - 14FFFFh
	47	32K-WORD	140000h - 147FFFh
	46	32K-WORD	138000h - 13FFFFh
	45	32K-WORD	130000h - 137FFFh
	44	32K-WORD	128000h - 12FFFFh
	43	32K-WORD	120000h - 127FFFh
	42	32K-WORD	118000h - 11FFFFh
	41	32K-WORD	110000h - 117FFFh
	40	32K-WORD	108000h - 10FFFFh
	39	32K-WORD	100000h - 107FFFh

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	38	32K-WORD	0F8000h - 0FFFFFh
	37	32K-WORD	0F0000h - 0F7FFFh
	36	32K-WORD	0E8000h - 0EFFFFh
	35	32K-WORD	0E0000h -0E7FFFh
	34	32K-WORD	0D8000h - 0DFFFFh
	33	32K-WORD	0D0000h - 0D7FFFh
	32	32K-WORD	0C8000h - 0C7FFFh
	31	32K-WORD	0B8000h - 0BFFFFh
	30	32K-WORD	0B0000h - 0B7FFFh
	29	32K-WORD	0A8000h - 0AFFFFh
	28	32K-WORD	0A0000h - 0A7FFFh
	27	32K-WORD	098000h - 09FFFFh
	26	32K-WORD	098000h - 09FFFFh
	25	32K-WORD	090000h - 097FFFh
	24	32K-WORD	088000h -08FFFFh
	23	32K-WORD	080000h - 087FFFh
PLANE0 (PARAMETER PLANE)	22	32K-WORD	078000h -07FFFFh
	21	32K-WORD	070000h - 077FFFh
	20	32K-WORD	068000h - 06FFFFh
	19	32K-WORD	060000h - 067FFFh
	18	32K-WORD	058000h - 05FFFFh
	17	32K-WORD	050000h - 057FFFh
	16	32K-WORD	048000h - 04FFFFh
	15	32K-WORD	040000h - 047FFFh
	14	32K-WORD	038000h - 03FFFFh
	13	32K-WORD	030000h - 037FFFh
	12	32K-WORD	028000h - 02FFFFh
	11	32K-WORD	020000h - 027FFFh
	10	32K-WORD	018000h - 01FFFFh
	9	32K-WORD	010000h - 017FFFh
	8	32K-WORD	008000h - 00FFFFh
	7	4K-WORD	007000h - 007FFFh
	6	4K-WORD	006000h - 006FFFh
	5	4K-WORD	005000h - 005FFFh
	4	4K-WORD	004000h - 004FFFh
	3	4K-WORD	003000h - 003FFFh
	2	4K-WORD	002000h - 002FFFh
	1	4K-WORD	001000h - 001FFFh
	0	4K-WORD	000000h - 000FFFh

Figure 2.2. Memory Map for LH28F320BX series (Bottom Parameter)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (PARAMETER PLANE)	134	4K-WORD	3FF000H - 3FFFFFH
	133	4K-WORD	3FE000H - 3FEFFFH
	132	4K-WORD	3FD000H - 3FDFFFH
	131	4K-WORD	3FC000H - 3FCFFFH
	130	4K-WORD	3FB000H - 3FBFFFH
	129	4K-WORD	3FA000H - 3FAFFFH
	128	4K-WORD	3F9000H - 3F9FFFH
	127	4K-WORD	3F8000H - 3F8FFFH
	126	32K-WORD	3F0000H - 3F7FFFH
	125	32K-WORD	3E8000H - 3EFFFFH
	124	32K-WORD	3E0000H - 3E7FFFH
	123	32K-WORD	3D8000H - 3DFFFFH
	122	32K-WORD	3D0000H - 3D7FFFH
	121	32K-WORD	3C8000H - 3CFFFFH
	120	32K-WORD	3C0000H - 3C7FFFH
	119	32K-WORD	3B8000H - 3BFFFFH
	118	32K-WORD	3B0000H - 3B7FFFH
	117	32K-WORD	3A8000H - 3AFFFFH
	116	32K-WORD	3A0000H - 3A7FFFH
	115	32K-WORD	398000H - 39FFFFH
	114	32K-WORD	390000H - 397FFFH
	113	32K-WORD	388000H - 38FFFFH
	112	32K-WORD	380000H - 387FFFH
	111	32K-WORD	378000H - 37FFFFH
	110	32K-WORD	370000H - 377FFFH
	109	32K-WORD	368000H - 36FFFFH
	108	32K-WORD	360000H - 367FFFH
	107	32K-WORD	358000H - 35FFFFH
	106	32K-WORD	350000H - 357FFFH
	105	32K-WORD	348000H - 34FFFFH
	104	32K-WORD	340000H - 347FFFH
	103	32K-WORD	338000H - 33FFFFH
	102	32K-WORD	330000H - 337FFFH
	101	32K-WORD	328000H - 32FFFFH
	100	32K-WORD	320000H - 327FFFH
	99	32K-WORD	318000H - 31FFFFH
	98	32K-WORD	310000H - 317FFFH
	97	32K-WORD	308000H - 30FFFFH
	96	32K-WORD	300000H - 307FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	63	32K-WORD	1F8000H - 1FFFFFH
	62	32K-WORD	1F0000H - 1F7FFFH
	61	32K-WORD	1E8000H - 1EFFFFH
	60	32K-WORD	1E0000H - 1E7FFFH
	59	32K-WORD	1D8000H - 1DFFFFH
	58	32K-WORD	1D0000H - 1D7FFFH
	57	32K-WORD	1C8000H - 1CFFFFH
	56	32K-WORD	1C0000H - 1C7FFFH
	55	32K-WORD	1B8000H - 1BFFFFH
	54	32K-WORD	1B0000H - 1B7FFFH
	53	32K-WORD	1A8000H - 1AFFFFH
	52	32K-WORD	1A0000H - 1A7FFFH
	51	32K-WORD	198000H - 19FFFFH
	50	32K-WORD	190000H - 197FFFH
	49	32K-WORD	188000H - 18FFFFH
	48	32K-WORD	180000H - 187FFFH
	47	32K-WORD	178000H - 17FFFFH
	46	32K-WORD	170000H - 177FFFH
	45	32K-WORD	168000H - 16FFFFH
	44	32K-WORD	160000H - 167FFFH
	43	32K-WORD	158000H - 15FFFFH
	42	32K-WORD	150000H - 157FFFH
	41	32K-WORD	148000H - 14FFFFH
	40	32K-WORD	140000H - 147FFFH
	39	32K-WORD	138000H - 13FFFFH
	38	32K-WORD	130000H - 137FFFH
	37	32K-WORD	128000H - 12FFFFH
	36	32K-WORD	120000H - 127FFFH
	35	32K-WORD	118000H - 11FFFFH
	34	32K-WORD	110000H - 117FFFH
	33	32K-WORD	108000H - 10FFFFH
	32	32K-WORD	100000H - 107FFFH

PLANE2 (UNIFORM PLANE)	95	32K-WORD	2F8000H - 2FFFFFH
	94	32K-WORD	2F0000H - 2F7FFFH
	93	32K-WORD	2E8000H - 2EFFFFH
	92	32K-WORD	2E0000H - 2E7FFFH
	91	32K-WORD	2D8000H - 2DFFFFH
	90	32K-WORD	2D0000H - 2D7FFFH
	89	32K-WORD	2C8000H - 2CFFFFH
	88	32K-WORD	2C0000H - 2C7FFFH
	87	32K-WORD	2B8000H - 2BFFFFH
	86	32K-WORD	2B0000H - 2B7FFFH
	85	32K-WORD	2A8000H - 2AFFFFH
	84	32K-WORD	2A0000H - 2A7FFFH
	83	32K-WORD	298000H - 29FFFFH
	82	32K-WORD	290000H - 297FFFH
	81	32K-WORD	288000H - 28FFFFH
	80	32K-WORD	280000H - 287FFFH
	79	32K-WORD	278000H - 27FFFFH
	78	32K-WORD	270000H - 277FFFH
	77	32K-WORD	268000H - 26FFFFH
	76	32K-WORD	260000H - 267FFFH
	75	32K-WORD	258000H - 25FFFFH
	74	32K-WORD	250000H - 257FFFH
	73	32K-WORD	248000H - 24FFFFH
	72	32K-WORD	240000H - 247FFFH
	71	32K-WORD	238000H - 23FFFFH
	70	32K-WORD	230000H - 237FFFH
	69	32K-WORD	228000H - 22FFFFH
	68	32K-WORD	220000H - 227FFFH
	67	32K-WORD	218000H - 21FFFFH
	66	32K-WORD	210000H - 217FFFH
	65	32K-WORD	208000H - 20FFFFH
	64	32K-WORD	200000H - 207FFFH

PLANE0 (UNIFORM PLANE)	31	32K-WORD	0F8000H - 0FFFFFH
	30	32K-WORD	0F0000H - 0F7FFFH
	29	32K-WORD	0E8000H - 0EFFFFH
	28	32K-WORD	0E0000H - 0E7FFFH
	27	32K-WORD	0D8000H - 0DFFFFH
	26	32K-WORD	0D0000H - 0D7FFFH
	25	32K-WORD	0C8000H - 0CFFFFH
	24	32K-WORD	0C0000H - 0C7FFFH
	23	32K-WORD	0B8000H - 0BFFFFH
	22	32K-WORD	0B0000H - 0B7FFFH
	21	32K-WORD	0A8000H - 0AFFFFH
	20	32K-WORD	0A0000H - 0A7FFFH
	19	32K-WORD	098000H - 09FFFFH
	18	32K-WORD	090000H - 097FFFH
	17	32K-WORD	088000H - 08FFFFH
	16	32K-WORD	080000H - 087FFFH
	15	32K-WORD	078000H - 07FFFFH
	14	32K-WORD	070000H - 077FFFH
	13	32K-WORD	068000H - 06FFFFH
	12	32K-WORD	060000H - 067FFFH
	11	32K-WORD	058000H - 05FFFFH
	10	32K-WORD	050000H - 057FFFH
	9	32K-WORD	048000H - 04FFFFH
	8	32K-WORD	040000H - 047FFFH
	7	32K-WORD	038000H - 03FFFFH
	6	32K-WORD	030000H - 037FFFH
	5	32K-WORD	028000H - 02FFFFH
	4	32K-WORD	020000H - 027FFFH
	3	32K-WORD	018000H - 01FFFFH
	2	32K-WORD	010000H - 017FFFH
	1	32K-WORD	008000H - 00FFFFH
	0	32K-WORD	000000H - 007FFFH

Figure 3.1. Memory Map for LH28F640BX series (Top Parameter)

	BLOCK NUMBER		ADDRESS RANGE
PLANE3 (UNIFORM PLANE)	134	32K-WORD	3F8000H - 3FFFFFH
	133	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127	32K-WORD	3C0000H - 3C7FFFH
	126	32K-WORD	3B8000H - 3BFFFFH
	125	32K-WORD	3B0000H - 3B7FFFH
	124	32K-WORD	3A8000H - 3AFFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
	122	32K-WORD	398000H - 39FFFFH
	121	32K-WORD	390000H - 397FFFH
	120	32K-WORD	388000H - 38FFFFH
	119	32K-WORD	380000H - 387FFFH
	118	32K-WORD	378000H - 37FFFFH
	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
	115	32K-WORD	360000H - 367FFFH
	114	32K-WORD	358000H - 35FFFFH
	113	32K-WORD	350000H - 357FFFH
	112	32K-WORD	348000H - 34FFFFH
	111	32K-WORD	340000H - 347FFFH
	110	32K-WORD	338000H - 33FFFFH
	109	32K-WORD	330000H - 337FFFH
	108	32K-WORD	328000H - 32FFFFH
	107	32K-WORD	320000H - 327FFFH
	106	32K-WORD	318000H - 31FFFFH
	105	32K-WORD	310000H - 317FFFH
	104	32K-WORD	308000H - 30FFFFH
	103	32K-WORD	300000H - 307FFFH
PLANE2 (UNIFORM PLANE)	102	32K-WORD	2F8000H - 2FFFFFH
	101	32K-WORD	2F0000H - 2F7FFFH
	100	32K-WORD	2E8000H - 2EFFFFH
	99	32K-WORD	2E0000H - 2E7FFFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
	93	32K-WORD	2B0000H - 2B7FFFH
	92	32K-WORD	2A8000H - 2AFFFFH
	91	32K-WORD	2A0000H - 2A7FFFH
	90	32K-WORD	298000H - 29FFFFH
	89	32K-WORD	290000H - 297FFFH
	88	32K-WORD	288000H - 28FFFFH
	87	32K-WORD	280000H - 287FFFH
	86	32K-WORD	278000H - 27FFFFH
	85	32K-WORD	270000H - 277FFFH
	84	32K-WORD	268000H - 26FFFFH
	83	32K-WORD	260000H - 267FFFH
	82	32K-WORD	258000H - 25FFFFH
	81	32K-WORD	250000H - 257FFFH
	80	32K-WORD	248000H - 24FFFFH
	79	32K-WORD	240000H - 247FFFH
	78	32K-WORD	238000H - 23FFFFH
	77	32K-WORD	230000H - 237FFFH
	76	32K-WORD	228000H - 22FFFFH
	75	32K-WORD	220000H - 227FFFH
	74	32K-WORD	218000H - 21FFFFH
	73	32K-WORD	210000H - 217FFFH
	72	32K-WORD	208000H - 20FFFFH
	71	32K-WORD	200000H - 207FFFH

	BLOCK NUMBER		ADDRESS RANGE
PLANE1 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
	39	32K-WORD	100000H - 107FFFH
PLANE0 (PARAMETER PLANE)	38	32K-WORD	0F8000H - 0FFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
	7	4K-WORD	007000H - 007FFFH
	6	4K-WORD	006000H - 006FFFH
	5	4K-WORD	005000H - 005FFFH
	4	4K-WORD	004000H - 004FFFH
	3	4K-WORD	003000H - 003FFFH
	2	4K-WORD	002000H - 002FFFH
	1	4K-WORD	001000H - 001FFFH
	0	4K-WORD	000000H - 000FFFH

Figure 3.2. Memory Map for LH28F640BX series (Bottom Parameter)

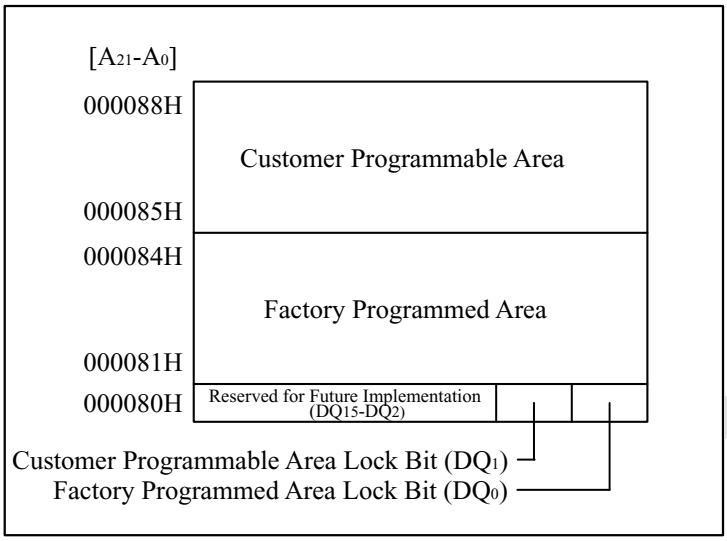

Figure 4. OTP Block Address Map for OTP Program(1, 2)
(The area outside 80H~88H cannot be used.)

NOTES:
1. A_{21} is not used for 32M-bit device.
2. Refer to Table 6 through Table 8 as to the OTP block address map for read operation.

2 Principles of Operation

Synchronous/Page Mode Dual Work Flash memory LH28F320BX/LH28F640BX series includes an on-chip WSM (Write State Machine) and can automatically execute block erase, full chip erase, (page buffer) program or OTP program operation after writing the proper command to the CUI (Command User Interface).

2.1 Operation Mode after Power-up or Reset Mode

After initial power-up or reset mode (refer to Bus Operation in Section 3), the device defaults to the following mode.

- Asynchronous read mode in which 8-word page mode is available
- Plane 0-2 are merged into one partition for top parameter devices and plane1-3 are merged into one partition for bottom parameter devices.
- All blocks default to locked state and are not locked-down.

Manipulation of external memory control pins (CE#, OE#) allow read array, standby and output disable modes.

2.2 Read, Program and Erase Operation

Independent of the V_{PP} voltage, the memory array, status register, identifier codes, OTP block and query codes can be accessed. And also, set/clear block lock configuration, set read configuration register and set partition configuration register are available even if the V_{PP} voltage is lower than V_{PPLK}. Applying the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP} enables successful block erase, full chip erase, (page buffer) program and OTP program operation. All functions associated with altering memory contents, which is block erase, full chip erase, (page buffer) program and OTP program, are accessed via the CUI and verified through the status register.

Commands are written using standard microprocessor write timings. Addresses and data are internally latched on the rising edge of CE# or WE# whichever goes high first during command write cycles. The CUI contents serve as input to the WSM, which controls block erase, full chip erase, (page buffer) program and OTP program. The internal algorithms are regulated by the WSM, including pulse repetition, internal verification and margining of data. Writing the appropriate command outputs array data, status register data, identifier codes, lock configuration codes, device configuration codes, data within the OTP block and query codes.

In any block, the user can store an interface software that initiates and polls progress of block erase or (page buffer) program. Because the LH28F320BX/LH28F640BX series has dual work function, data can be read from the partition not being erased or programmed without using the block erase suspend or (page buffer) program suspend. When the target partition is being erased or programmed, block erase suspend or (page buffer) program suspend allows system software to read/program data from/to blocks other than that which is suspended.

2.3 Status Register for Each Partition

The LH28F320BX/LH28F640BX series has status registers for each partition. The 8-bit status register is available to monitor the partition state, or the erase or program status. Status Register indicates the status of the partition, not WSM. Even if the status register bit SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration. The status register reports if an erase or program operation to each partition has been successfully completed, and if not, indicates a reason for the error. This register cannot be set, only can be cleared by writing the Clear Status Register command or by resetting the device.

2.4 Data Protection

Block lock bit and block lock-down bit can be set for each block, to protect the data within its block.

If the RST# is driven low (V_{IL}), or if the voltage on the V_{CC} pin is below the write lock out voltage (V_{LKO}), or if the voltage on the V_{PP} pin is below the write lock out voltage (V_{PPLK}), then all write functions including OTP program are disabled.

The system should be designed to switch the voltage on V_{PP} below the write lock out voltage (V_{PPLK}) for read cycles. This scheme provides the data protection at the hardware level. The two-cycle command sequence architecture for block erase, full chip erase, (page buffer) program, OTP program, and block lock configuration provides the data protection at the software level against data alternation.

3 Bus Operation

The system CPU reads and writes the flash memory. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles. Table 4 lists the bus operation.

3.1 Read Array

LH28F320BX/LH28F640BX series has seven control pins (CLK, CE#, OE#, ADV#, WE#, RST# and WP#). When RST# is V_{IH}, read operations access the memory array, status register, identifier codes, OTP block and query codes independent of the voltage on V_{PP}.

The device is automatically initialized upon power-up or device reset mode and set to asynchronous read mode in which 8-word page mode is available. As necessary, write the appropriate read command (Read Array, Read Identifier codes/OTP, Read Query or Read Status Register command) with the partition address to the CUI (Command User Interface). The CUI decodes the partition address and set the target partition to the appropriate read mode.

Synchronous burst mode can be set by writing the Set Read Configuration Register command. It is impossible to set one partition to asynchronous read mode and other partition to synchronous burst mode at a time.

Asynchronous page mode and synchronous burst mode are available only for main array, that is, parameter blocks and main blocks. Read operations for status register, identifier codes, OTP block and query codes support single asynchronous read cycle or single synchronous read cycle.

To read data from the LH28F320BX/LH28F640BX series, RST# and WE# must be at V_{IH}, and CE# and OE# at V_{IL}. ADV# must be driven V_{IL} to fetch address. CE# is the device selection control, and CE#-low enables the selected memory device. OE# is the data output (DQ_0-DQ_{15}) control and OE#-low drives the selected memory data onto the I/O bus.

3.2 Output Disable

With OE# at V_{IH}, the device outputs are disabled. Output pins DQ_0 - DQ_{15} are placed in a high-impedance (High Z) state.

3.3 Standby

CE# at a logic-high level (V_{IH}) places the LH28F320BX/LH28F640BX series in standby mode.

In standby mode, the LH28F320BX/LH28F640BX series substantially reduces its power consumption because almost of all internal circuits are inactive. DQ_0-DQ_{15} outputs a High Z state independent of OE#. Even if CE# is set to V_{IH} during block erase, full chip erase, (page buffer) program or OTP program, the device continues the operation and consumes active power until the completion of the operation.

3.4 Reset

Driving RST# to logic-low level (V_{IL}) places the LH28F320BX/LH28F640BX series in reset mode.

If RST# is held V_{IL} for a minimum t_{PLPH} in read modes, the device is deselected and internal circuitry is turned off. Outputs are placed in a High Z state. Status register is set to 80H. Time t_{PHQV} is required after return from reset mode until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The device returns to the initial mode described in Section 2.1.

During block erase, full chip erase, (page buffer) program or OTP program mode, RST#-low will abort the operation. Memory contents being altered are no longer valid; the data may be partially erased or programmed. Status register bit SR.7 remains "0" until the reset operation has been completed. After RST# goes to V_{IH}, time t_{PHWL} and t_{PHEL} is required before another command can be written.

As with any automated device, it is important to assert RST# during system reset. When the system comes out of reset, it expects to read the data from the flash memory. LH28F320BX/LH28F640BX series allows proper CPU initialization following a system reset through the use of the RST# input. In this application, RST# is controlled by the same RESET# signal that resets the system CPU. After return from reset mode, the LH28F320BX/LH28F640BX series is automatically set to asynchronous read mode in which 8-word page mode is available. Delay time t_{PHQV} is required until memory access outputs are valid.

••••• Synchronous burst mode will be available for future device.

Table 4. Bus Operation(1, 2)

Mode	Notes	RST#	CE#	OE#	WE#	Address	V_{PP}	DQ_{0-15}
Read Array	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	X	D_{OUT}
Output Disable		V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	High Z
Standby		V_{IH}	V_{IH}	X	X	X	X	High Z
Reset	3	V_{IL}	X	X	X	X	X	High Z
Read Identifier Codes/OTP	6	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Table 6 through Table 8	X	See Table 6 through Table 8
Read Query	6,7	V_{IH}	V_{IL}	V_{IL}	V_{IH}	See Section 6	X	See Section 6
Write	4,5,6	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	D_{IN}

NOTES:
1. Refer to DC Characteristics. When $V_{PP} \leq V_{PPLK}$, memory contents can be read, but cannot be altered.
2. X can be V_{IL} or V_{IH} for control pins and addresses, and V_{PPLK} or $V_{PPH1/2}$ for V_{PP}. See DC Characteristics for V_{PPLK} and $V_{PPH1/2}$ voltages.
3. RST# at GND±0.2V ensures the lowest power consumption.
4. Command writes involving block erase, full chip erase, (page buffer) program or OTP program are reliably executed when $V_{PP}=V_{PPH1/2}$ and V_{CC} is the specified voltage.
5. Refer to Table 5 for valid D_{IN} during a write operation.
6. Never hold OE# low and WE# low at the same timing.
7. Refer to Appendix of LH28F320BX/LH28F640BX series for more information about query code.

3.5 Read Identifier Codes/OTP

The manufacturer code, device code, block lock configuration codes, read configuration register code, partition configuration register code and the data within the OTP block can be read in the read identifier codes/ OTP mode (see Table 6 through Table 8). Using the manufacturer and device codes, the system CPU can automatically match the device with its proper algorithms.

3.6 Read Query

CFI (Common Flash Interface) code, which is called query code, can be read after writing the Read Query command. The address to read query code should be in the partition address which is written with the Read Query command. The CFI data structure contains information such as block size, density, command set and electrical specifications (see Section 6). In this mode, read cycles retrieve CFI information. To return to read array mode, write the Read Array command (FFH) with the partition address.

3.7 Write the Command to the CUI

Except for the Full Chip Erase command, writing commands to the CUI always requires the word address, block address or partition address. Before writing the Block Erase command, Full Chip Erase command, (Page Buffer) Program command or OTP Program command, WSM (Write State Machine) should be ready and not be used in any partition.

Applying the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP} enables successful block erase, full chip erase, (page buffer) program or OTP program with writing the proper command and address to the CUI. Erase or program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

The Block Erase command requires appropriate command and an address within the block to be erased. The Full Chip Erase command requires appropriate command. The (Page Buffer) Program command requires appropriate command and an address of the location to be programmed. The Set/Clear Block Lock Bit or Set Block Lock-down Bit command requires appropriate command and an address within the target block. The OTP Program command requires appropriate command and an address of the location to be programmed within the OTP block. The Set Read Configuration Register command or the Set Partition Configuration Register command requires appropriate command and configuration register code presented on the addresses A_0-A_{15}.

The CUI itself does not occupy an addressable memory location. When both CE# and WE# go V_{IL} (valid), the command is written to CUI and the address and data are latched on the rising edge of CE# or WE#, whichever goes high first. The command can be written to the CUI at the standard microprocessor writing timing.

4 Command Definitions

Operations of the device are selected by the specific commands written to the CUI (Command User Interface). Since commands are partition-specific, it is important to write commands within the target partition's address range (see Table 5).

Each command except for the Full Chip Erase command and OTP Program command affects only the mode of the partition to which the command is written.

4.1 Read Array Command

Upon initial device power-up or after reset mode, all the partitions in the device default to asynchronous read mode in which 8-word page mode is available. The Read Array command to a partition places the partition to read array mode. The partition remains enabled for read array mode until another valid command is written to the partition. When RST# is at V_{IH}, the Read Array command is valid independent of the voltage on V_{PP}. Once the internal WSM (Write State Machine) has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Array command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Array command can be accepted in other partitions except for full chip erase or OTP program operation.

Since LH28F320BX/LH28F640BX series provide dual work capability, partitions not executing block erase or (page buffer) program operation are allowed to set to the read array mode and the memory array data within the partitions can be read without suspending block erase or (page buffer) program operation.

4.2 Read Identifier Codes/OTP Command

The read identifier codes/OTP mode is initiated by writing the Read Identifier Codes/OTP command (90H) to the target partition. Read operations to that partition output the identifier codes or the data within the OTP block. To terminate the operation, write another valid command to the partition. In this mode, the manufacturer code, device code, block lock configuration codes, read configuration register code, partition configuration register code and the data within the OTP block as well as the OTP block lock state can be read on the addresses shown in Table 6 through Table 8. Once the internal WSM has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Identifier Codes/ OTP command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Identifier Codes/OTP command can be accepted in other partitions except for full chip erase or OTP program operation. Like the Read Array command, the Read Identifier Codes/OTP command functions independently of the V_{PP} voltage and RST# must be at V_{IH}.

To read the data in the OTP block, it is important to write addresses within the OTP area's address range (refer to Table 6 through Table 8).

Asynchronous page mode and synchronous burst mode are not available for reading identifier codes/OTP. Read operations for identifier codes or OTP block support single asynchronous read cycle or single synchronous read cycle.

Table 5. Command Definitions(11)

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper(1)	Addr(2)	Data(3)	Oper(1)	Addr(2)	Data(3)
Read Array	1	2	Write	PA	FFH			
Read Identifier Codes/OTP	≥ 2	2,3,4	Write	PA	90H	Read	IA or OA	ID or OD
Read Query	≥ 2	2,3,4	Write	PA	98H	Read	QA	QD
Read Status Register	2	2,3	Write	PA	70H	Read	PA	SRD
Clear Status Register	1	2	Write	PA	50H			
Block Erase	2	2,3,5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	2,5,9	Write	X	30H	Write	X	D0H
Program	2	2,3,5,6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	2,3,5,7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	2,8,9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	2,8,9	Write	PA	D0H			
Set Block Lock Bit	2	2	Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	2,10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2	2	Write	BA	60H	Write	BA	2FH
OTP Program	2	2,3,9	Write	OA	C0H	Write	OA	OD
Set Read Configuration Register	2	2,3	Write	RCRC	60H	Write	RCRC	03H
Set Partition Configuration Register	2	2,3	Write	PCRC	60H	Write	PCRC	04H

NOTES:
1. Bus operations are defined in Table 4.
2. First bus cycle command address should be the same as the second cycle address.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See Table 6 through Table 8).
   QA=Query codes address. Refer to Appendix of LH28F320BX/LH28F640BX series for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   OA=Address of OTP block to be read or programmed (See Figure 4).
   RCRC=Read configuration register code presented on the addresses A_0-A_{15}.
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes. (See Table 6 through Table 8).
   QD=Data read from query database. Refer to Appendix of LH28F320BX/LH28F640BX series for details.
   SRD=Data read from status register. See Table 9 for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   OD=Data to be programmed at location OA. Data is latched on the rising edge of WE# or CE# (whichever goes high first).
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes/OTP command, read operations access manufacturer code, device code, block lock configuration code, read configuration register code, partition configuration register code and the data within OTP block (See Table 6 through Table 8).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when RST# is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.

7. Following the third bus cycle, inputs the program sequential address and write data of "N" times. Finally, input the any valid address within the target partition to be programmed and the confirm command (D0H). Refer to Appendix of LH28F320BX/LH28F640BX series for details.
8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase and OTP program operations can not be suspended. The OTP Program command can not be accepted while the block erase operation is being suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when WP# is V_{IL}. When WP# is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

Table 6. Identifier Codes and OTP Address for Read Operation

	Code	Address $[A_{15}\text{-}A_0]$(1)	Data $[DQ_{15}\text{-}DQ_0]$	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	
Device Code (32M-bit device)	32M Top Parameter Device Code	0001H	00B4H	2
	32M Bottom Parameter Device Code	0001H	00B5H	3
Device Code (64M-bit device)	64M Top Parameter Device Code	0001H	00B0H	2
	64M Bottom Parameter Device Code	0001H	00B1H	3
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	$DQ_0 = 0$	4
	Block is Locked		$DQ_0 = 1$	4
	Block is not Locked-Down		$DQ_1 = 0$	4
	Block is Locked-Down		$DQ_1 = 1$	4
Device Configuration Code	Read Configuration Register	0005H	RCRC	5
	Partition Configuration Register	0006H	PCRC	6
OTP	OTP Lock	0080H	OTP-LK	7
	OTP	0081-0088H	OTP	8

NOTES:
1. The address $A_{20}\text{-}A_{16}$ to read the manufacturer, device, lock configuration, device configuration code and OTP data are shown in below table.
2. Top parameter device has its parameter blocks in the plane3 (The highest address).
3. Bottom parameter device has its parameter blocks in the plane0 (The lowest address)
4. $DQ_{15}\text{-}DQ_2$ is reserved for future implementation.
5. RCRC=Read Configuration Register Code.
6. PCRC=Partition Configuration Register Code.
7. OTP-LK=OTP Block Lock configuration.
8. OTP=OTP Block data.

Table 7. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1) for 32M-bit device

Partition Configuration Register			Address (32M-bit device)
PCR.10	PCR.9	PCR.8	$[A_{20}\text{-}A_{16}]$
0	0	0	00H
0	0	1	00H or 08H
0	1	0	00H or 10H
1	0	0	00H or 18H
0	1	1	00H or 08H or 10H
1	1	0	00H or 10H or 18H
1	0	1	00H or 08H or 18H
1	1	1	00H or 08H or 10H or 18H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).

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••••• Synchronous burst mode will be available for future device.

Table 8. Identifier Codes and OTP Address for Read Operation on Partition Configuration(1) for 64M-bit device

Partition Configuration Register			Address (64M-bit device)
PCR.10	PCR.9	PCR.8	[A_{21}-A_{16}]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

NOTES:
1. The address to read the identifier codes or OTP data is dependent on the partition which is selected when writing the Read Identifier Codes/OTP command (90H).

4.3 Read Query Command

The read query mode is initiated by writing the Read Query command (98H) to the target partition. Read operations to that partition output the query code (Common Flash Interface code) shown in Section 6. To terminate the operation, write another valid command to the partition. Once the internal WSM has started block erase, full chip erase, (page buffer) program or OTP program in one partition, the partition will not recognize the Read Query command until the WSM completes its operation or unless the WSM is suspended via the Block Erase Suspend or (Page Buffer) Program Suspend command. However, the Read Query command can be accepted in other partitions except for full chip erase or OTP program operation. Like the Read Array command, the Read Query command functions independently of the V_{PP} voltage and RST# must be at V_{IH}. Refer to Section 6 for more information about query code.

Asynchronous page mode and synchronous burst mode are not available for reading query code. Read operations for query code support single asynchronous read cycle or single synchronous read cycle.

4.4 Read Status Register Command

The status register may be read to determine when block erase, full chip erase, (page buffer) program or OTP program has been completed and whether the operation has been successfully completed or not (see Table 9). The status register can be read at any time by writing the Read Status Register command (70H) to the target partition. Subsequent read operations to that partition output the status register data until another valid command is written. The status register contents are latched on the falling edge of OE# or CE# whichever occurs later. OE# or CE# must toggle to V_{IH} before further reads to update the status register latch. The Read Status Register command functions independently of the V_{PP} voltage and RST# must be at V_{IH}.

Asynchronous page mode and synchronous burst mode are not available for reading status register. Read operations for status register support single asynchronous read cycle or single synchronous read cycle.

During the dual work operation, the status register data is read from the partition which is executing block erase or (page buffer) program operation. The memory array data can be read from other partitions which are not executing block erase or (page buffer) program operation. The partition to be accessed is automatically identified according to the input address.

4.5 Clear Status Register Command

Status register bits SR.5, SR.4, SR.3 and SR.1 that have been set to "1"s by the WSM can only be cleared by writing the Clear Status Register command (50H). This command functions independently of the V_{PP} voltage. RST# must be at V_{IH}. To clear the status register, write the Clear Status Register command and an address within the target partition to the CUI.

Status register bits SR.5, SR.4, SR.3 and SR.1 indicate various error conditions occurring after writing commands (see Table 9). When erasing multiple blocks or programming several words in sequence, clear these bits before starting each operation. The status register bits indicate an error for during the sequence.

After executing the Clear Status Register command, the partition returns to read array mode. This command clears only the status register of the addressed partition. During block erase suspend or (page buffer) program suspend, the Clear Status Register command is invalid and the status register cannot be cleared.

••••• Synchronous burst mode will be available for future device.

Table 9. Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPOPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)
- 1 = Ready
- 0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)
- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)
- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM AND OTP PROGRAM STATUS (PBPOPS)
- 1 = Error in (Page Buffer) Program or OTP Program
- 0 = Successful (Page Buffer) Program or OTP Program

SR.3 = V_{PP} STATUS (VPPS)
- 1 = V_{PP} LOW Detect, Operation Abort
- 0 = V_{PP} OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)
- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)
- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 to determine block erase, full chip erase, (page buffer) program or OTP program completion. SR.6 - SR.0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, page buffer program, set/clear block lock bit, set block lock-down bit or set read/partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH1}$, V_{PPH2} or V_{PPLK}.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes/OTP command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Table 10. Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)
- 1 = Page Buffer Program available
- 0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:
After issue a Page Buffer Program command (E8H), XSR.7=1 indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

4.6 Block Erase Command

The two-cycle Block Erase command initiates one block erase at the addressed block within the target partition. Read operations to that partition output the status register data of its partition. At the first cycle, command (20H) and an address within the block to be erased is written to the CUI, and command (D0H) and the same address as the first cycle is written at the second cycle. Once the Block Erase command is successfully written, the WSM automatically starts erase and verification processes. The data in the selected block are erased (becomes FFFFH). The system CPU can detect the block erase completion by analyzing the output data of the status register bit SR.7. The partition including the block to be erased remains in read status register mode after the completion of the block erase operation until another command is written to the CUI. Figure 5.1 and Figure 5.2 show a flowchart of the block erase operation.

Check the status register bit SR.5 at the end of block erase. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The partition remains in read status register mode until a new command is written to that partition.

This two-cycle command sequence ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in status register bits SR.5 and SR.4 of the partition being set to "1" and the operation will be aborted.

For reliable block erase operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, block erase operations are not guaranteed. For example, attempting a block erase at $V_{PP} \leq V_{PPLK}$ causes SR.5 and SR.3 being set to "1". Also, successful block erase requires that the selected block is unlocked. When block erase is attempted to the locked block, bits SR.5 and SR.1 will be set to "1".

Block erase operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

4.7 Full Chip Erase Command

The two-cycle Full Chip Erase command erases all of the unlocked blocks. Before writing this command, all of the partitions should be ready (WSM should not be occupied by any partition). At the first cycle, command (30H) is written to the CUI, and command (D0H) is written at the second cycle. After writing the command, the device outputs the status register data when any address within the device is selected. The WSM automatically starts the erase operation for all unlocked blocks, skipping the locked blocks. The full chip erase operation cannot be suspended through the erase suspend command (described later). The system CPU can detect the full chip erase completion by analyzing the output data of the status register bit SR.7. All the partitions remain in the read status register mode after the completion of the full chip erase operation until another command is written to the CUI. Figure 6.1 and Figure 6.2 show a flowchart of the full chip erase operation.

The WSM aborts the operation upon encountering an error during the full chip erase operation and leaves the remaining blocks not erased. After the full chip erase operation, check the status register bit SR.5. When a full chip erase error is detected, SR5 of all partitions will be set to "1". The status registers for all partitions should be cleared before system software attempts corrective actions. After that, retry the Full Chip Erase command or erase block by block using the Block Erase command.

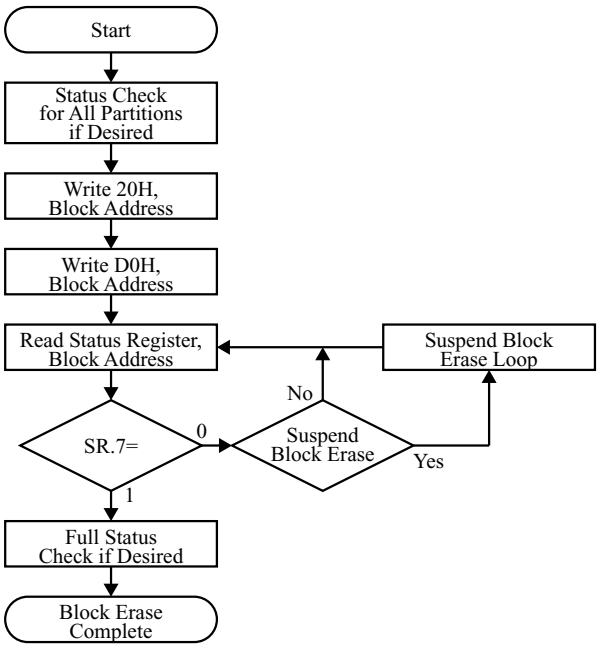
This two-cycle command sequence ensures that block contents are not accidentally erased. An invalid Full Chip Erase command sequence will result in status register bits SR.5 and SR.4 of all partitions being set to "1" and the operation will be aborted.

For reliable full chip erase operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, full chip erase operations are not guaranteed. For example, attempting a full chip erase at $V_{PP} \leq V_{PPLK}$ causes SR.5 and SR.3 being set to "1".

As previously mentioned, the Full Chip Erase command erases all blocks except for the locked blocks. Unlike the block erase, the status register bits SR.5 and SR.1 are not set to "1" even if the locked block is included. However, when all blocks are locked, the bits SR.5 and SR.1 are set to "1" and the operation will not be executed.

If an error is detected during the full chip erase operation, error bits for all status registers are set to "1". This requires that the Clear Status Register command be written to all partitions to clear the error bits.

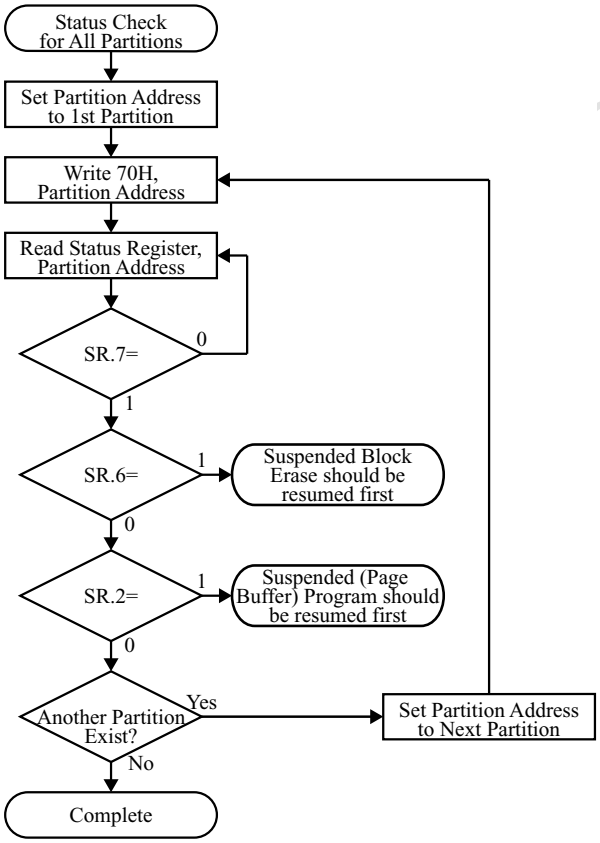
Dual work operation is not available during the full chip erase mode. The memory array data cannot be read in this mode. To return to the read array mode, write the Read Array command (FFH) to the CUI after the completion of the full chip erase operation.



Bus Operation	Command	Comments
Write	Block Erase	<First cycle> Data=20H Addr=Within Block to be Erased
		<Second cycle> Data=D0H Addr=Within Block to be Erased
Read		Status Register Data Addr=Within Block to be Erased
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

When subsequently erasing a block, repeat the above sequence.
Full status check can be done after each block erase or after a sequence of block erasures.
Write FFH after a sequence of block erasures to place device in read array mode.

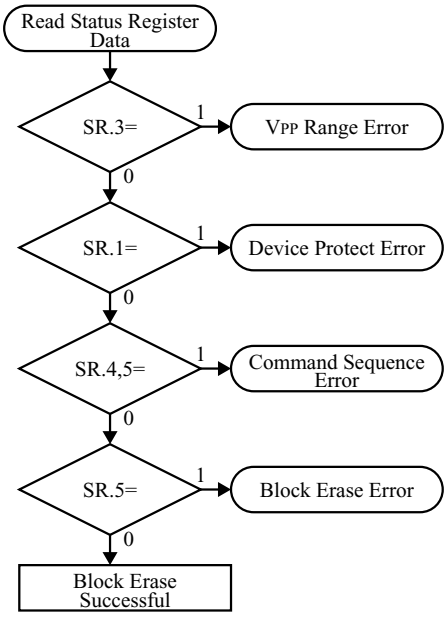
STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE BLOCK ERASE OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed

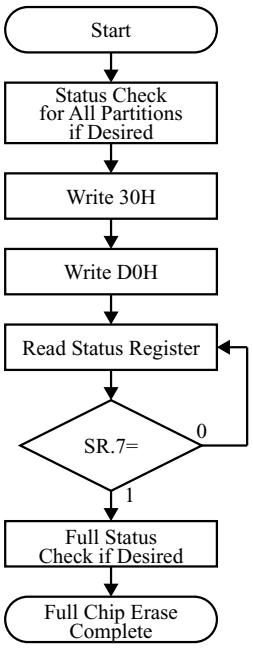
Figure 5.1. Automated Block Erase Flowchart

FULL STATUS CHECK PROCEDURE



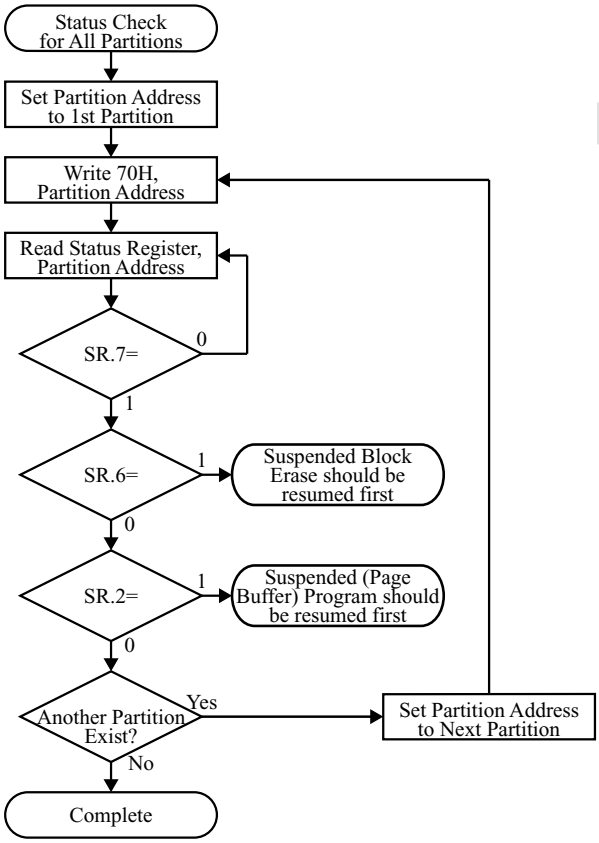
Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Block Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 5.2. Automated Block Erase Flowchart (Continued)



Bus Operation	Command	Comments
Write	Full Chip Erase	<First cycle> Data=30H Addr=X
		<Second cycle> Data=D0H Addr=X
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Check the status after full chip erase. Write FFH after the full chip erase to place device in read array mode.		

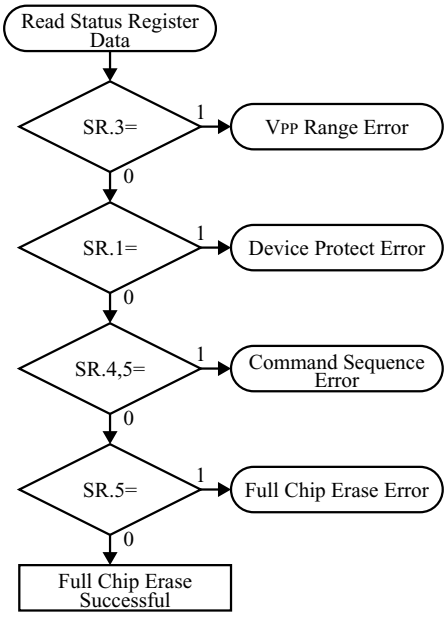
STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE FULL CHIP ERASE OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed

Figure 6.1. Automated Full Chip Erase Flowchart

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect All Blocks are locked.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.5 1=Full Chip Erase Error
SR.5, SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple blocks are erased before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 6.2. Automated Full Chip Erase Flowchart (Continued)

4.8 Program Command

A two-cycle command sequence written to the target partition initiates a word program operation. Read operations to the target partition to be programmed output the status register data until another valid command is written. At the first cycle, write command (standard 40H or alternate 10H) and an address of memory location to be programmed, followed by the second write that specifies the address and data. The WSM then takes over, controlling the internal word program algorithm. The system CPU can detect the word program completion by analyzing the output data of the status register bit SR.7. Figure 7.1 and Figure 7.2 show a program flowchart.

The internal WSM verify only detects errors for "1"s that are not successfully programmed to "0"s. Check the status register bit SR.4 at the end of word program. If a word program error is detected, the status register should be cleared before system software attempts corrective actions. The partition remains in read status register mode until it receives another command.

For reliable word program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, word program operations are not guaranteed. For example, attempting a word program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". Also, successful word program requires for the selected block is unlocked. When word program is attempted to the locked block, bits SR.4 and SR.1 will be set to "1".

Word program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.

4.9 Page Buffer Program Command

The LH28F320BX/LH28F640BX series has two planes of 16-word page buffer, which can perform fast sequential programming up to 32 words. The data are once loaded to the page buffer and programmed to the flash array when the confirm command (D0H) is written. See the flowchart in Figure 8.1 and Figure 8.2.

The page buffer program is executed by at least four-cycle or up to 19-cycle command sequence. First, write the Page Buffer Program setup command (E8H) and start address to the partition's CUI. At this point, read operations to the target partition to be programmed output the extended status register data (see Table 10). Check the extended status register data. If the extended status register bit XSR 7 is "0", no page buffer is available and Page Buffer Program setup command which has just been written is ignored. To retry, continue monitoring XSR.7 by writing Page Buffer Program setup (E8H) with program address until XSR.7 transitions to "1". When XSR.7 transitions to "1", the setup command written is valid. Then, at the second cycle, write the word count [N]-1 and start address if the number of words to be programmed is [N] in total. That is, when the number of [N] is 1 word, write (00H); if [N] is 16 words, write (0FH). The word count [N]-1 must be less than or equal to 0FH. Attempting to write more than 0FH for the word count causes the sequence error and the status register bits SR.5 and SR.4 are set to "1". After writing a word count [N]-1, read operations to the target partition to be programmed output the status register data. At the third cycle following the write of [N]-1, write the first data to be programmed and start address to the partition's CUI. Lower 4 bits (A_0-A_3) of the start address also correspond to the page buffer address and the data are stored in the page buffer. At the fourth and subsequent cycles, write additional data and address, depending on the count. All subsequent address must lie within the start address plus the count. After writing the Nth word data, write the confirm command (D0H) and an address within the target partition at the last cycle. This initiates the WSM to being transferring the data from the page buffer to the flash array. If a command other than the confirm command (D0H) is written, sequence error occurs and status register bits SR.5 and SR.4 of the partition are set to "1". When the data are transferred from the page buffer to the flash array, the status register bit SR.7 is set to "0". Then, the target partition is in the page buffer program busy mode.

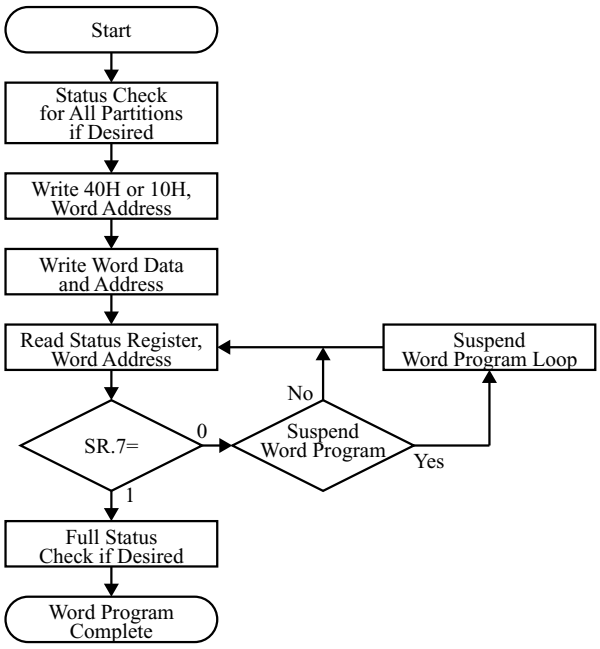
For additional page buffer program, write another Page Buffer Program setup command (E8H) and check XSR.7. The Page Buffer Program command can be queued while WSM is busy as long as XSR.7 indicates "1", because LH28F320BX/LH28F640BX series has two buffers. If an error occurs while programming, the device will stop programming and flush next page buffer program command which has been previously queued. Status register bit SR.4 is set to "1". SR.4 should be cleared before writing next command.

If the Page Buffer Program command is attempted past an erase block boundary, the device will program the data to the flash array up to an erase block boundary and then stop programming. The status register bits SR.5 and SR.4 will be set to "1" (command sequence error). SR.5 and SR.4 should be cleared before writing next command.

For reliable page buffer program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, page buffer program operations are not guaranteed. For example, attempting a page buffer program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". Also, successful page buffer program requires for the selected block is unlocked. When page buffer program is attempted to the locked block, bits SR.4 and SR.1 will be set to "1".

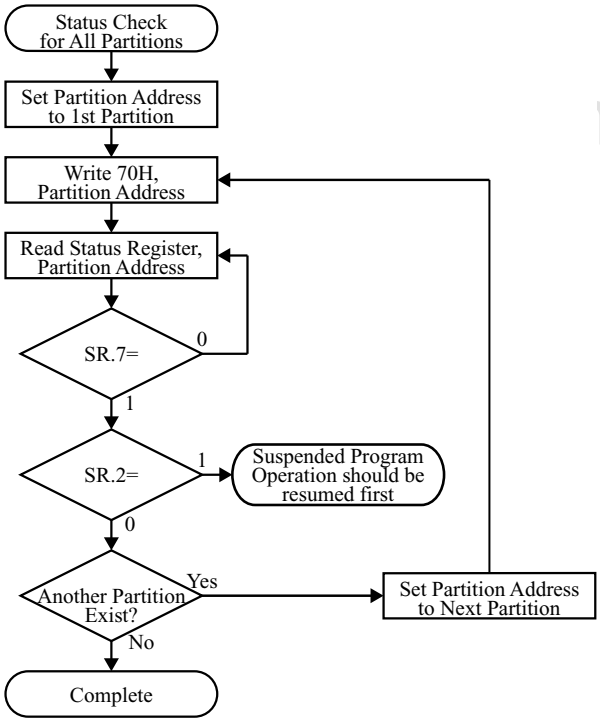
During page buffer program, dual work operation is available. The array data can be read from partitions not being programmed.

Page buffer program operation may occur in only one partition at a time. Other partitions must be in one of the read modes.



Bus Operation	Command	Comments
Write	Word Program	<First cycle> Data=40H or 10H Addr=Location to be Programmed
		<Second cycle> Data= Data to be Programmed Addr=Location to be Programmed
Read		Status Register Data Addr=Location to be Programmed
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat the above sequence for the subsequent word programs. SR full status check can be done after each word program, or after a sequence of word programs. Write FFH after a sequence of word programs to place device in read array mode.		

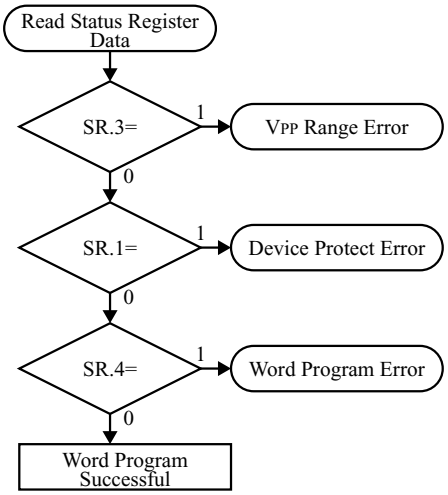
STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE WORD PROGRAM OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Program Suspended 0=Program Completed

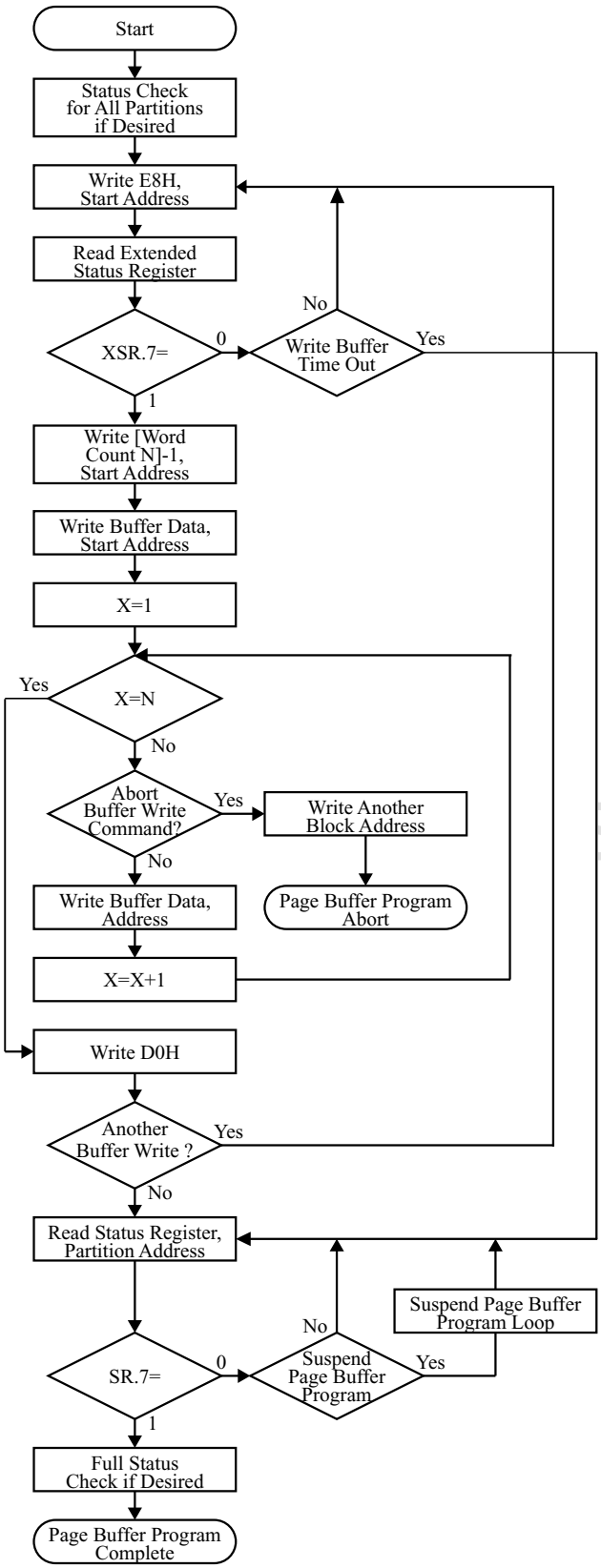
Figure 7.1. Automated Program Flowchart

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4 1=Word Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register Command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

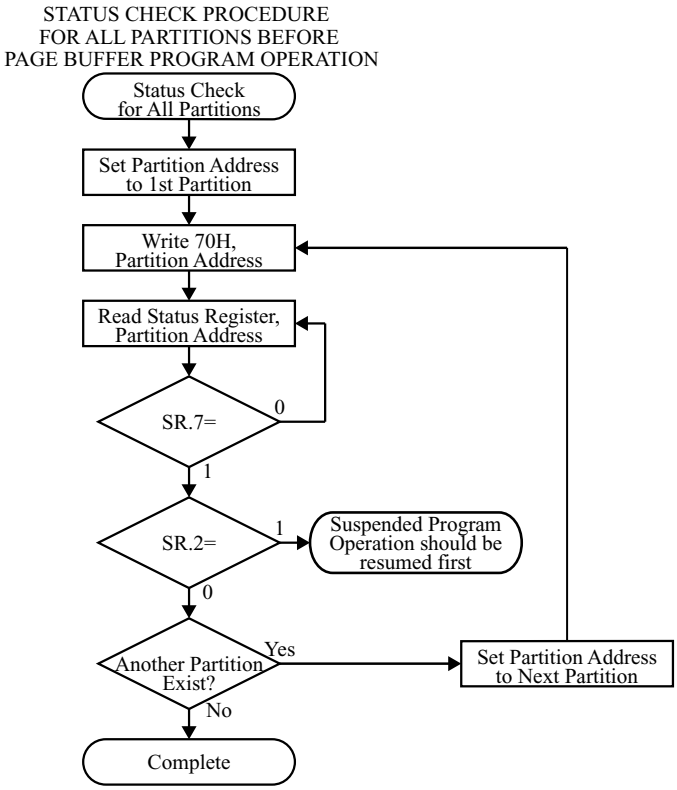
Figure 7.2. Automated Program Flowchart (Continued)



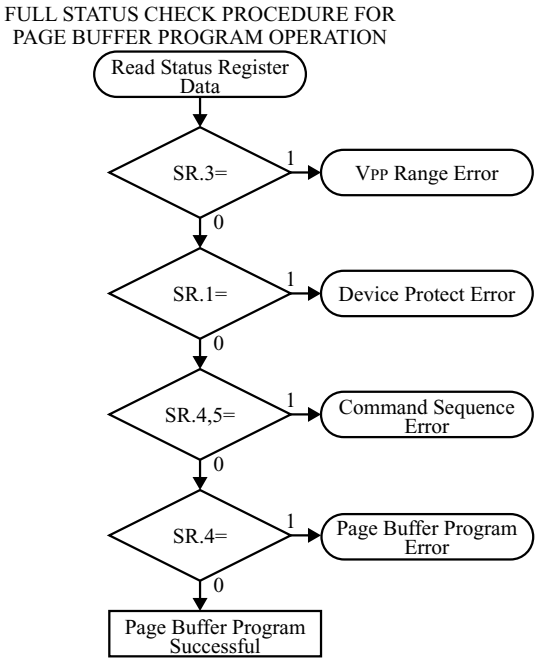
Bus Operation	Command	Comments
Write	Page Buffer Program	<First cycle> Data=E8H Addr=Start Address
Read		Extended Status Register Data
Standby		Check XSR.7 1=Page Buffer Program Ready 0=Page Buffer Program Busy
Write (Note 1)	Page Buffer Program	<Second cycle> Data=[Word Count N]-1 Addr=Start Address
Write (Note 2, 3)		<Third cycle> Data=Buffer Data Addr=Start Address
Write (Note 4, 5)		<(N+2)th cycle> Data=Buffer Data Addr=Sequential Address following start address
Write		<(N+3)th cycle> Data=D0H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

1. Word count values on DQ_{0-7} are loaded into count register.
2. Write Buffer contents will be programmed at the start address.
3. Align the start address on a Write Buffer boundary for maximum programming performance.
4. The device aborts the Page Buffer Program command if the current address is outside of the original block address.
5. The Status Register indicates an “improper command sequence” if the Page Buffer Program command is aborted. Follow this with a Clear Status Register command.
   SR full status check can be done after each page buffer program, or after a sequence of page buffer programs.
   Write FFH after the last page buffer program operation to place device in read array mode.

Figure 8.1. Automated Page Buffer Program Flowchart



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=Program Suspended 0=Program Completed



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect Block lock bit is set.
Standby		Check SR.4,5 Both 1=Command Sequence Error
Standby		Check SR.4 1=Page Buffer Program Error
SR.5,SR.4,SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the Status Register before attempting retry or other error recovery.		

Figure 8.2. Automated Page Buffer Program Flowchart (Continued)

4.10 Block Erase Suspend Command and Block Erase Resume Command

The Block Erase Suspend command (B0H) allows block erase interruption to read or program data in the blocks other than that which is suspended. This command is valid for the block erase operation and the full chip erase operation can not be suspended.

Once the block erase process starts in a partition, writing the Block Erase Suspend command to the partition requests that the WSM suspends the block erase sequence at a predetermined point in the algorithm. Read operations to the target partition after writing the Block Erase Suspend command access the status register. Status register bits SR.7 and SR.6 indicate if the block erase operation has been suspended (both will be set to "1"). Specification t_{WHRH2} or t_{EHRH2} defines the block erase suspend latency.

When the Block Erase Suspend command is written after the completion of the block erase operation, the partition returns to read array mode. Therefore, the Read Status Register command (70H) must be written to the target partition after writing the Block Erase Suspend command. If the status register bits SR.7 and SR.6 are set to "1", block erase has been suspended.

At this point, a Read Array command can be written to read data from blocks other than that which is suspended. A (Page Buffer) Program command sequence can also be written during block erase suspend to program data in other blocks. Using the (Page Buffer) Program Suspend command (see Section 4.11), a program operation can also be suspended during a block erase suspend.

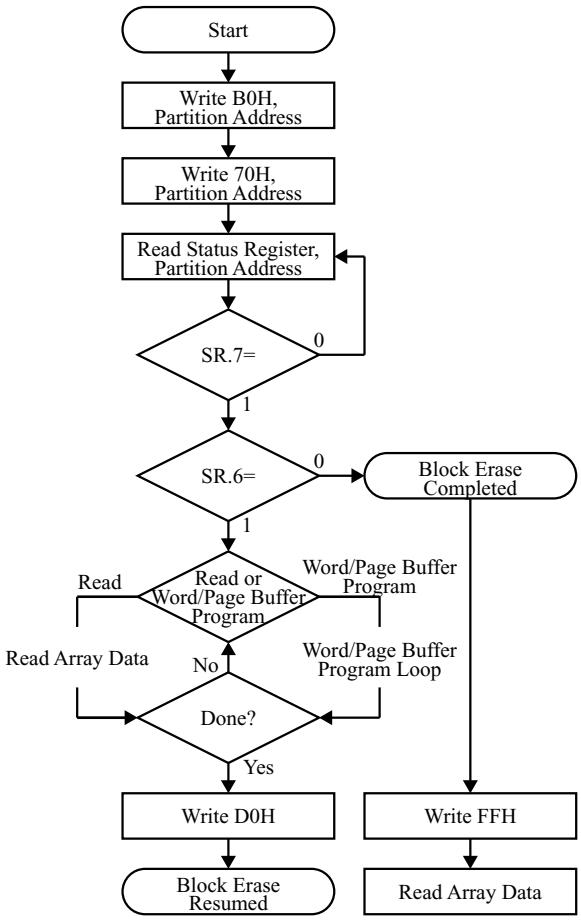
During a word program operation with block erase suspended, status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate the block erase suspend status.

If the Page Buffer Program setup command (E8H) is written to the target partition during block erase suspend in which SR.7 and SR.6 are set to "1", read operations to the target partition to be programmed output the extended status register data. In read extended status register mode, bit XSR.7 is only valid, which indicates that the written command (E8H) is available, and other bits (from XSR.6 to XSR.0) are invalid (see Table 10). When writing the word count [N]-1 and start address at next command cycle, the target partition returns to read status register mode and the status register bits SR.7 and SR.6 are set to "1". After the Page Buffer Program confirm command (D0H) is written, the status register bit SR.7 will return to "0". However, SR.6 will remain "1" to indicate the block erase suspend status.

The only other valid commands while block erase is suspended are Read Identifier Codes/OTP, Read Query, Read Status Register, Set Block Lock Bit, Clear Block Lock Bit, Set Block Lock-down Bit, Set Read Configuration Register and Block Erase Resume command.

To resume the block erase operation, write the Block Erase Resume command (D0H) to the partition. Status Register bits SR.7 and SR.6 will be automatically cleared. After the Block Erase Resume command is written, the target partition automatically outputs the status register data when read. V_{PP} must remain at $V_{PPH1/2}$ (at the same level before block erase suspended) while block erase is suspended. RST# must remain at V_{IH} and WP# must also remain at V_{IL} or V_{IH} (at the same level before block erase suspended). Block erase cannot resume until (page buffer) program operation initiated during block erase suspend is completed. Figure 9 shows the block erase suspend and block erase resume flowchart.

If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.



Bus Operation	Command	Comments
Write	Block Erase Suspend	Data=B0H Addr=Within Partition
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.6 1=Block Erase Suspended 0=Block Erase Completed
Write	Block Erase Resume	Data=D0H Addr=Within Block to be Suspended

Figure 9. Block Erase Suspend and Block Erase Resume Flowchart

4.11 (Page Buffer) Program Suspend Command and (Page Buffer) Program Resume Command

The (Page Buffer) Program Suspend command (B0H) allows word and page buffer program interruption to read data from locations other than that which is suspended.

Once the (page buffer) program process starts in a partition, writing the (Page Buffer) Program Suspend command to the partition requests that the WSM suspends the (page buffer) program sequence at a predetermined point in the algorithm. Read operations to the target partition after writing the (Page Buffer) Program Suspend command access the status register. Status register bits SR.7 and SR.2 indicate if the (page buffer) program operation has been suspended (both will be set to "1"). Specification t_{WHRH1} or t_{EHRH1} defines the (page buffer) program suspend latency.

When the (Page Buffer) Program Suspend command is written after the completion of the (page buffer) program operation, the partition returns to read array mode. Therefore, the Read Status Register command (70H) must be written to the target partition after writing the (Page Buffer) Program Suspend command. If the status register bits SR.7 and SR.2 are set to "1", (page buffer) program has been suspended.

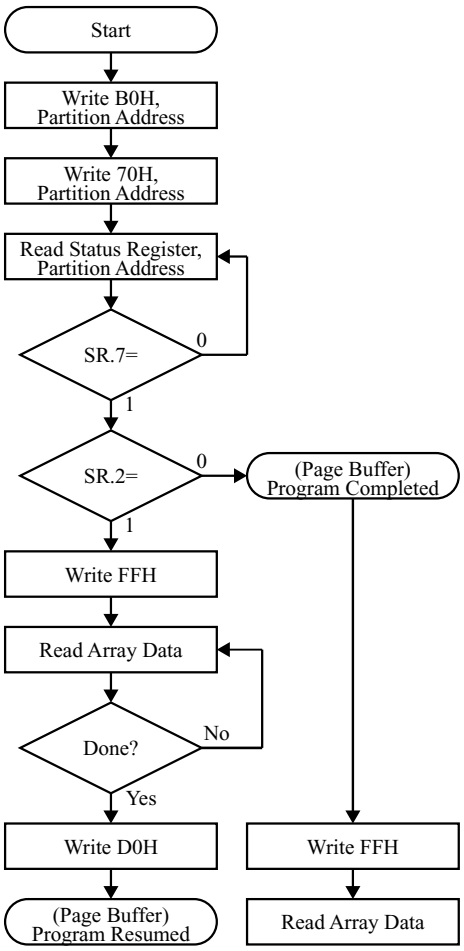
At this point, a Read Array command can be written to read data from locations other than that which is suspended.

The only other valid commands while (page buffer) program is suspended are Read Identifier Codes/OTP, Read Query, Read Status Register, Set Read Configuration Register and (Page Buffer) Program Resume command.

To resume the (page buffer) program operation, write the (Page Buffer) Program Resume command (D0H) to the partition. Status Register bits SR.7 and SR.2 will be automatically cleared. After the (Page Buffer) Program Resume command is written, the target partition automatically outputs the status register data when read. V_{PP} must remain at $V_{PPH1/2}$ (at the same level before (page buffer) program suspended) while (page buffer) program is suspended. RST# must remain at V_{IH} and WP# must also remain at V_{IL} or V_{IH} (at the same level before (page buffer) program suspended). Figure 10 shows the (page buffer) program suspend and (page buffer) program resume flowchart.

If the interval time from a (Page Buffer) Program Resume command to a subsequent (Page Buffer) Program Suspend command is short and its sequence is repeated, the (page buffer) program operation may not be finished.

After the (Page Buffer) Program Suspend command is written to the 1st partition to suspend the program operation while the 2nd partition is in block erase suspend mode, the (Page Buffer) Program Resume command should be written to the 1st partition first to resume the suspended (page buffer) program operation. After that, the Block Erase Resume command is written to the 2nd partition to resume the suspended block erase operation. If the Block Erase Resume command is written before the (Page Buffer) Program Resume command, the Block Erase Resume command is ignored and the partition to which the Block Erase Resume command is written is set to read array mode with block erase suspended.



Bus Operation	Command	Comments
Write	(Page Buffer) Program Suspend	Data=B0H Addr=Within Partition
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Standby		Check SR.2 1=(Page Buffer) Program Suspended 0=(Page Buffer) Program Completed
Write		Data=FFH Addr=Within Partition
Read		Read array locations from block other than that being programmed
Write	(Page Buffer) Program Resume	Data=D0H Addr=Location to be Suspended

Figure 10. (Page Buffer) Program Suspend and (Page Buffer) Program Resume Flowchart

4.12 Set Block Lock Bit Command

The LH28F320BX/LH28F640BX series is provided with a block lock bit for each parameter block and main block. The features of set block lock bit is as follows:

- Any block can be independently locked by setting its block lock bit.
- The time required for block locking is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Block erase, full chip erase or (page buffer) program on a locked block cannot be executed (see Table 11 and Table 12).
- At power-up or device reset, all blocks default to locked state, regardless of the states before power-off or reset operation.
  (Lock bit is volatile.)

The Set Block Lock Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be locked is written to the target partition. At the second cycle, command (01H) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock bit is set within the minimum command cycle time and the corresponding block is locked. To check the lock status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock/unlock status is represented by the output pin DQ_0. If the output of DQ_0 is "1", the block lock bit is set correctly. Figure 11 shows set block lock bit flowchart.

The two-cycle command sequence ensures that block is not accidentally locked. An invalid Set Block Lock Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

The Set Block Lock Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

At power-up or device reset, since all blocks default to locked state, write the Clear Block Lock Bit command described later to clear block lock bit before a erase or program operation.

Table 11. Functions of Block Lock(1) and Block Lock-Down

Current State					Erase/Program Allowed? (3)
State	WP#	DQ_1(2)	DQ_0(2)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](4)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](4)	1	0	1	Locked	No
[110](5)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

NOTES:
1. OTP (One Time Program) block has the lock function which is different from those described above.
2. DQ_0=1: a block is locked; DQ_0=0: a block is unlocked.
   DQ_1=1: a block is locked-down; DQ_1=0: a block is not locked-down.
3. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
4. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] (WP#=0) or [101] (WP#=1), regardless of the states before power-off or reset operation.
5. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

Table 12. Block Locking State Transitions upon Command Write(4)

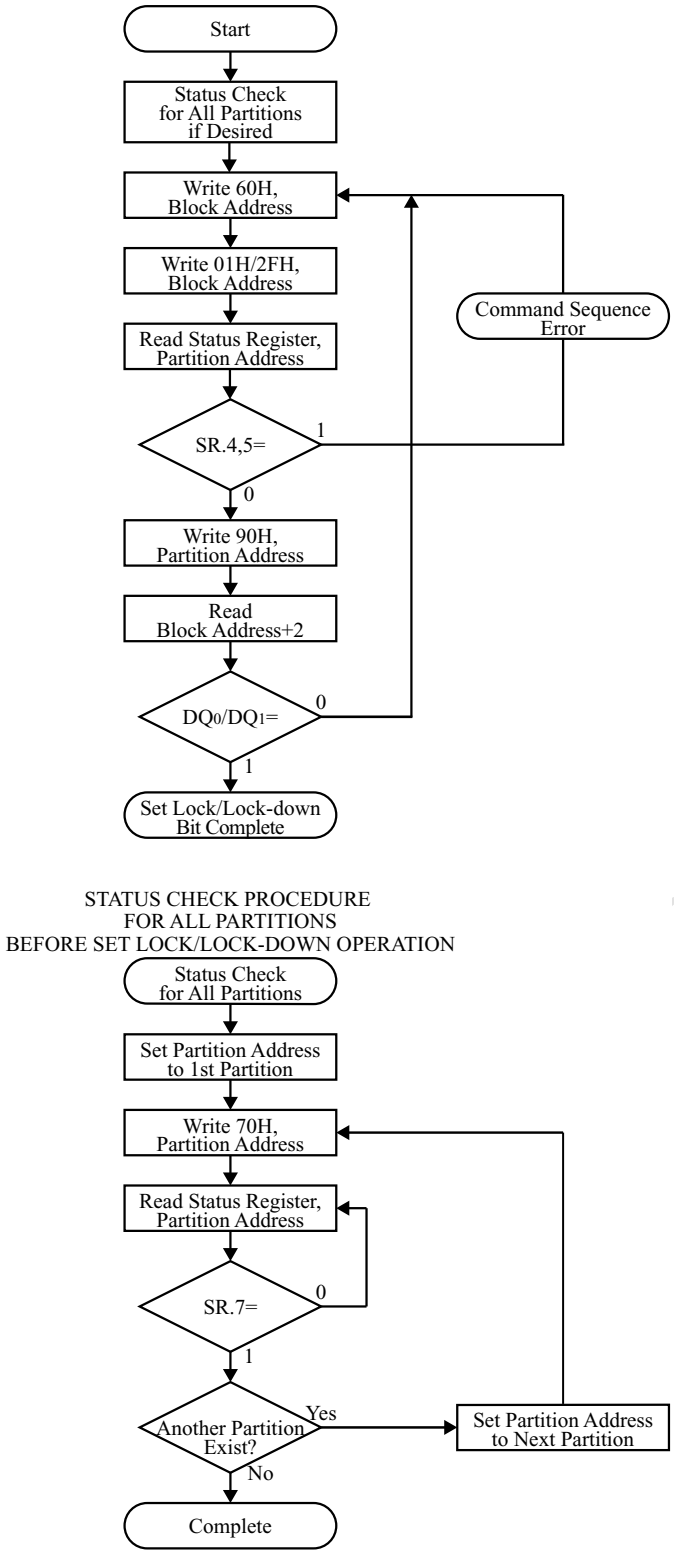
Current State				Result after Lock Command Written (Next State)		
State	WP#	DQ_1	DQ_0	Set Lock(1)	Clear Lock(1)	Set Lock-down(1)
[000]	0	0	0	[001]	No Change	[011](2)
[001]	0	0	1	No Change(3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111](2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111](2)
[111]	1	1	1	No Change	[110]	No Change

NOTES:
1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0=0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that WP# is not changed and fixed V_{IL} or V_{IH}.

Table 13. Block Locking State Transitions upon WP# Transition(4)

Previous State	Current State				Result after WP# Transition (Next State)	
	State	WP#	DQ_1	DQ_0	WP#=0→1(1)	WP#=1→0(1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110](2)	[011]	0	1	1	[110]	-
Other than [110](2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011](3)
-	[111]	1	1	1	-	[011]

NOTES:
1. "WP#=0→1" means that WP# is driven to V_{IH} and "WP#=1→0" means that WP# is driven to V_{IL}
2. State transition from the current state [011] to the next state depends on the previous state.
3. When WP# is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.



Bus Operation	Command	Comments
Write	Set Block Lock Bit/Set Block Lock-down Bit	<First cycle> Data=60H Addr=Within Block to be Locked or Locked-down
		<Second cycle> Data= 01H (Lock Bit), or 2FH(Lock-down Bit) Addr=Within Block to be Locked or Locked-down
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Lock Bit or Lock-down Bit Data Addr=Block Address+2 (see Table 6 through Table 8)
Standby		Check DQ_0/DQ_1 1=Lock Bit or Lock-down Bit is Set
Repeat for the subsequent set block lock/lock-down bit. Lock status check can be done after each set block lock/lock-down bit operation or after a sequence of set block lock/lock-down bit operations. SR.5 and SR.4 are only cleared by the Clear Status Register command in cases where multiple block lock/lock-down bits are set before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery. Write FFH after a sequence of set block lock/lock-down bit operations to place device in read array mode.		

STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE SET LOCK/LOCK-DOWN OPERATION

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 11. Set Block Lock Bit and Set Block Lock-down Bit Flowchart

4.13 Clear Block Lock Bit Command

A locked block can be unlocked by writing the Clear Block Lock Bit command. The features of clear block lock bit is as follows:

- Any block can be independently unlocked by clearing its block lock bit.
- The time required to be unlocked is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Block erase, full chip erase or (page buffer) program on an unlocked block can be executed (see Table 11 and Table 12).

The Clear Block Lock Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be unlocked is written to the target partition. At the second cycle, command (D0H) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock bit is cleared within the minimum command cycle time and the corresponding block is unlocked. To check the unlock status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock/unlock status is represented by the output pin DQ_0. If the output of DQ_0 is "0", the block lock bit is cleared correctly. Figure 12 shows clear block lock bit flowchart.

The two-cycle command sequence ensures that block is not accidentally unlocked. An invalid Clear Block Lock Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

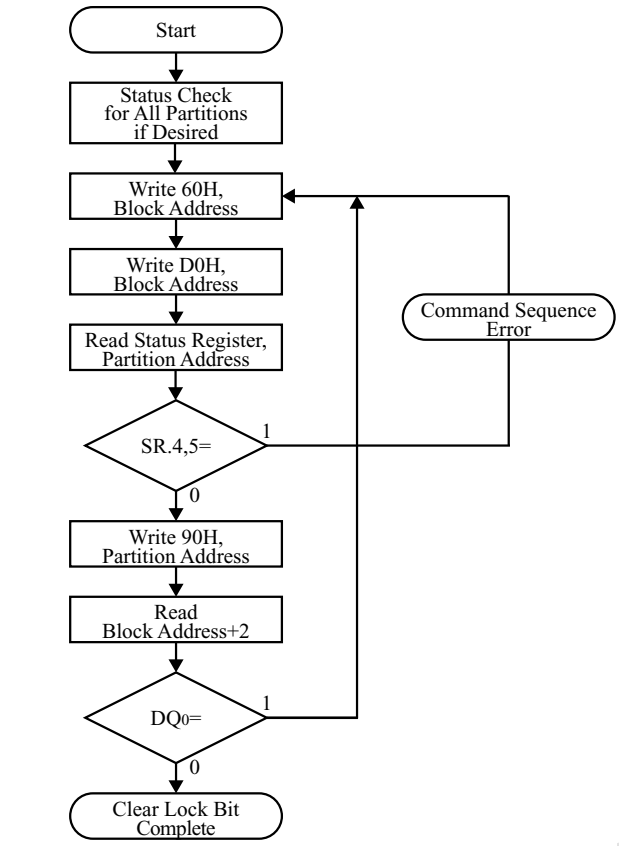
The Clear Block Lock Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

4.14 Set Block Lock-Down Bit Command

The block lock-down bit, when set, increases the security for data protection. The block lock-down bit has the following functions.

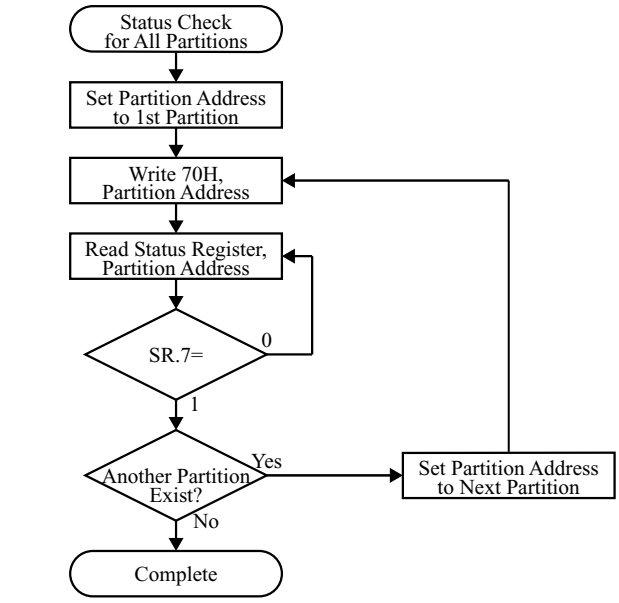
- Any block can be independently locked-down by setting its block lock-down bit.
- The time required to be locked-down is less than the minimum command cycle time (minimum time from the rising edge of CE# or WE# to write the command to the next rising edge of CE# or WE#).
- Locked-down block is automatically locked regardless of WP# at V_{IL} or V_{IH}.
- When WP# is V_{IL}, locked-down blocks are protected from lock status changes.
- When WP# is V_{IH}, the lock-down bits are disabled and locked-down blocks can be individually unlocked by software command. These blocks can then be re-locked and unlocked as desired while WP# remains V_{IH}. When WP# goes V_{IL}, blocks that were previously marked lock-down return to the lock-down state regardless of any changes made while WP# was V_{IH} (see Table 13).
- At power-up or device reset, all blocks are not locked-down regardless of the states before power-off or reset operation.
  (Lock-down bit is volatile.)
- Lock-down bit cannot be cleared by software, only by power-off or device reset.

The Set Block Lock-down Bit command is a two-cycle command. At the first cycle, command (60H) and an address within the block to be locked-down is written to the target partition. At the second cycle, command (2FH) and the same address as the first cycle is written. Read operations to the target partition output the status register data until another valid command is written. After writing the second cycle command, the block lock-down bit is set within the minimum command cycle time and the corresponding block is locked-down. To check the lock-down status, write the Read Identifier Codes/OTP command (90H) and an address within the target block. Subsequent reads at Block Base Address +2 (see Table 6 through Table 8) will output the lock/unlock status of that block. The lock-down status is represented by the output pin DQ_1. If the output of DQ_1 is "1", the block lock-down bit is set correctly. Figure 11 shows set block lock-down bit flowchart.



Bus Operation	Command	Comments
Write	Clear Block Lock Bit	<First cycle> Data=60H Addr=Within Block to be Unlocked
		<Second cycle> Data= D0H Addr=Within Block to be Unlocked
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Lock Bit Data Addr=Block Address+2 (see Table 6 through Table 8)
Standby		Check DQ_0 0=Lock Bit is Cleared
Repeat for the subsequent clear block lock bit. Lock status check can be done after each clear block lock bit operation or after a sequence of clear block lock bit operations. SR.5 and SR.4 are only cleared by the Clear Status Register command in cases where multiple block lock bits are cleared before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery. Write FFH after a sequence of clear block lock bit operations to place device in read array mode.		

STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE CLEAR LOCK OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 12. Clear Block Lock Bit Flowchart

The two-cycle command sequence ensures that block is not accidentally locked-down. An invalid Set Block Lock-down Bit command sequence will result in both status register bits SR.5 and SR.4 being set to "1" and the operation will not be executed.

The Set Block Lock-down Bit command is available when the power supply voltage is specified level, independent of the voltage on V_{PP}.

At power-up or device reset, since no blocks are locked-down, write the Set Block Lock-down Bit command as necessary.

While WP# is V_{IH}, the lock-down bits are disabled but not cleared. Once any block is locked-down, it cannot be cleared until power-off or device reset.

4.15 OTP Program Command

OTP program is executed by a two-cycle command sequence. At the first cycle, command (C0H) and an address within the OTP block (see Figure 4) is written, followed by the second write that specifies the address and data. After writing the command, the device outputs the status register data when any address within the device is selected. The WSM then takes over, controlling the internal OTP program algorithm. The system CPU can detect the OTP program completion by analyzing the output data of the status register bit SR.7. Figure 13.1 and Figure 13.2 show OTP program flowchart.

The address written at the command cycle must be the address within the OTP block (refer to Figure 4). Writing an address outside the OTP block will cause a OTP program error and the status register bit SR.4 is set to "1". Clear the status register before writing next command.

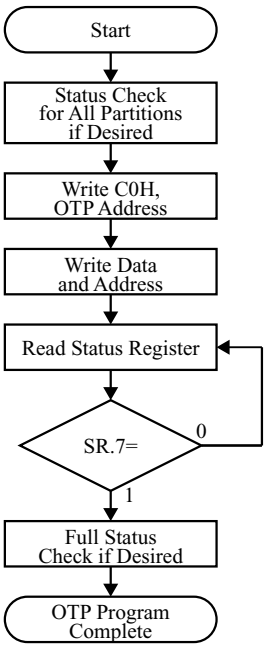
The internal WSM verify only detects errors for "1"s that are not successfully programmed to "0"s. Check the status register bit SR.4 at the end of OTP program. If a OTP program error is detected, the status register should be cleared before system software attempts corrective actions.

For reliable OTP program operation, apply the specified voltage on V_{CC} and $V_{PPH1/2}$ on V_{PP}. In the absence of this voltage, OTP program operations are not guaranteed. For example, attempting an OTP program at $V_{PP} \leq V_{PPLK}$ causes SR.4 and SR.3 being set to "1". OTP program operation on locked area causes SR.4 and SR.1 being set to "1" and the operation will not be executed.

OTP program cannot be suspended through the (Page Buffer) Program Suspend command (B0H). Even if the (Page Buffer) Program Suspend command is written during OTP program operation, the suspend command will be ignored.

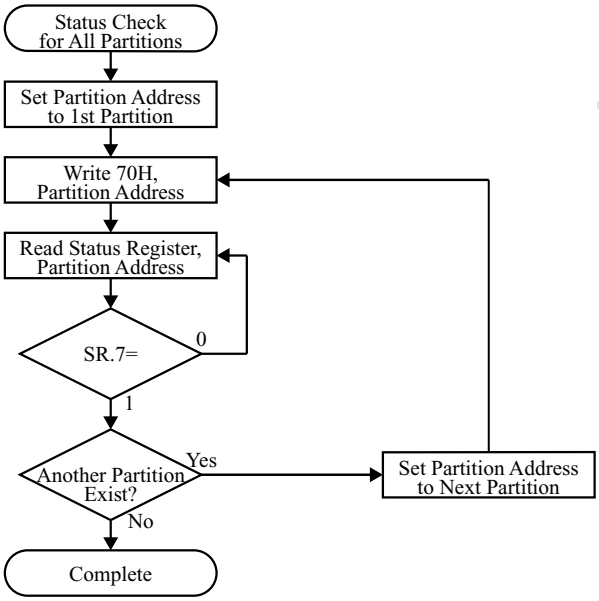
If an error is detected during the OTP program operation, error bits for all status registers are set to "1". This requires that the Clear Status Register command be written to all partitions to clear the error bits.

Dual work operation is not available while the OTP program mode, and the memory array data cannot be read even if that operation has been completed. To return to the read array mode, write the Read Array command (FFH) to the partition's CUI after the completion of the OTP program operation.



Bus Operation	Command	Comments
Write	OTP Program	<First cycle> Data=C0H Addr=Location to be Programmed
Write		<Second cycle> Data=Data to be Programmed Addr=Location to be Programmed
Read		Status Register Data Addr=X
Standby		Check SR.7 1=WSM Ready 0=WSM Busy
Repeat for subsequent OTP program. SR full status check can be done after each OTP program, or after a sequence of OTP programs. Write FFH after the OTP program operation to place device in read array mode.		

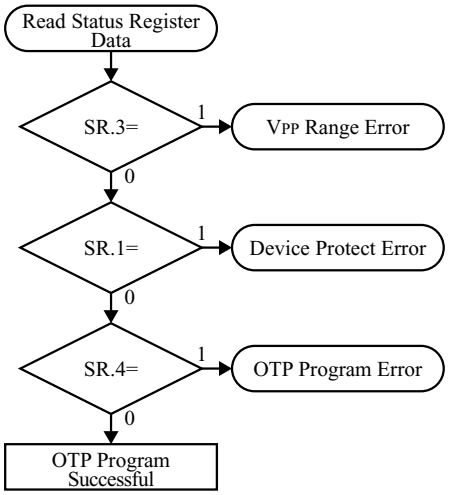
STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE OTP PROGRAM OPERATION



Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 13.1. Automated OTP Program Flowchart

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=V_{PP} Error Detect
Standby		Check SR.1 1=Device Protect Detect
Standby		Check SR.4 1=OTP Program Error
SR.4, SR.3 and SR.1 are only cleared by the Clear Status Register command in cases where multiple locations are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 13.2. Automated OTP Program Flowchart (Continued)

4.16 Set Read Configuration Register Command

The Read Configuration Register (RCR) bits are set by writing the Set Read Configuration Register command to the device.

This operation is initiated by a two-cycle command sequence. The read configuration register can be configured by writing the command with the read configuration register code. At the first cycle, command (60H) and a read configuration register code is written. At the second cycle, command (03H) and the same address as the first cycle is written. The read configuration register code is placed on the address bus, A_{15} - A_0, and is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first). The read configuration register code sets the device's read configuration, burst order, frequency configuration, and burst length. This command functions independently of the V_{PP} voltage. RST# must be at V_{IH}. After executing this command, the partition returns to read array mode. The read configuration register bits RCR.13-11, RCR.9, RCR.8, RCR.7, RCR.6, RCR.3 and RCR.2-0 are only valid for synchronous burst mode. Figure 16 shows set read configuration register flowchart.

NOTES:
- The read configuration register code can be read via the Read Identifier Codes/OTP command (90H). Address 0005H on A_{15} - A_0 contains the read configuration register code (see Table 6 through Table 8).
- All the bits in the read configuration register are set to "1" after device power-up or reset. (Read configuration register bits are volatile.)

4.16.1 Device Read Configuration (Read Mode)

Each partition supports a high performance synchronous burst mode read configuration. The read configuration register bit RCR.15 sets the device read configuration (read mode; see Table 14).

All the parameter and main blocks support asynchronous read mode, asynchronous 8-word page mode and synchronous burst mode configuration.

Status register, query code, identifier codes, OTP block and configuration register codes can only be read in single asynchronous or single synchronous read mode.

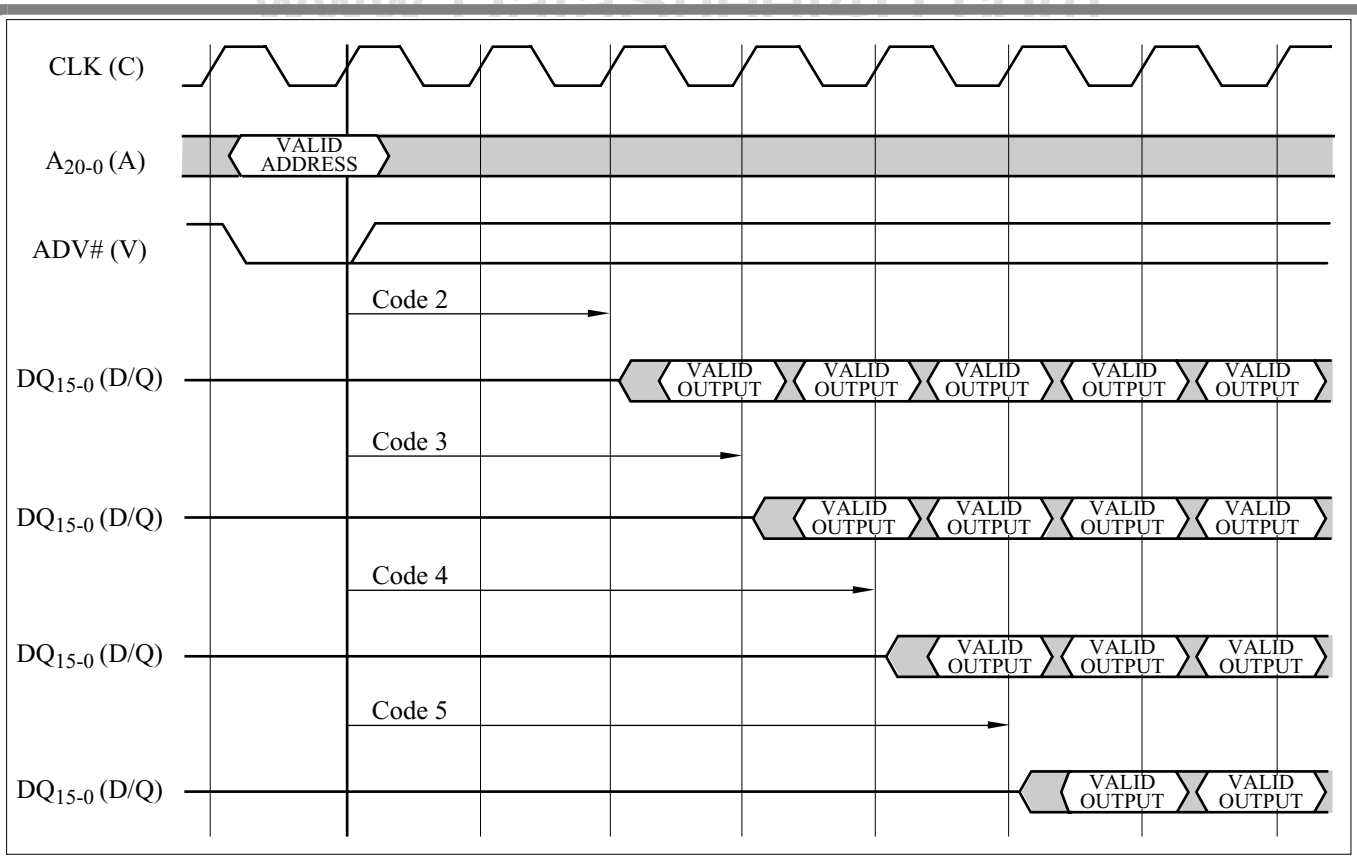


Figure 14. Frequency Configuration

••••• Synchronous burst mode will be available for future device.

Table 14. Read Configuration Register Definition

RM	R	FC2	FC1	FC0	R	DOC	WC
15	14	13	12	11	10	9	8
BS	CC	R	R	BW	BL2	BL1	BL0
7	6	5	4	3	2	1	0

RCR.15 = READ MODE (RM)
- 0 = Synchronous Burst Reads Enabled
- 1 = Asynchronous Reads Enabled (Default)

RCR.14 = RESERVED FOR FUTURE ENHANCEMENTS (R)

RCR.13-11 = FREQUENCY CONFIGURATION (FC2-0)
- 000 = Code 0 reserved for future use
- 001 = Code 1 reserved for future use
- 010 = Code 2
- 011 = Code 3
- 100 = Code 4
- 101 = Code 5
- 110 = Code 6 reserved for future use
- 111 = Code 7 reserved for future use (Default)

RCR.10 = RESERVED FOR FUTURE ENHANCEMENTS (R)

RCR.9 = DATA OUTPUT CONFIGURATION (DOC)
- 0 = Hold Data for One Clock
- 1 = Hold Data for Two Clocks (Default)

RCR.8 = WAIT# CONFIGURATION (WC)
- 0 = WAIT# Asserted During Delay
- 1 = WAIT# Asserted One Data Cycle Before Delay (Default)

RCR.7 = BURST SEQUENCE (BS)
- 0 = Intel Burst Order
- 1 = Linear Burst Order (Default)

RCR.6 = CLOCK CONFIGURATION (CC)
- 0 = Burst Starts and Data Output on Falling Clock Edge
- 1 = Burst Starts and Data Output on Rising Clock Edge (Default)

RCR.5-4 = RESERVED FOR FUTURE ENHANCEMENTS (R)

RCR.3 = BURST WRAP (BW)
- 0 = Wrap Burst Reads within Burst Length set by RCR.2-0
- 1 = No Wrap Burst Reads within Burst Length set by RCR.2-0 (Default).

RCR.2-0 = BURST LENGTH (BL2-0)
- 001 = 4 Word Burst
- 010 = 8 Word Burst
- 011 = Reserved for future use
- 111 = Continuous (Linear) Burst (Default)

NOTES:

Read configuration register affects the read operations from main and parameter blocks. Read operations for status register, query code, identifier codes, OTP block and device configuration codes support single read cycles.

RCR.14, RCR.10, RCR.5 and RCR.4 bits are reserved for future use.

Refer to Frequency Configuration in Section 4.16.2 for information about the frequency configuration RCR.13-11.

Undocumented combinations of bits RCR.13-11 are reserved by Sharp Corporation for future implementations and should not be used.

Refer to Section 4.16.7 for information about Burst Wrap configuration RCR.3.

In the asynchronous page mode, the burst length always equals 8 words.

All the bits in the read configuration register are set to "1" after power-up or device reset.

When the bit RCR.15 is set to "1", other bits are invalid.

Table 15. Frequency Configuration Settings

Read Configuration Register			Frequency Configuration Code	Input Clock Frequency	
RCR.13	RCR.12	RCR.11		TBD ns	TBD ns
0	1	0	2	≤ 24MHz	≤ TBD MHz
0	1	1	3	≤ 36MHz	≤ TBD MHz
1	0	0	4	≤ 40MHz	≤ TBD MHz
1	0	1	5	≤ TBD MHz	≤ TBD MHz

4.16.2 Frequency Configuration

The read configuration register bits RCR.13, RCR.12 and RCR.11 indicates the frequency configuration (see Table 14). The frequency configuration informs the number of clocks that must elapse after ADV# is driven active (V_{IL}) before data will be available. This value is determined by the input clock frequency. See Table 15 for the specific input CLK frequency configuration. Figure 14 shows data output latency from ADV# going V_{IL} for different frequency configuration codes.

4.16.3 Data Output Configuration

The data output configuration, shown by RCR.9 (see Table 14), determines the number of clocks that data will be held valid. The data hold time for the LH28F320BX/ LH28F640BX series can be set to one clock or two clocks (see Figure 15).

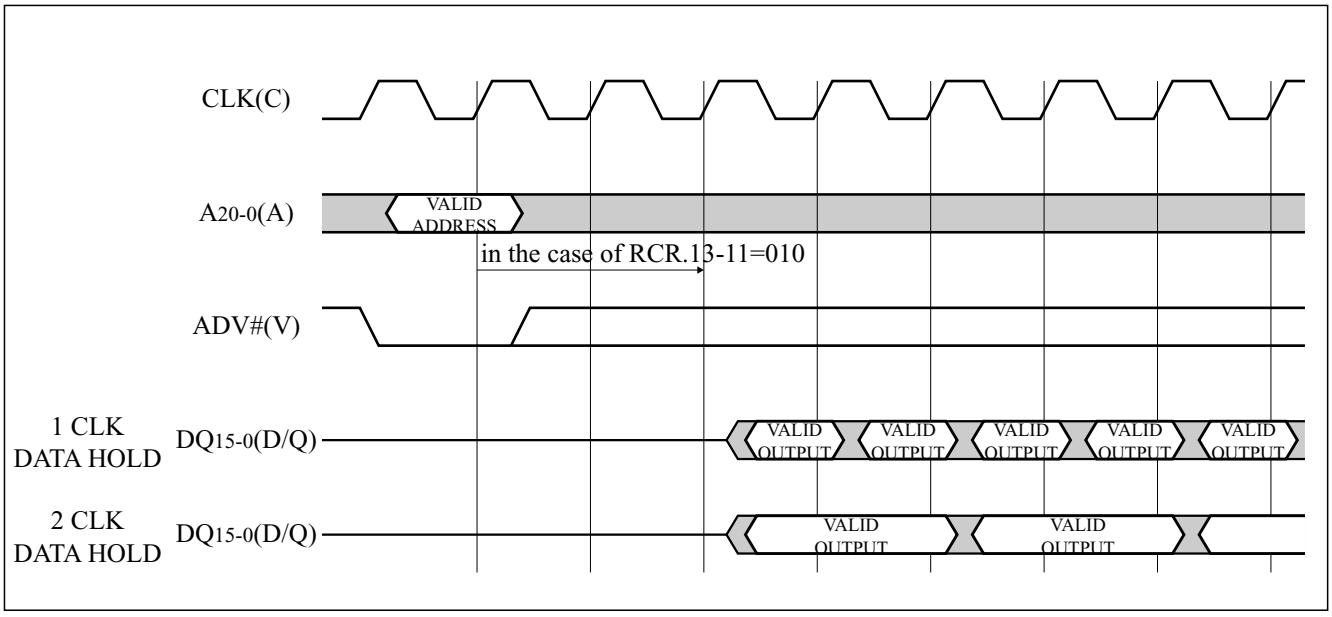


Figure 15. Output Configuration

••••• Synchronous burst mode will be available for future device.

4.16.4 WAIT# Configuration

The WAIT# configuration bit RCR.8 (see Table 14) controls the WAIT# output signal. This output signal can be set to be asserted during or one CLK cycle before an output delay occurs, when the burst read crosses the first 64-word boundary in continuous burst length or the 4- or 8-word burst length with no-wrap mode. Its setting will depend on the system and CPU characteristic.

4.16.5 Burst Sequence

The burst sequence bit RCR.7 (see Table 14) determines the order in which data is addressed in synchronous burst mode. This order is configurable to either linear or Intel burst order. The continuous burst length only supports linear burst order. The order will be determined by the CPU characteristic. Refer to Table 16 for linear burst order and Intel burst order in detail.

4.16.6 Clock Configuration

The clock configuration bit RCR.6 (see Table 14) configures the device to start a burst cycle, output data, and assert WAIT# on the rising or falling edge of the clock. This CLK flexibility enables interfacing the LH28F320BX/LH28F640BX series Flash memory to a wide range of burst CPUs.

4.16.7 Burst Wrap

The burst wrap bit RCR.3 (see Table 14) determines the wrap mode as follows.

- 4- or 8-word burst-accesses are performed within the burst-length boundary in wrap mode (RCR.3="0").
- 4- or 8-word and continuous burst-accesses cross the burst-length boundaries in no-wrap mode (RCR.3="1").
  No-wrap mode is only valid for linear burst order (RCR.7="1").

No-wrap mode (RCR.3="1") enables WAIT# to hold off the system processor, as it does in the continuous burst mode. In the no-wrap mode, the device operates similar to continuous linear burst mode but consumes less power during 4- and 8-word bursts. Refer to Table 16 for burst wrap in detail.

For example, if RCR.3="0" (wrap mode) and RCR.2-0=001 (4-word burst length), then possible linear burst sequences are 0-1-2-3, 1-2-3-0, 2-3-0-1 and 3-0-1-2.

If RCR.3="1" (no-wrap mode) and RCR.2-0=001 (4-word burst length), then possible linear burst sequences are 0-1-2-3, 1-2-3-4, 2-3-4-5 and 3-4-5-6. No-wrap mode not only enables limited non-aligned sequential burst, but also reduces power by minimizing the number of internal read operations.

4.16.8 Burst Length

The burst length is the number of words that the device will output. The read configuration register bits RCR.2-0 (see Table 14) set the burst length. The LH28F320BX/LH28F640BX series supports burst lengths of four and eight words. It also supports a continuous burst mode. In continuous burst mode, the device will linearly output data until the internal burst counter reaches the end of the device's burst-able address space or a partition boundary. Refer to Table 16 for burst length in detail.

4.16.8.1 Continuous Burst Length

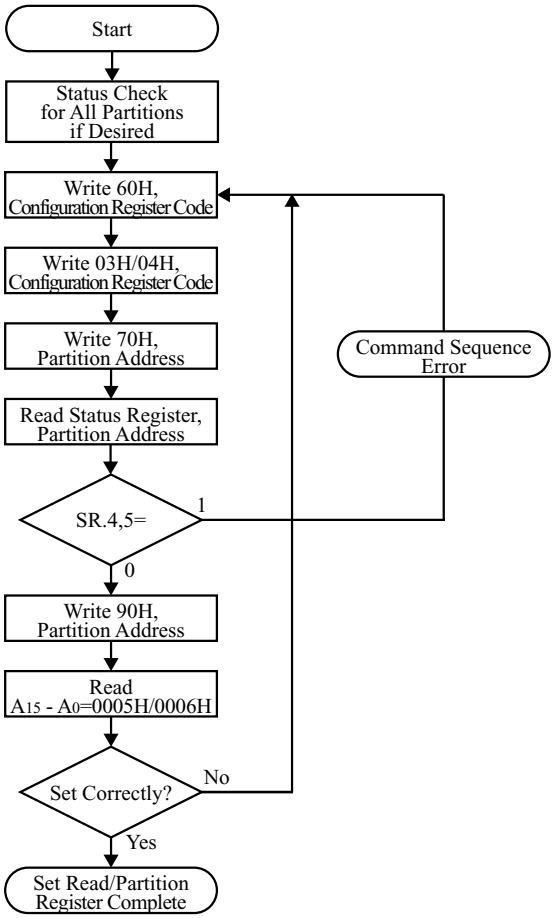
In continuous burst mode or 4-, 8-word burst with no-wrap (RCR.3="1") mode, the flash memory may cause an output delay when the burst read crosses the first 64-word boundary. It depends on the starting address whether an output delay will occur or not. When the starting address is aligned to a 64-word boundary, the delay will not occur. If the starting address is the end of a 64-word boundary, the output delay will be equal to the frequency configuration setting; this is the worst case delay. The delay will only take place once during a continuous burst access. If the burst read never crosses a 64-word boundary, the delay will never happen. The WAIT# output pin is used in continuous burst mode or 4-, 8-word burst with no-wrap mode to inform the system if this output delay occurs.

Table 16. Read Sequence and Burst Length

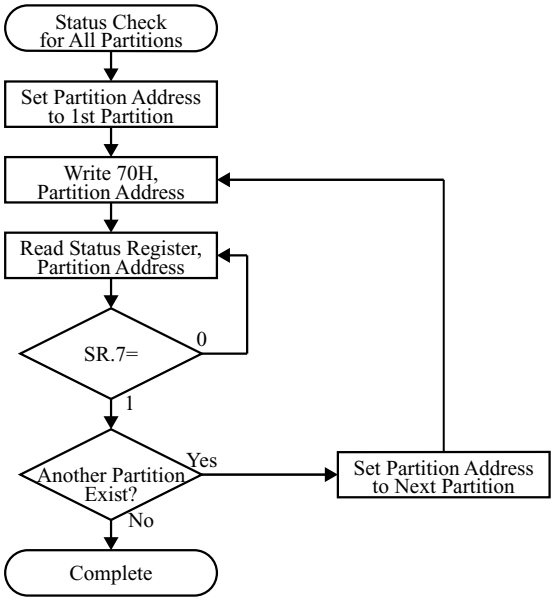
Starting Address [Decimal]	Burst Wrap(1) (RCR.3=)	Burst Addressing Sequence [Decimal]				
		4-Word Burst Length (RCR.2-0=001)		8-Word Burst Length (RCR.2-0=010)		Cotinuous Burst (RCR.2-0=111)
		Linear	Intel	Linear	Intel	Linear
0	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6…
1	0	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7…
2	0	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8…
3	0	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9…
4	0			4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10…
5	0			5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11…
6	0			6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12…
7	0			7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	0					14-15-16-17-18-19-20…
15	0					15-16-17-18-19-20-21…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	0-1-2-3	NA	0-1-2-3-4-5-6-7	NA	0-1-2-3-4-5-6…
1	1	1-2-3-4	NA	1-2-3-4-5-6-7-8	NA	1-2-3-4-5-6-7…
2	1	2-3-4-5	NA	2-3-4-5-6-7-8-9	NA	2-3-4-5-6-7-8…
3	1	3-4-5-6	NA	3-4-5-6-7-8-9-10	NA	3-4-5-6-7-8-9…
4	1			4-5-6-7-8-9-10-11	NA	4-5-6-7-8-9-10…
5	1			5-6-7-8-9-10-11-12	NA	5-6-7-8-9-10-11…
6	1			6-7-8-9-10-11-12-13	NA	6-7-8-9-10-11-12…
7	1			7-8-9-10-11-12-13-14	NA	7-8-9-10-11-12-13…
⋮	⋮	⋮	⋮	⋮	⋮	⋮
14	1					14-15-16-17-18-19-20…
15	1					15-16-17-18-19-20-21…

NOTE:

1. The burst wrap bit (RCR.3) determines whether 4- or 8-word burst-accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses.
   In the no-wrap mode (RCR.3=1), the device operates similar to continuous linear burst mode but consumes less power during 4- and 8-word bursts.



STATUS CHECK PROCEDURE
FOR ALL PARTITIONS
BEFORE SET READ/PARTITION
CONFIGURATION REGISTER OPERATION



Bus Operation	Command	Comments
Write	Set Read Configuration Register, Set Partition Configuration Register	<First cycle> Data=60H Addr=Configuration Register Code (see Table 14 or Table 17)
		<Second cycle> Data= 03H (Read Configuration), or 04H(Partition Configuration) Addr=Configuration Register Code (see Table 14 or Table 17)
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.4, 5 Both 1=Command Sequence Error
Write	Read ID Code	Data=90H Addr=Within Partition
Read		Read/Partition Configuration Register Code Addr=0005H/0006H (see Table 6 through Table 8)
Standby		Check DQ_{15}-DQ_0 for Read/ Partition Configuration Register Code
Configuration register code can be read after set read/ partition configuration register operation. SR.5 and SR.4 are only cleared by the Clear Status Register command. If an error is detected, clear the status register before attempting retry or other error recovery. After a successful set read/partition configuration register operation, the device returns to read array mode.		

Bus Operation	Command	Comments
Write	Read Status Register	Data=70H Addr=Within Partition
Read		Status Register Data Addr=Within Partition
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

Figure 16. Set Read Configuration Register and Set Partition Configuration Register Flowchart

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••••• Synchronous burst mode will be available for future device.

4.17 Set Partition Configuration Register Command

The Partition Configuration Register (PCR) bits are set by writing the Set Partition Configuration Register command to the device.

This operation is initiated by a two-cycle command sequence. The partition configuration register can be configured by writing the command with the partition configuration register code. At the first cycle, command (60H) and a partition configuration register code is written. At the second cycle, command (04H) and the same address as the first cycle is written. The partition configuration register code is placed on the address bus, A_{15} - A_0, and is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first). The partition configuration register code sets the partition boundaries. This command functions independently of the V_{PP} voltage. RST# must be at V_{IH}. After executing this command, the device returns to read array mode and status registers are cleared. Figure 16 shows set partition configuration register flowchart.

NOTES:
- The partition configuration register code can be read via the Read Identifier Codes/OTP command (90H). Address 0006H on A_{15} - A_0 contains the partition configuration register code (see Table 6 through Table 8).
- Partition configuration after device power-up or reset is as follows.
  (Partition configuration register bits are volatile.)
  Plane 0-2 are merged into one partition.
  (top parameter device)
  Plane1-3 are merged into one partition.
  (bottom parameter device)

4.17.1 Partition Configuration

The partition configuration shown in Table 17 determines the partiton boundaries for the dual work (simultaneous read while erase/program) operation. The partition boundaries can be set to any plane boundaries. If the partition configuration register bits PCR.10-8 (PC.2-0) are set to "001", the partition boundary is set between plane0 and plane1. There are two partitions in this configuration. Plane1-3 are merged to one partition. Status registers for plane1-3 are also merged to one. If the partition configuration register bits are set to "101", the partition boundaries are set between plane0 and plane1 and between plane2 and plane3. There are three partitions in this configuration. Plane1-2 are merged to one partition. If the partition configuration register bits are set to "111", there are four partitions. Each partition is just the same as each plane. Figure 17 illustrates the various partition configuration.

Table 17. Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

NOTES:

1. After power-up or device reset, PCR10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.
2. See Figure 17 for the detail on partition configuration.
3. PCR.15-11 and PCR.7-0 bits are reserved for future use. If these bits are read via the Read Identifier Codes/OTP command, the device may output "1" or "0" on these bits.

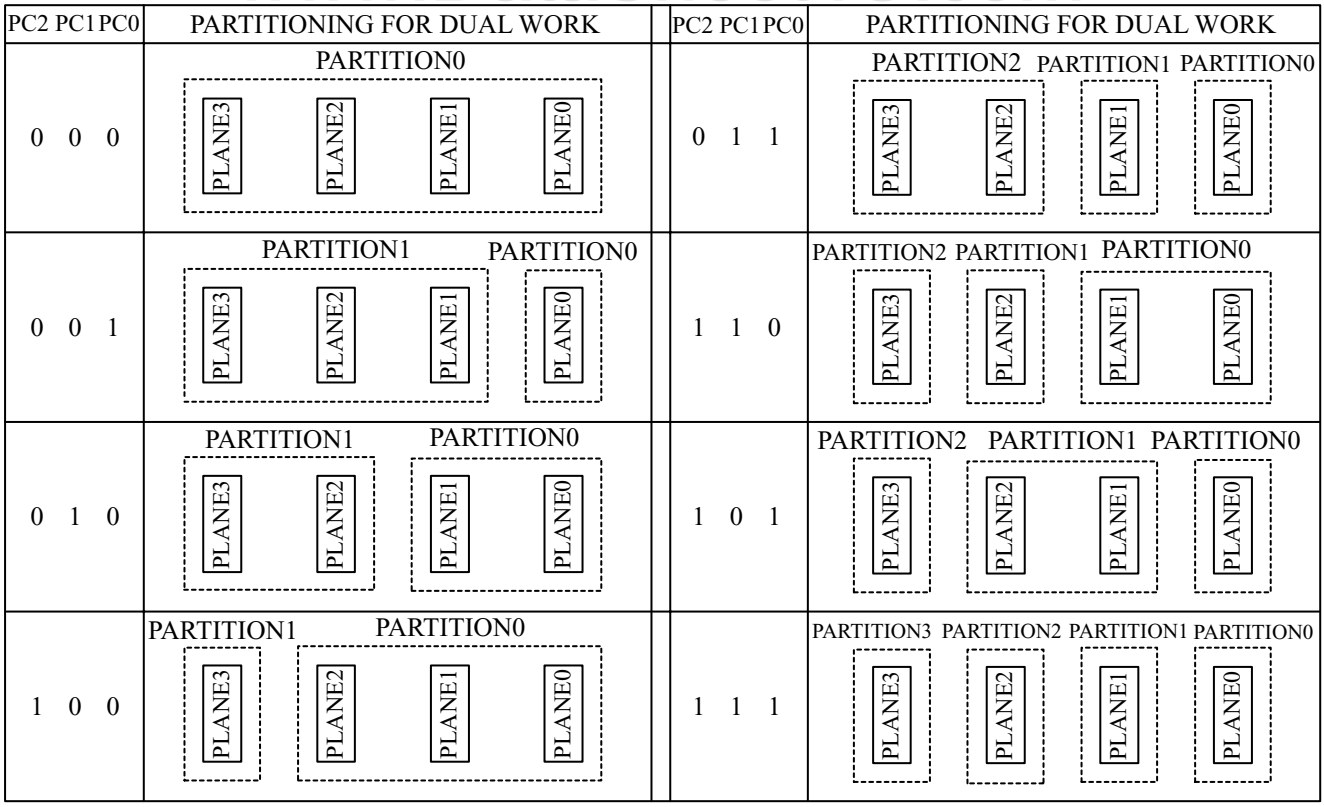

Figure 17. Partition Configuration

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5 Design Considerations

5.1 Hardware Design Considerations

5.1.1 Control using RST#, CE# and OE#

The device will often be used in large memory arrays. SHARP provides three control input pins to accommodate multiple memory connection. Three control input pins, RST#, CE# and OE# provide for:

- Minimize the power consumption of the memory
- Avoid data confliction on the data bus

To effectively use these control input pins, access the desired memory by enabling the CE# through the address decoder. Connect OE# to READ# control signal of all memory devices and system. With these connections, the selected memory devices are activated and deselected memory devices are in standby mode. RST# should be connected to the system POWERGOOD signal to prevent unintended writes during system power transitions. POWERGOOD should toggle (once set to V_{IL}) during system reset.

5.1.2 Power Supply Decoupling

Flash memory's power switching characteristics require careful device decoupling for eliminating noises to the system power lines. System designers should consider standby current levels (I_{CCS}), active current levels (I_{CCR}) and transient peaks produced by falling and rising edges of CE# and OE#. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each flash device should have a 0.1µF ceramic capacitor connected between each V_{CC}, V_{CCQ} and GND and between V_{PP} and GND (when V_{PP} is used as 12V supply). These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads. Additionally, for every eight devices, a 4.7µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. These capacitors will overcome voltage slumps caused by circuit board trace inductance.

5.1.3 V_{PP} Traces on Printed Circuit Boards

The V_{PP} pin on the LH28F320BX/LH28F640BX series Flash memory is only used to monitor the power supply voltage and is not used for a power supply pin except for 12V supply. Therefore, even when on-board writing to the flash memory on the system, it is not required to consider that V_{PP} supplies the currents on the printed circuit boards.

However, in erase or program operations with applying 12V±0.3V to V_{PP} pin, V_{PP} is used for the power supply pin. When executing these operations, V_{PP} trace widths and layout should be similar to that of V_{CC} to supply the flash memory cells current for erasing or programming. Adequate V_{PP} supply traces, and decoupling capacitors placed adjacent to the component, will decrease spikes and overshoots.

5.1.4 V_{CC}, V_{PP}, RST# Transitions

If V_{PP} is lower than V_{PPLK}, V_{CC} is lower than V_{LKO}, or RST# is not at V_{IH}, block erase, full chip erase, (page buffer) program and OTP program operation are not guaranteed. When V_{PP} error is detected, the status register bits SR.5 or SR.4 (depending on the attempted operation) and SR.3 will be set to "1". If RST# transitions to V_{IL} during the block erase, full chip erase, (page buffer) program or OTP program operation, the status register bit SR.7 will remain "0" until reset operation has been completed. Then, the attempted operation will be aborted and the device will enter reset mode after the completion of the reset sequence. If RST# is taken V_{IL} during a block erase, full chip erase, (page buffer) program or OTP program operation, the memory contents at the aborted location are no longer valid. Therefore, the proper command must be written again. And also, if V_{CC} transitions to lower than V_{LKO} during a block erase, full chip erase, (page buffer) program or OTP program operation, the attempted operation will be aborted and the memory contents at the aborted location are no longer valid. Write the proper command again after V_{CC} transitions above V_{LKO}.

5.1.5 Power-Up/Down Protection

The LH28F320BX/LH28F640BX series is designed to offer protection against accidental block erase, full chip erase, (page buffer) program, OTP program due to noises during power transitions. When the device power-up, holding V_{PP} and RST# to GND until V_{CC} has reached the specified level and in stable. For additional information, please refer to the AP-007-SW-E *RST#, V_{PP} Electric Potential Switching Circuit*. After power-up, the LH28F320BX/LH28F640BX series defaults to the mode described in Section 2.1.

System designers must guard against spurious writes when V_{CC} voltages are above V_{LKO} and V_{PP} voltages are above V_{PPLK}, by referring to Section 5.3 and the following design considerations. Since both CE# and WE# must be at V_{IL} for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection because alternation of memory contents can only occur after successful completion of the two-step command sequences.

The individual block locking scheme, which enables each block to be independently locked, unlocked or locked-down, prevents the accidental data alternation. The device is also disabled until RST# is brought to V_{IH}, regardless of the state of its control inputs. By holding the device in reset during power-up/down, invalid bus conditions can be masked, providing yet another level of memory protection.

5.1.6 Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. The LH28F320BX/LH28F640BX series' nonvolatility increases usable battery life because data is retained when system power is removed.

5.1.7 Automatic Power Savings

Automatic Power Savings (APS) provides low-power operation during active mode. APS mode allows the flash memory to put itself into a low current state when not being accessed. After data is read from the memory array and addresses not switching, the device enters the APS mode where typical I_{CC} current is comparable to I_{CCS}. The flash memory stays in this static state with outputs valid until a new location is read. Standard address access timings (t_{AVQV}) provide new data when addresses are changed. During dual work operation (one partition being erased or programmed, while other partitions are one of read modes), the device cannot enter the APS mode even if the input address remains unchanged.

5.1.8 Reset Operation

During power-up/down or transitions of power supply voltage, hold the RST# pin at V_{IL} to protect data against noises which are caused by invalid bus conditions and initialize the internal circuitry in flash memory. Bringing RST# to V_{IL} resets the internal WSM (Write State Machine) and sets the status register to 80H.

After return from reset, a time t_{PHQV} is required until outputs are valid, and a delay, t_{PHWL} and t_{PHEL}, is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored.

5.2 Software Design Considerations

5.2.1 WSM (Write State Machine) Polling

The status register bit SR.7 provides a software method of detecting block erase, full chip erase, (page buffer) program and OTP program completion. After the Block Erase, Full Chip Erase, (Page Buffer) Program or OTP Program command is written to the CUI (Command User Interface), SR.7 goes to "0". It will return to "1" when the WSM (Write State Machine) has completed the internal algorithm.

The status register bit SR.7 is "1" state when the device is in the following mode.

- The device can accept the next command.
- Block erase is suspended and (page buffer) program operation is not executed.
- (Page buffer) program is suspended.
- Reset mode

5.2.2 Attention to Program Operation

Do not *re*-program "0" data for the bit in which "0" has been already programmed. This *re*-program operation may generate the bit which cannot be erased.

To change the data from "1" to "0", take the following steps.

- Program "0" for the bit in which you want to change the data from "1" to "0".
- Program "1" for the bit in which "0" has been already programmed.
  (When "1" is programmed, erase/program operations are not executed onto the memory cell in flash memory.)

For example, changing the data from "10111101" to "10111100" requires "11111110" programmed.

5.3 Data Protection Method

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto WE# signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

♦ The below describes data protection method.

1) Protection of data in each block

- Any locked block by setting its block lock bit is protected against the data alternation. When WP# is V_{IL}, any locked-down block by setting its block lock-down bit is protected from lock status changes.
  By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
- For detailed block locking scheme, refer to Sections 4.12 to 4.14.

2) Protection of data with V_{PP} control

- When the level of V_{PP} is lower than V_{PPLK} (V_{PP} lockout voltage), write functions to all blocks including OTP block are disabled. All blocks are locked and the data in the blocks are completely protected.

3) Protection of data with RST#

- Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing RST# to V_{IL}, which inhibits write operation to all blocks including OTP block.
- For detailed description on RST# control, refer to Section 5.1.5.

♦ Protection against noises on WE# signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on WE# signal.

5.4 High Performance Read Mode

5.4.1 CPU Compatibility

LH28F320BX/LH28F640BX series supports two high-performance read modes for the parameter and main blocks:

- Asynchronous read mode in which 8-word page mode is available
- Synchronous burst mode

These two read modes provide much higher read accesses than was previously used.

The asynchronous read mode is suitable for non-clocked memory systems and is compatible with standard page-mode ROM. If the memory subsystem has access to an external processor referenced clock, the synchronous burst mode is available for increased read performance. The clock frequency for synchronous burst mode is described in specifications. If the system CPU or ASIC does not support page-mode or burst accesses, single asynchronous and synchronous read modes can be used.

It depends on the setting in the read configuration register which read mode is available. When the read configuration register bit RCR.15 is set to "1", the device is in asynchronous read mode. If the bit RCR.15 is set to "0", the device is in synchronous burst mode. Upon reset, the device defaults to asynchronous read mode and is put into read array mode.

5.4.2 Features of ADV# and CLK

ADV# and CLK pins are important for synchronous burst mode.

- ADV# can be derived from the processor's transaction start signal. If the processor does not have this type of signal, other standard CPU control signals can be used to control ADV#. ADV# must toggle to inform the flash memory to latch a new address.
  If this signal is not used in asynchronous read mode, CE# must toggle to inform the flash memory of a new address.
- CLK can be derived from the processor's memory clock output. If the processor does not supply this control signal to the memory subsystem, the signal can be received from the clock signal generator through a clock buffer. This buffer minimizes clock load and skew.

5.4.3 Address Latch

The internal address latch latches the address for read and write operations. The address latch is controlled by ADV#. When ADV# is V_{IL}, the latch is open. The latch closes when ADV# is driven high or upon the first rising (or falling) edge of CLK while ADV# is V_{IL}. This stores the current address on the bus into the flash memory device and lets the address bus change without affecting the flash. This pin works the same in write operations; the address to be written to the CUI is latched on the rising ADV# edge. Since write operations are asynchronous mode, CLK is ignored and the address is not latched on the clock edge. In asynchronous read mode, the address latch does not need to be used but addresses must then stay stable during the entire read operation. If ADV# is not used, which is fixed V_{IL}, in asynchronous mode, addresses are latched on the rising edge of CE# during reads and on the rising edge of CE# or WE# whichever goes high first during writes.

5.4.4 Using Asynchronous Page Mode

After initial power-up or reset mode, the device defaults to asynchronous read mode in which 8-word page mode is available. The asynchronous page mode is available for the parameter and main blocks, and is not supported from other locations within the device, such as the status register, identifier codes, OTP block and query codes. In asynchronous page mode, CLK is ignored and ADV# must be held V_{IL} throughout the page access. Holding ADV# V_{IL} allows new page mode accesses. The initial valid address will store 8 words of data in the internal page buffer. Each word is then output onto the data bus by toggling the address A_{2-0}.

If the asynchronous page mode is only used, CLK and ADV# can be tied to GND. Holding CLK and ADV# GND will minimize the power consumed by these two pins and will simplify the interface, making it compatible with standard flash memory and industry standard page mode ROMs. With ADV# at V_{IL}, the addresses cannot be latched into the device. Therefore, addresses must stay valid throughout the entire read cycle until CE# goes to V_{IH}. Figure 18 shows a waveform for asynchronous page mode read timing with ADV# held low. Note that the address A_{2-0} must be toggled to output the page-mode data.

In asynchronous read mode, the output of WAIT# is fixed to V_{OH}.

••••• Synchronous burst mode will be available for future device.

5.4.5 Using Synchronous Burst Mode

Synchronous burst mode provides a performance increase over asynchronous read mode. It supports effective zero wait-state performance up to the frequency described in specifications. The synchronous burst mode is available for the parameter and main blocks, and is not supported from other locations within the device, such as the status register, identifier codes, OTP block and query codes. It is not possible to do a synchronous burst read across the partition boundary. Figure 19 illustrates a waveform for synchronous burst mode read timing. The valid addresses are asserted, and then the device will output the first data after certain delay time. Subsequent data will be output every CLK cycle.

There are two different considerations for an external interface logic whether or not the processor supports synchronous burst mode at boot-up.

- Case 1, the processor does not support synchronous burst mode at boot-up, but rather boots up in asynchronous read mode. This is the initial mode of the flash memory, so no special design considerations need to be made. After booting up, the processor can configure the read configuration register for synchronous burst mode.
- Case 2, the processor does support synchronous burst mode at boot-up. After return from reset, the flash memory defaults to asynchronous read mode, which is inherently slower than synchronous burst mode. External interface logic will be needed to inform the processor of this, and to insert wait states to match the flash memory's timing with the processor's timing. This logic is only necessary until the processor has a chance to set the flash memory device to synchronous burst mode, at which time the external logic must be notified of this change. This can be accomplished via a write-able register within the system wait-state logic or via a general purpose I/O (GPIO) pin. The GPIO pin may operate as an input into the system logic.

5.4.6 Using WAIT# in Burst Mode

LH28F320BX/LH28F640BX series supports 4-word, 8-word and continuous burst modes. In continuous burst mode or 4-, 8-word burst with no-wrap (RCR.3="1") mode, WAIT# informs the system CPU whether output data is valid or not (refer to Section 4.16.8.1).

- WAIT#="1": there is valid data on the bus.
- WAIT#="0": the data on the bus is invalid.

When the output delay is encountered, the WAIT# pin will be asserted at a logic "0". This signal should be fed into the systems wait-state control logic or directly to the CPU. The WAIT# output pin is gated by CE# and OE#. If either CE# or OE# go to V_{IH}, the WAIT# output buffer turns off. An internal pull-up resistor holds WAIT# at a logic "1" state. Figure 20 shows a waveform for an output delay timing with ADV# at a logic "0".

WAIT# can be configured for assertion during the delay or one data cycle before the delay by setting the read configuration register bit RCR.8.

5.4.7 Single Read Mode

The following data can only be read in single asynchronous read mode or single synchronous read mode.

- Status register
- Query code
- Manufacturer code
- Device code
- Block lock configuration code
- Read configuration register code
- Partition configuration register code
- OTP block

A waveform of read timing for single asynchronous read mode and single synchronous read mode are shown in Figure 21 and Figure 22, respectively.

Single asynchronous read mode is compatible with previous SHARP flash memory devices. CLK is ignored in this mode. The valid addresses are asserted, and then the device will output data after certain delay time, such as t_{AVQV}, t_{VLQV}, t_{ELQV} or t_{GLQV}. Addresses are latched on the rising edge of ADV#. If ADV# is held V_{IL}, addresses must stay valid throughout the entire read cycle until CE# goes to V_{IH}.

In single synchronous read mode, after the valid addresses are asserted, the corresponding data will be output on the rising or falling edge of CLK, which is determined by the read configuration register bit RCR.6. Addresses are lathed when ADV# is driven high or upon the rising or falling edge of CLK while ADV# is V_{IL}. 4-word, 8-word or continuous burst accesses is not available in this mode. Therefore, the external input addresses must be incremented every read cycle.

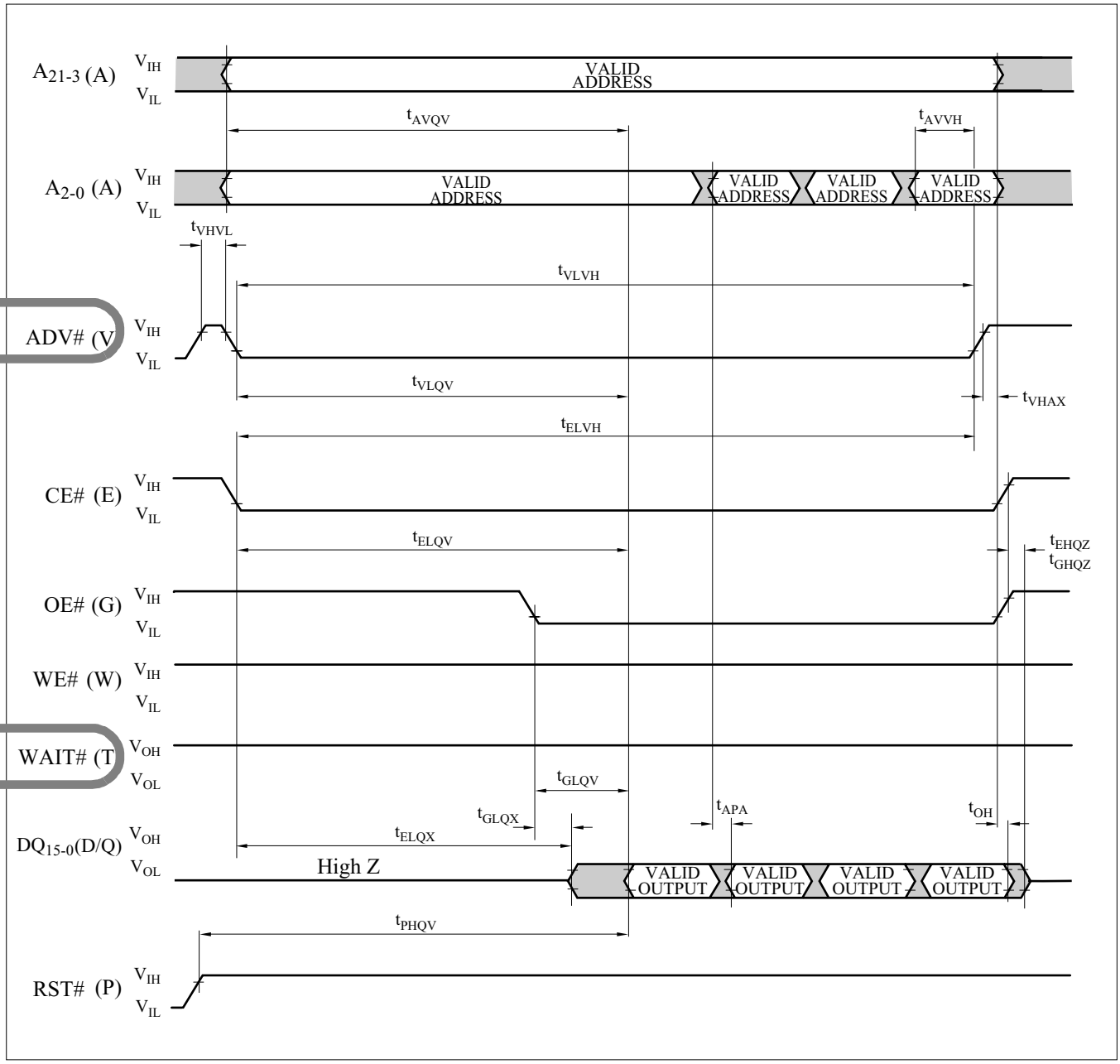

Figure 18. AC Waveform for Asynchronous Page Mode Read Operations
from Main Blocks or Parameter Blocks
(A_{21} is not used for 32M-bit device.)

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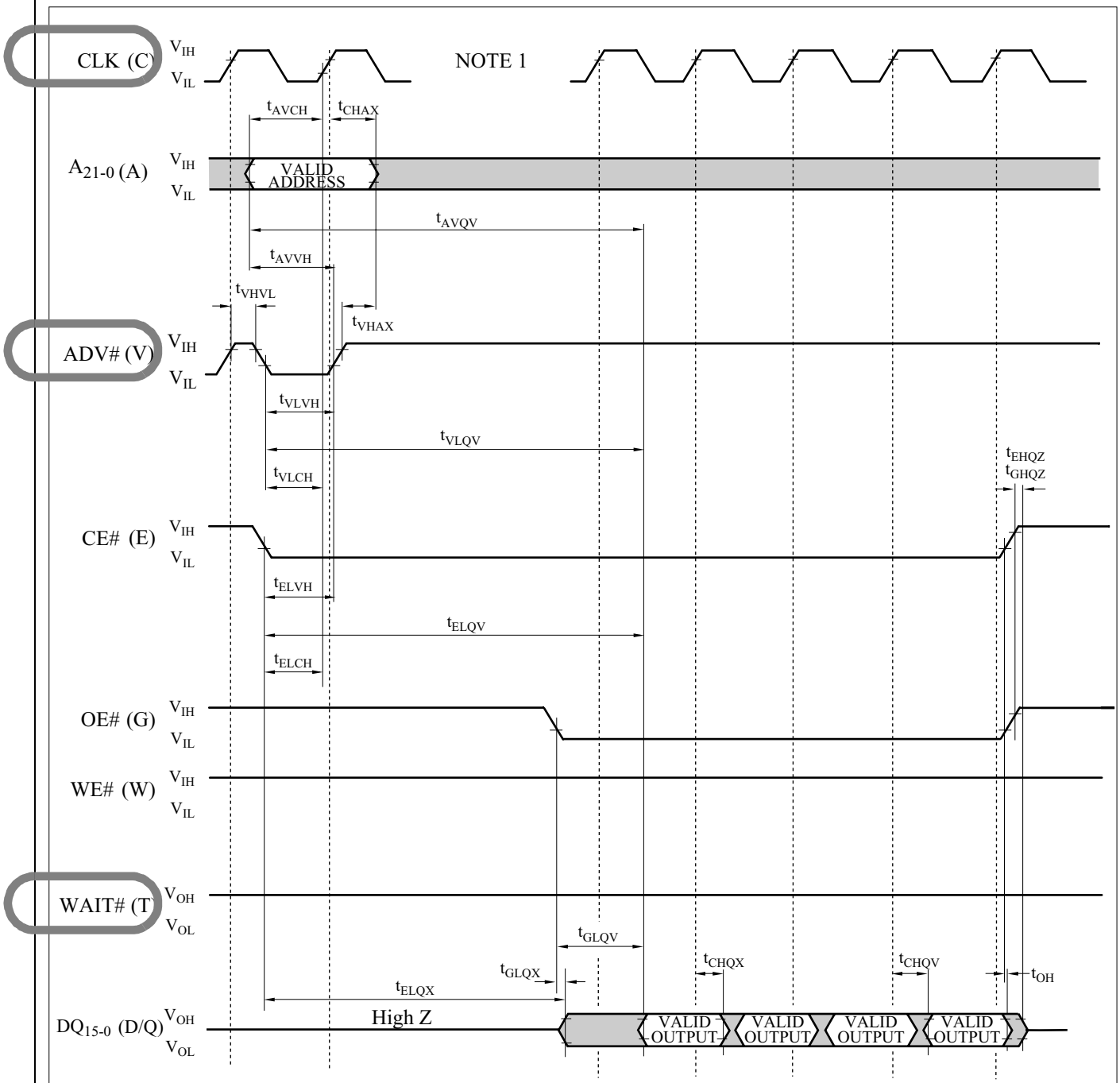
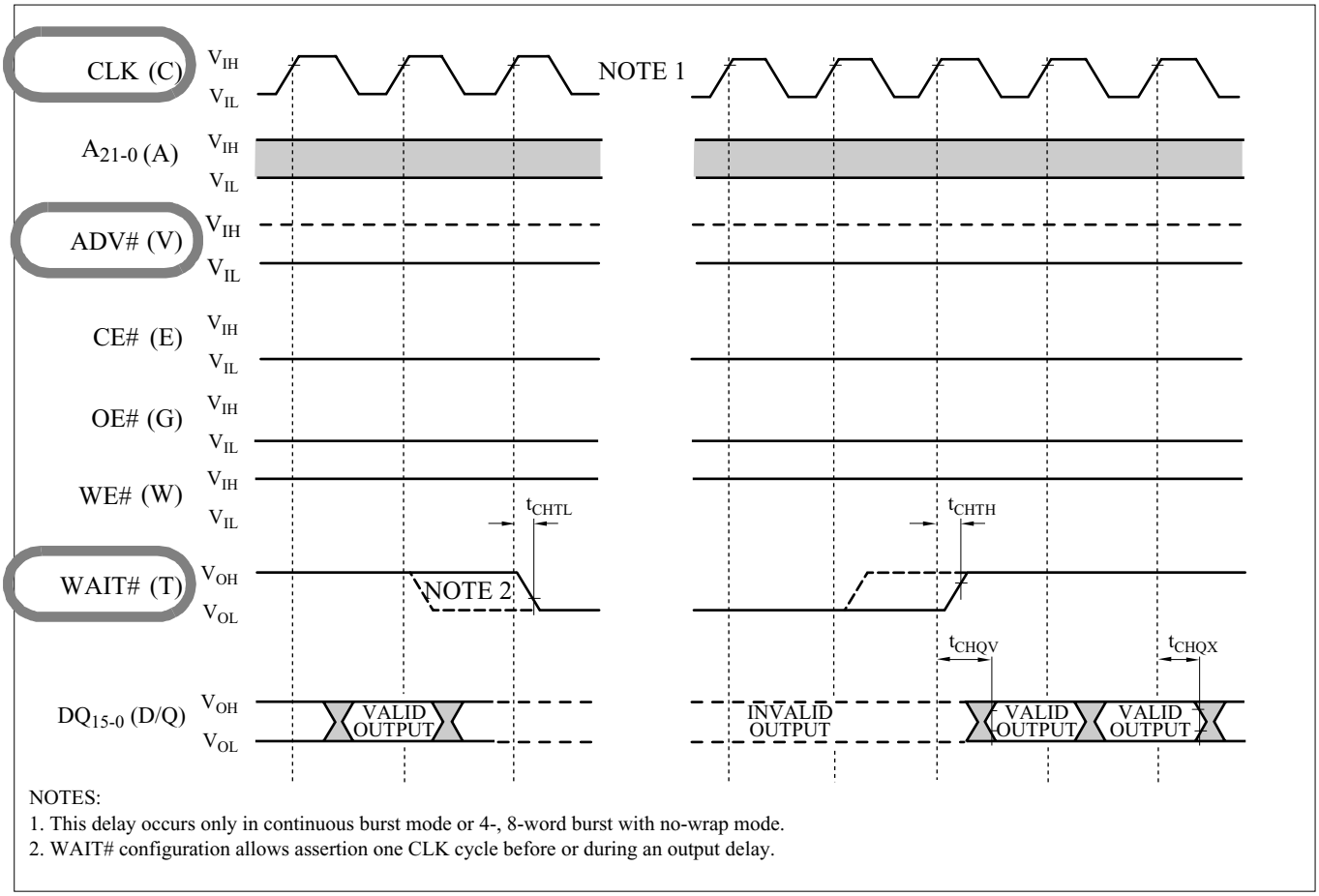
••••• Synchronous burst mode will be available for future device.



NOTE:
1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   Frequency Configuration Code 2, insert two clock cycles
   Frequency Configuration Code 3, insert three clock cycles
   Frequency Configuration Code 4, insert four clock cycles

Figure 19. AC Waveform for Synchronous Burst Mode Read Operations from Main Blocks or Parameter Blocks in 4-Word Burst Mode: RCR.2-0=001 (A_{21} is not used for 32M-bit device.)



NOTES:
1. This delay occurs only in continuous burst mode or 4-, 8-word burst with no-wrap mode.
2. WAIT# configuration allows assertion one CLK cycle before or during an output delay.

Figure 20. AC Waveform for an Output Delay when Continuous Burst Read with Data Output Configurations Set to One Clock (A_{21} is not used for 32M-bit device.)

• • • • • Synchronous burst mode will be available for future device.

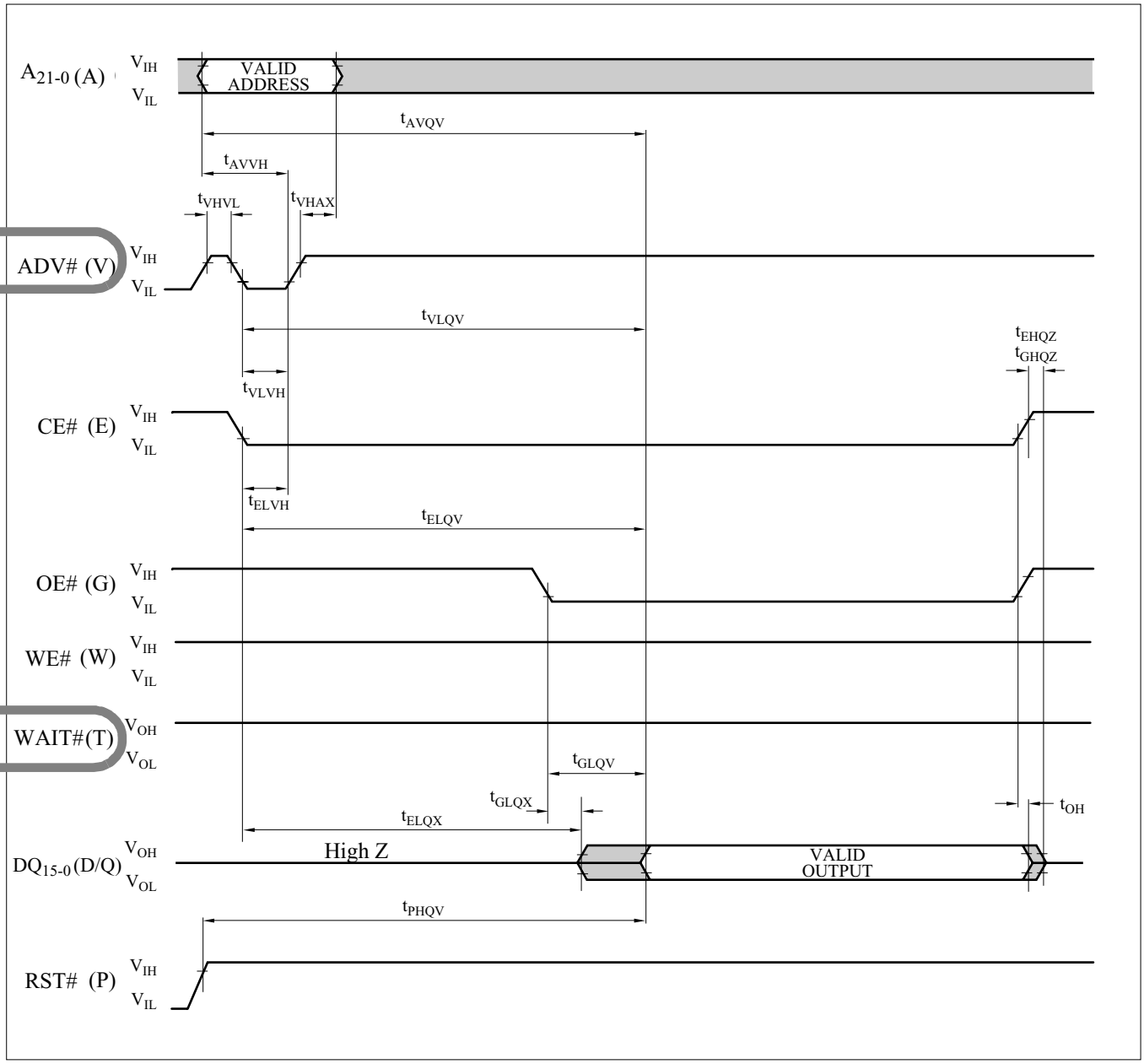
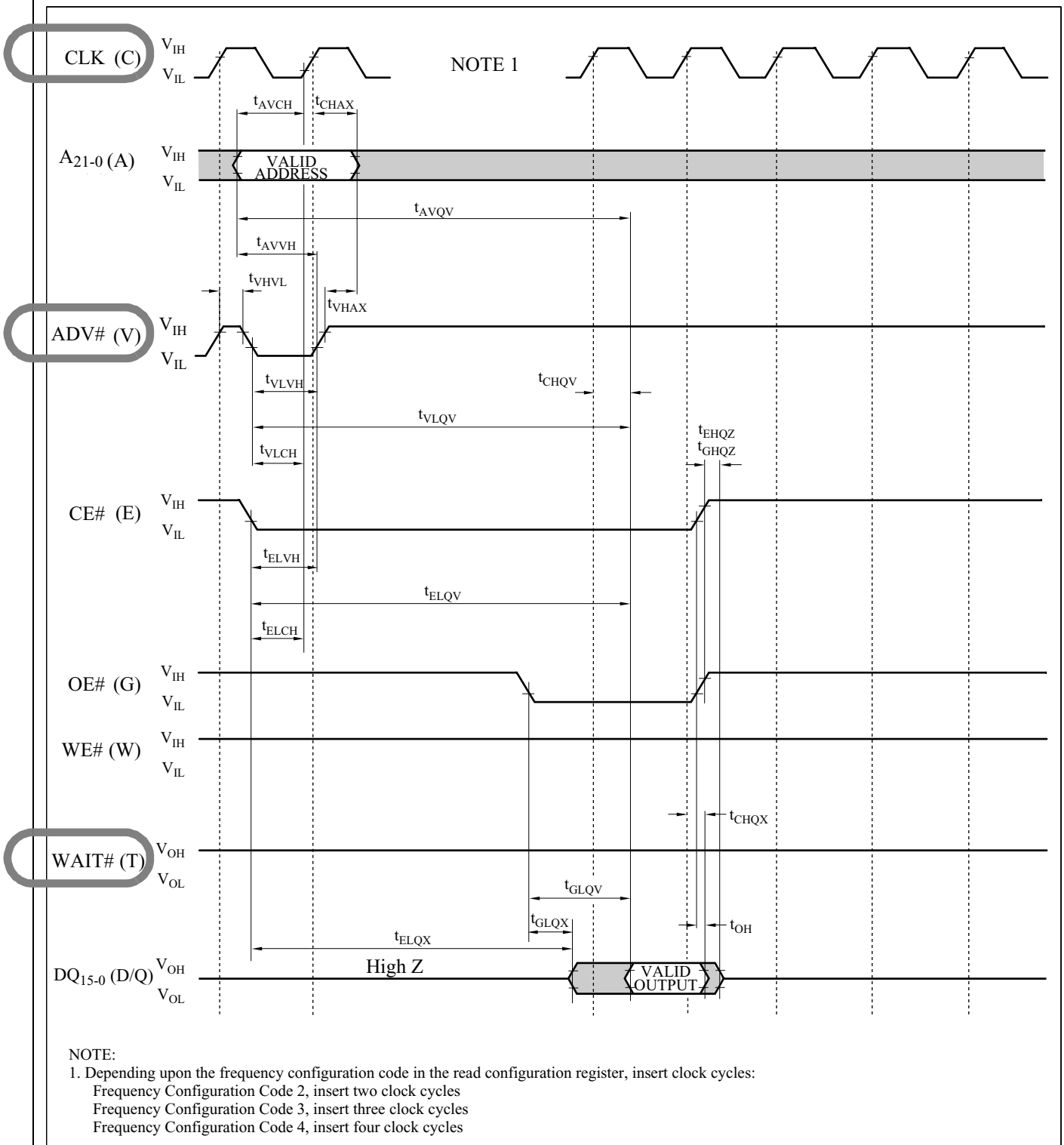


Figure 21. AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code
(A_{21} is not used for 32M-bit device.)

••••• Synchronous burst mode will be available for future device.



NOTE:
1. Depending upon the frequency configuration code in the read configuration register, insert clock cycles:
   Frequency Configuration Code 2, insert two clock cycles
   Frequency Configuration Code 3, insert three clock cycles
   Frequency Configuration Code 4, insert four clock cycles

Figure 22. AC Waveform for Single Synchronous Read Operations from Status Register, Identifier Codes, OTP Block or Query Code
(A_{21} is not used for 32M-bit device.)

••••• Synchronous burst mode will be available for future device.

6 Common Flash Interface

This section defines the data structure of the Common Flash Interface (CFI) code, which is called query code. Query code can be read by writing the Read Query command (98H) to the target partition's CUI. System software should confirm this code to gain critical information such as block size, density, bit organization and electrical specifications. Once this code has been obtained, the software will understand which command sets should be used to enable erases, programs and other operations for the flash memory device. The query code is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface or CFI.

Common Flash Interface for the LH28F320BX/ LH28F640BX series is now under development. Query code is described in the next version of Appendix.

7 Related Document Information(1)

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

