Application Information for Sharp's LS013B7DH03 Memory LCD

Sharp Microelectronics of the Americas

INTRODUCTION

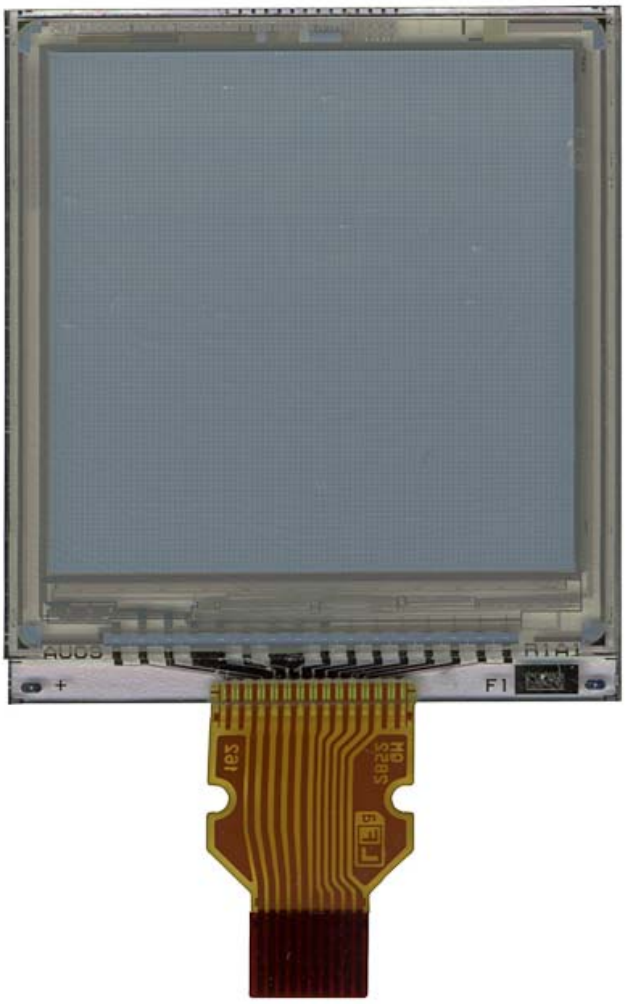
This Application Note provides additional design assistance for Sharp's LS013B7DH03 Memory LCD. This module is a transflective, monolithic active-matrix liquid crystal module utilizing Sharp's CG-silicon thin-film transistor process. Operating from a single 3 V supply, it offers high performance and power efficiency for compact display applications, with a serial interface for simple integration.

Subjects covered will be:

- Mechanical Specifications, including dimension drawings and connector specifications
- Absolute Maximum Ratings
- Optical Specifications, including view angles, reflectivity, contrast, and risetime
- Electrical Characteristics, including interfacing and signal timing information
- Design Notes
- Manufacturing Information, including handling and storage
- Reliability Information

This Note is based on Sharp's document number LCP-2111042 and is designed to provide supplementary information for the Specifications for this part.

Always refer to the latest Specifications when designing with these devices.



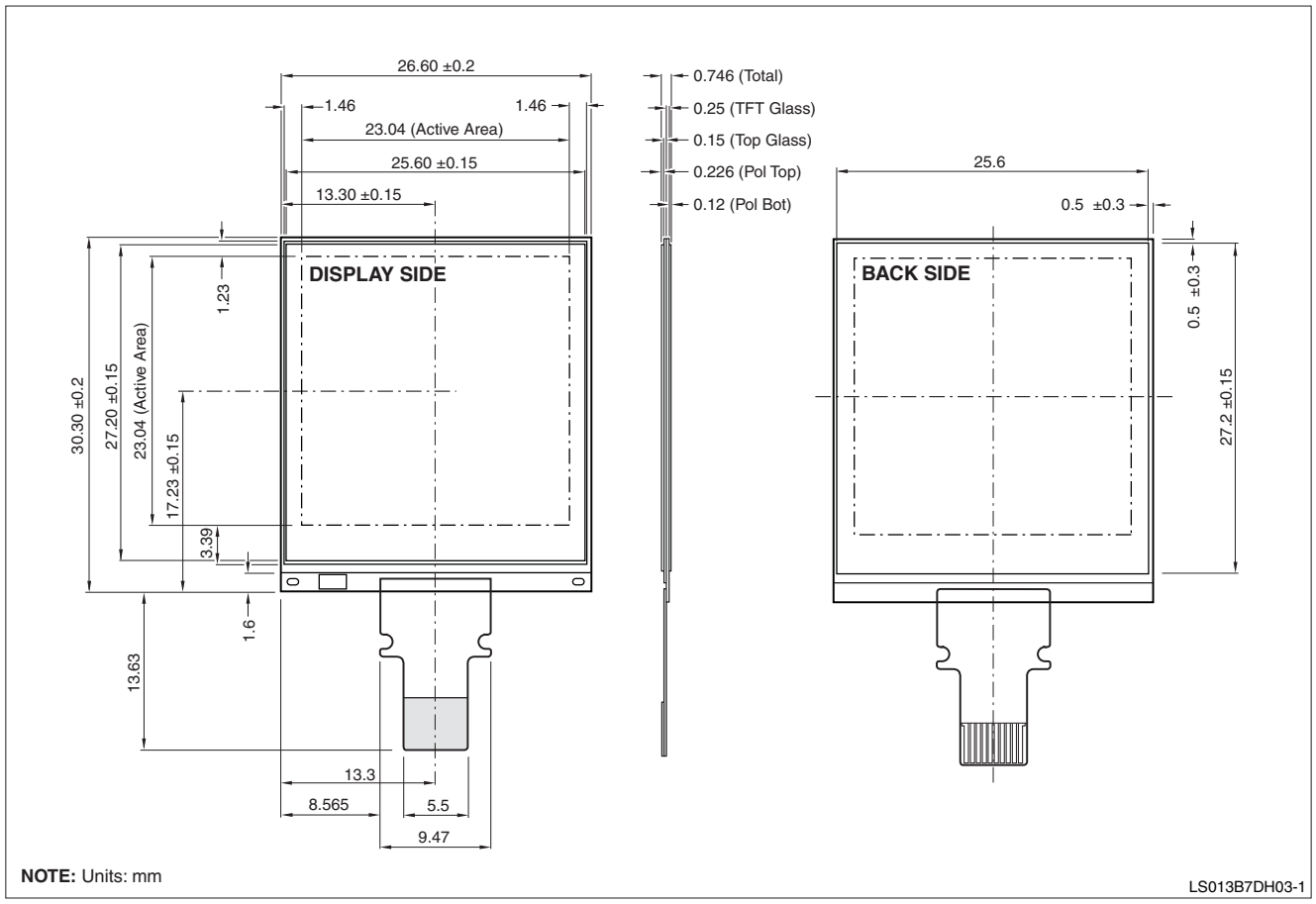
FEATURES

- Transflective monochrome panel
- Accepts a separate backlight for low-ambient situations
- Normally White
- Square aspect ratio (1:1)
- 1.28-inch screen with 128 × 128 resolution
- 3-wire serial interface
- Screen data is arbitrarily renewable by line
- Built-in, 1-bit internal memory in each pixel
- Super low power consumption TFT panel
- RoHS compliant

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATION	UNIT
Screen Size	1.28	Inch
Viewing Area	23.04 (H) × 23.04 (V)	mm
Dot Configuration (Square panel)	128 (H) × 128 (V)	Dots
Dot Pitch	0.18 (H) × 0.18 (V)	mm
Pixel Array	Square	-
External Dimensions	26.6 (W) × 30.3 (H) × 0.746 (D)	mm
Mass	3.6 (TYP.)	g
Surface Hardness	3H	Pencil hardness

External Dimensions



Connector Specifications

Table 1. Input Terminals and Functions

TERMINAL	SYMBOL	I/O	FUNCTION	NOTES
1	SCLK	INPUT	Serial clock signal	
2	SI	INPUT	Serial Data input signal	
3	SCS	INPUT	Chip select signal	
4	EXTCOMIN	INPUT	External COM inversion signal input (H: enable)	1
5	DISP	INPUT	Display ON/OFF signal	2
6	VDDA	POWER	Power supply (Analog)	
7	VDD	POWER	Power supply (Digital)	
8	EXTMODE	INPUT	COM inversion select terminal	3
9	VSS	POWER	GND (Digital)	
10	VSSA	POWER	GND (Analog)	

NOTES:
1. EXTCOMIN is HIGH enabled. When LOW, the serial input flag is enabled. See Figure 10 and Figure 11 for recommended circuits.
2. DISP enables/disables the display. All pixels will revert to Normal mode (reflective) when LOW; pixel memory is retained. When DISP = H, data in the pixel memories displays normally.
3. EXTMODE pin must be connected to VDD for HIGH, and to VSS for LOW. See FIGURE in *Interfacing and Signals*.

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Power Supply Voltage (Logic)	VDD	-0.3	+3.6	V	
Input Signal Voltage	VIN	-0.3	VDD	V	1
Storage Temperature	Tstg	-10	+60	°C	2
Operation Temperature (panel surface)	Topr	-20	+70	°C	2

NOTES:
1. Applies to SCLK, SI, SCS, DISP, EXTCOMIN.
2. Maximum wet bulb temperature is 57°C or lower, non-condensing. Condensation will cause electrical leakage and may cause the module to fail to meet this Specification.
3. For contrast, response time, and other display quality determination, use Ta = + 25°C.

OPTICAL SPECIFICATIONS

Ta = 25°C

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Viewing Angle CR ≥ 5	H	θ21, θ22	50	60		° (degrees)	1
	V	θ11	50	60		° (degrees)	1
		θ12	50	60		° (degrees)	1
Contrast Ratio		CR	21	26			2
Reflectivity Ratio		R	14	18		%	2
Transmissivity Ratio		T		0.2		%	3
Chromaticity	White	x		0.31			2
		y		0.33			2

NOTES:

1. Viewing Angle is described as clock positions: θ12 = 12 o'clock, θ11 = 6 o'clock, θ21 = 3 o'clock, θ22 = 9 o'clock. See Figure 1.
2. Contrast Ratio, Reflectivity Ratio, and Chromaticity are measured through the use of an integrating sphere. See Figure 2.
3. When this panel is backlit, luminance can be calculated by multiplying transmissivity × backlight luminance.

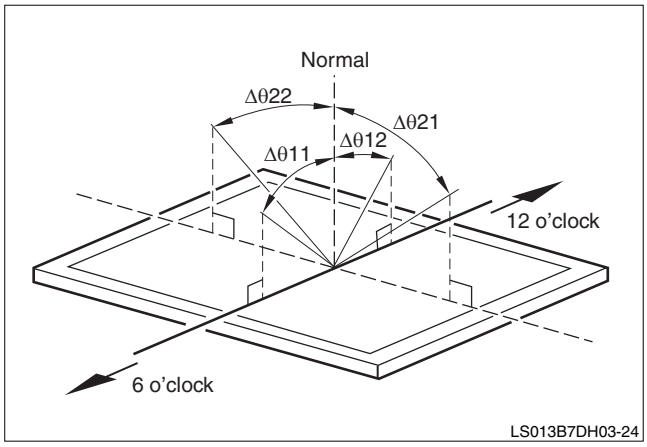


Figure 1. Viewing Angle

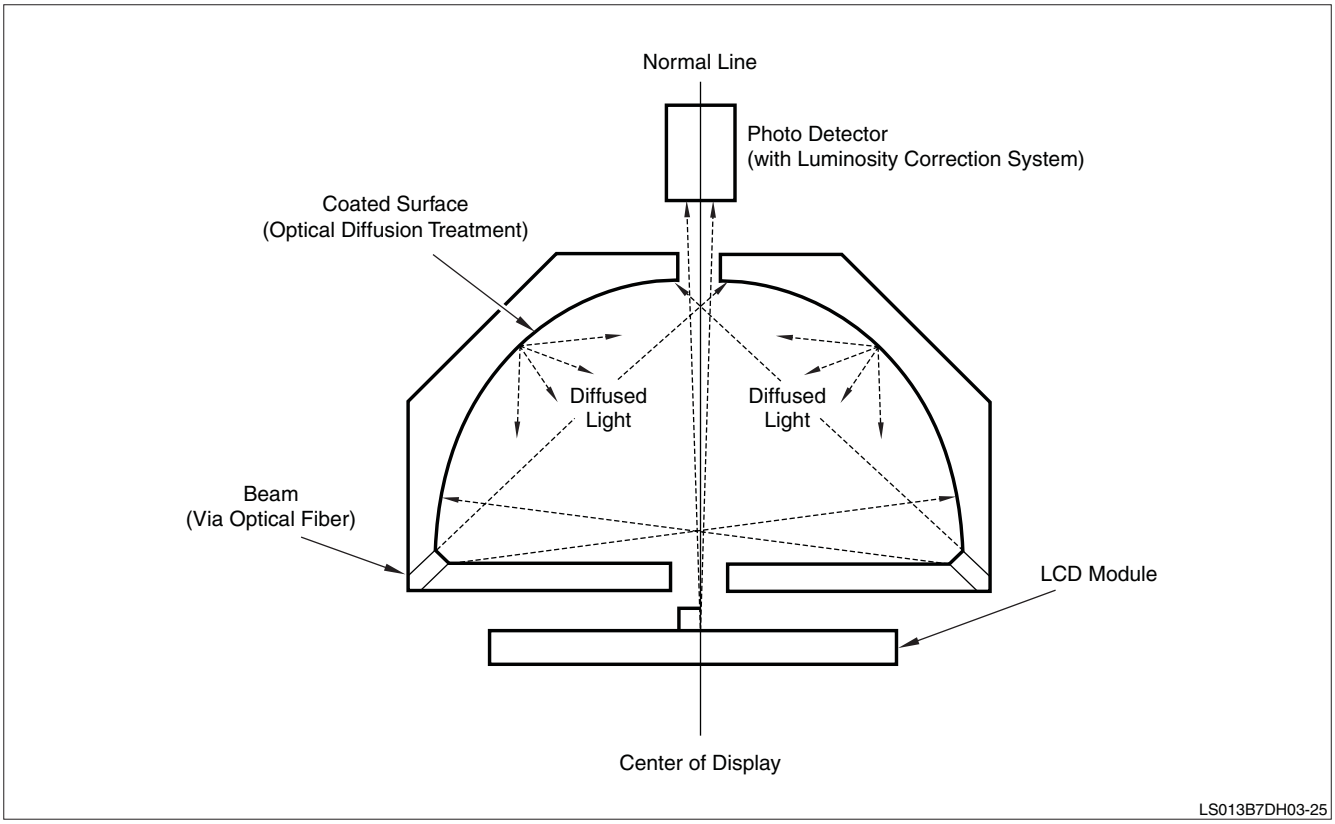


Figure 2. Setup for Contrast, Reflection Ratio, and Chromaticity

ELECTRICAL SPECIFICATIONS

Here are the Recommended Operating Conditions for this module, with VSS (GND) = 0 V and Ta = 25°C.

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Driver Supply Voltage		VDD	2.7	3.0	3.3	V	
Input Signal Voltage	HIGH	VINH	VDD-0.1		VDD	V	1
	LOW	VINL	VSS		VSS+0.1	V	
Power Consumption 1		IVDD1			20	µA	2
Power Consumption 2		IVDD2			340	µA	3

NOTES:

1. Applies to SCLK, SI, SCS, DISP, EXTCOMIN.
2. All-black display, no image updating.
   SCS = SCLK = SI = L, EXTCOMIN = 60 Hz
3. 1-dot-wide vertical stripes, continuous image updating, SCLK = 1.1MHz, EXTCOMIN= 60 Hz

Power Consumption

This module has the ability to shut down most of its logic circuits when in Static mode (not being updated). It has two levels of power consumption: Static and Dynamic Display.

Static Display: 20 µA (MAX.) All black display; fully static, no display updates.

- This includes a 1 Hz VCOM toggle, and VDD = 3 V, SCS, SCLK, SI are all held LOW. fEXTCOMIN = 60 Hz

Dynamic Display: 340 µA (MAX.) Vertical stripe display; updated at each clock transition.

- VDD = 3 V, fSCLK = 1.1 MHz, fEXTCOMIN = 60 Hz

These numbers represent peak power usage when driving VCOM. Always allow for a margin in power supply design.

Decoupling Capacitors

Use of a decoupling capacitor on VDD and VDDA is recommended, even when the two supplies are tied together. See Figure 3.

Values for these capacitors:

C1: DISP to VSS: rank B, 0.1 µF Ceramic

C2: VDDA to VSS: rank B, 0.1 µF Ceramic

C3: VDD to VSS: rank B, 1 µF Ceramic

These are recommended values; actual values should be determined by the final design. Always place the decoupling capacitors as close as possible to the part as the impedance of the VDD and VSS lines is low when the module is operating.

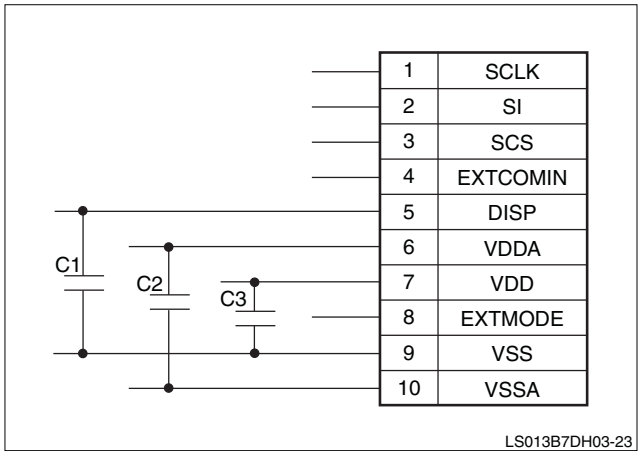


Figure 3. Decoupling Capacitors

Power Supply Sequencing

This device requires proper supply sequencing on both startup and shutdown to prevent latching of the logic circuits. Refer to Figure 4.

POWER-UP

VDD and VDDA must rise together or VDD must rise faster than VDDA.

1. 3 V rises to nominal
2. Initialize pixel memory: send M2 CLEAR ALL flag or set the display to all-white (minimum once).

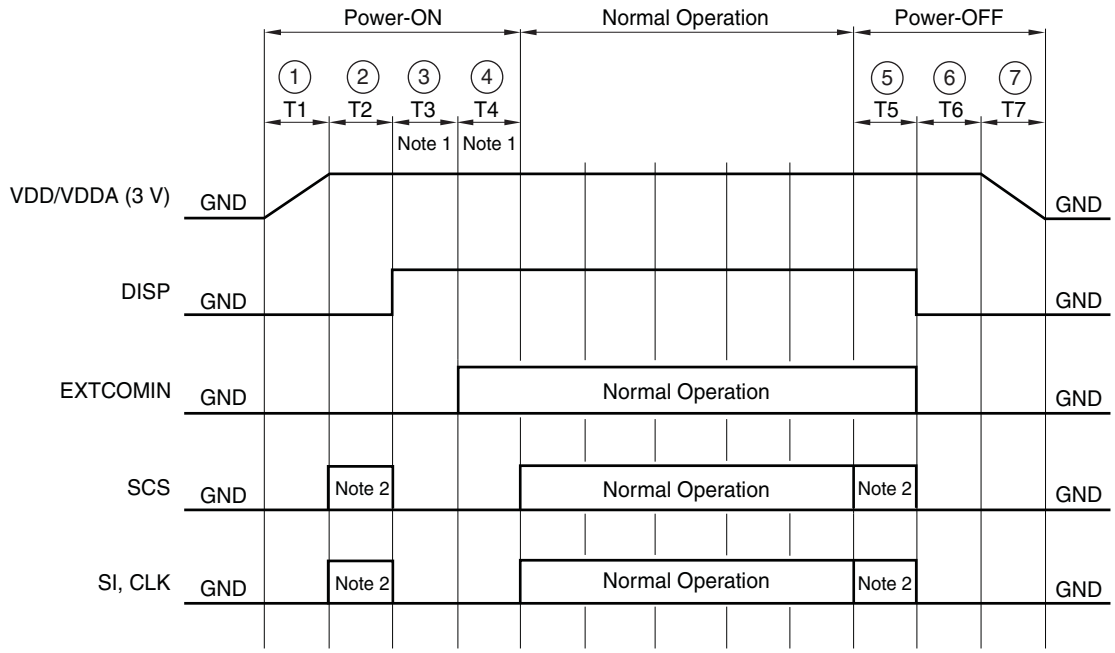
   An alternate method requires at least 16 tsSCS + SCLK cycles (See *CLEAR ALL* under *Programming*).
3. Latch cancellation for TCOM; requires a period to cancel the COM latch circuit by DISP = HIGH (requires ≥ 30 µs)
4. TCOM polarity initialization by EXTCOMIN (requires ≥ 30 µs)

POWER-DOWN

VDD and VDDA must fall together or VDDA must fall faster than VDD.

1. Initialize pixel memory: send M2 CLEAR ALL flag or set the display to all-white (minimum once).

   An alternate method requires at least 16 tsSCS + SCLK cycles (See *CLEAR ALL* under *Programming*).
2. Initialize VA, VB, and VCOM (requires ≥ 30 µs)
3. 3 V falls



NOTES:

1. The order of (3) and (4) can be reversed. VCOM polarity inversion timing controlled by EXTCOMIN doesn't work when DISP = 'L'. When DISP and EXTCOMIN go HIGH simultaneously, allow >30 µs <60 µs before SCS goes HIGH.
2. Setup value to initialize pixel memory data.

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Figure 4. Power Supply Sequencing

SIGNAL DESCRIPTIONS

Input signal characteristics are given in Table 4 and Table 5. All measurements are at VDDA = +5.0 V, VDD = +5.0 V, GND = 0 V, Ta = 25°C.

Table 4. Signal Frequencies

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT
ƒSCS	Frame frequency	1	-	60	Hz
ƒSCLK	Clock frequency		0.5	1.1	MHz
tV	Vertical Interval	16.67	-	1000	ms
ƒCOM	COM Frequency	0.5	-	30	Hz

Table 5. Signal Transition Times

PARAMETER	DESCRIPTION	MIN.	TYP.	MAX.	UNIT	NOTES
trSCS	SCS Risetime			70	ns	
tfSCS	SCS Falltime			70	ns	
twSCSH	SCS HIGH width	153.45			µs	1
		22.55			µs	2
twSCSL	SCS LOW width	2			µs	
tsSCS	SCS setup time	6			µs	
thSCS	SCS hold time	2			µs	
trSI	SI Risetime			50	ns	
tfSI	SI Falltime			50	ns	
tsSI	SI setup time	227			ns	
thSI	SI hold time	525			ns	
trSCLK	SCLK Risetime			50	ns	
tfSCLK	SCLK Falltime			50	ns	
twSCLKH	SCLK HIGH width	404.55	950		ns	
twSCLKL	SCLK LOW width	404.55	950		ns	
ƒEXTCOMIN	EXTCOMIN frequency	1		60	Hz	3
trEXTCOMIN	EXTCOMIN Risetime			70	ns	
tfEXTCOMIN	EXTCOMIN Falltime			70	ns	
thlEXTCOMIN	EXTCOMIN HIGH width	2			µs	
trDISP	DISP Risetime			70	ns	
tfDISP	DISP Falltime			70	ns	

NOTES:
1. Dynamic Mode (continuously updating display)
2. Static Mode (no display updating)
3. ƒEXTCOMIN must always be less than ƒSCS (Table 4)

Timing Diagrams

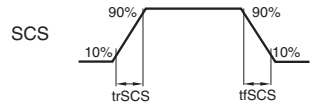
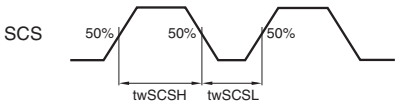
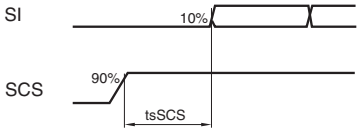
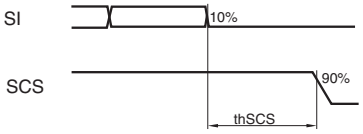
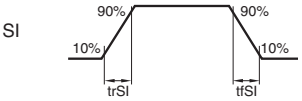
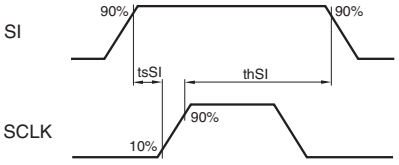
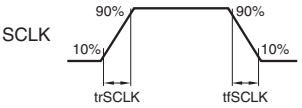
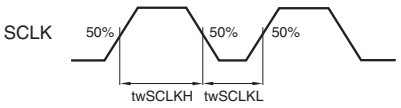
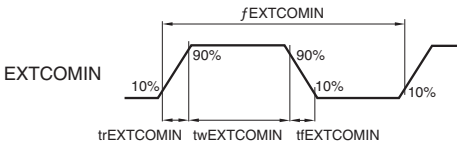
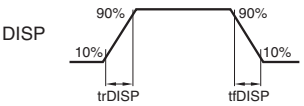
PIN NAME	ITEM	SYMBOL	WAVEFORM
SCS	SCS risetime	trSCS	
	SCS falltime	tfSCS	
	SCS HIGH width	twSCSH	
	SCS LOW width	twSCSL	
	SCS setup time	tsSCS	
	SCS hold time	thSCS	
SI	SI risetime	trSI	
	SI falltime	tfSI	
	SI setup time	tsSI	
	SI hold time	thSI	
SCLK	SCLK risetime	trSCLK	
	SCLK falltime	tfSCLK	
	SCLK HIGH width	twSCLKH	
	SCLK LOW width	twSCLKL	
EXTCOMIN	EXTCOMIN frequency	ƒEXTCOMIN	
	EXTCOMIN risetime	trEXTCOMIN	
	EXTCOMIN falltime	tfEXTCOMIN	
	EXTCOMIN HIGH width	twEXTCOMINH	
DISP	DISP risetime	trDISP	
	DISP falltime	tfDISP	

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Figure 5. SCS, SI, SCLK, EXTCOMIN, and DISP Signals

PROGRAMMING

For software commands, see the Application Note, *Programming Sharp's Memory LCDs,* by Ken Green.

In all the following diagrams and descriptions, these conventions are used:

- M0: MODE
  When M0 is 'H', the module enters Dynamic Mode, where pixel data will be updated.
  When M0 is 'L' the module remains in Static Mode, where pixel data is retained.
- M1: VCOM
  This polarity-inversion flag enables a periodic polarity inversion on the panel to keep a latent charge from building up within the Liquid Crystal cells. When M1 is 'H' then VCOM = 'H' is output. If M1 is 'L' then VCOM = 'L' is output.
  When EXTMODE = 'H', M1 value = XX (don't care). See *COM Inversion and Signal Selection.*
- M2: CLEAR ALL
  When M2 is 'L' then all flags are cleared. When a full display clearing is required, set M0 and M2 = HIGH and set all display data to white*. (Also see CLEAR ALL under Static Mode.)*
- D[1:128]: Display data
  Setting D(*n)* = 'L' sets that pixel to black. Conversely, Setting D(*n)* = 'H' sets that pixel to white.
- DUMMY DATA: Dummy data
  Dummy data is typically 'XX (don't care); however Sharp recommends setting bits to 'L'.

Data Addressing and Positions

This part uses mixed addressing for columns and lines. Columns (X direction) are addressed using an 8-bit binary scheme, and lines (Y direction) are addressed directly as 128 bits. See Table 6. One line is the minimum addressable unit in the display; even if only one pixel in the line is to be updated, the entire line must be sent.

Table 6. Column (X Direction) Addressing

LINE ADDRESS	COLUMN ADDRESS							
	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7
L1	H	L	L	L	L	L	L	L
L2	L	H	L	L	L	L	L	L
L3	H	H	L	L	L	L	L	L
:	:	:	:	:	:	:	:	:
L126	L	H	H	H	H	H	H	L
L127	H	H	H	H	H	H	H	L
L128	L	L	L	L	L	L	L	H

Dynamic Mode

For software commands, see the *Programming Sharp's Memory LCDs* application note.

MULTIPLE LINE WRITE

Dynamic Mode assumes the updating of at least one line in the display. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Dynamic Mode is entered by sending M0 = H and M2 = L.

Figure 6 shows an example of writing multiple lines.

SINGLE LINE WRITE

Writing a single line of data is much the same as writing multiple lines. During the Data Write period, data is stored in the panel's binary latch. During Data Transfer, the data from the latch is written to the panel memory, line-by-line. During the write to panel memory, data for the next line is latched.

Single Line Write requires the panel to be in Dynamic Mode.

Dynamic Mode is entered the same way, by sending M0 = H and M2 = L.

Figure 7 shows an example of writing a single line.

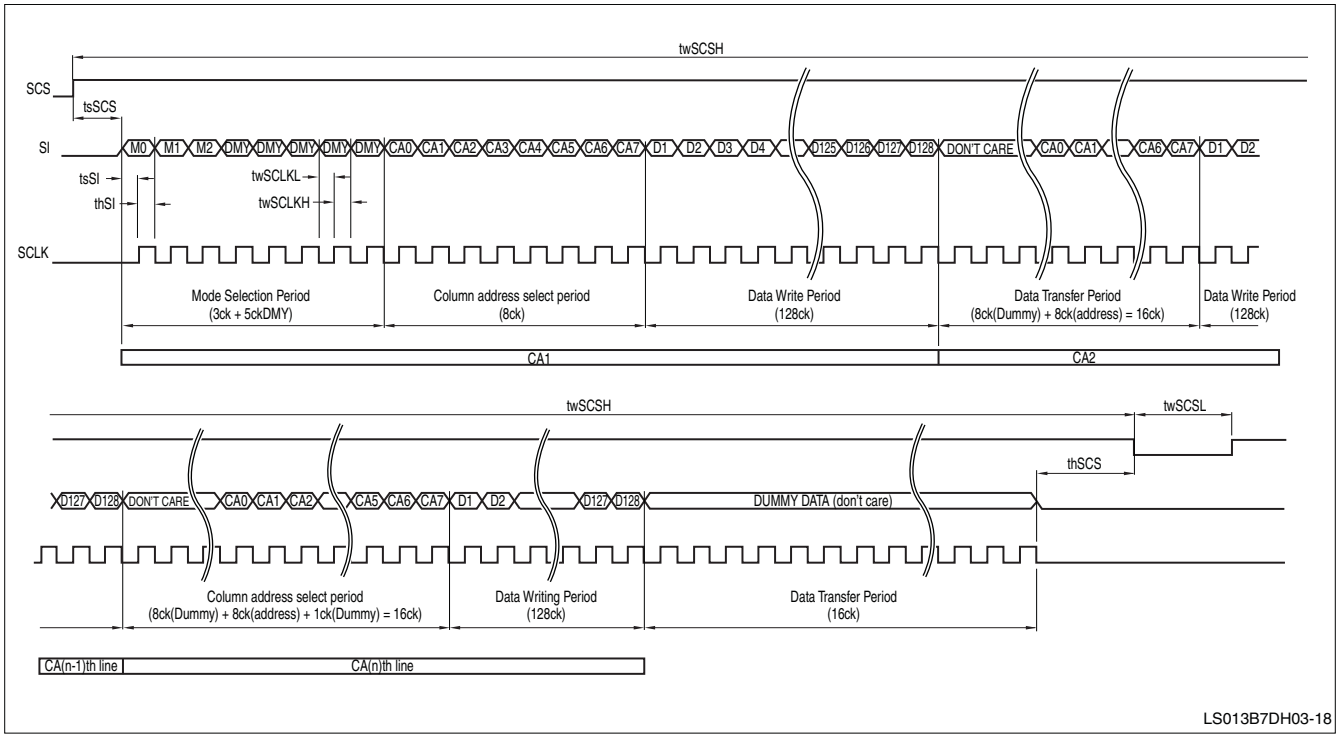


Figure 6. Dynamic Mode Timing Diagram, Writing Multiple Lines

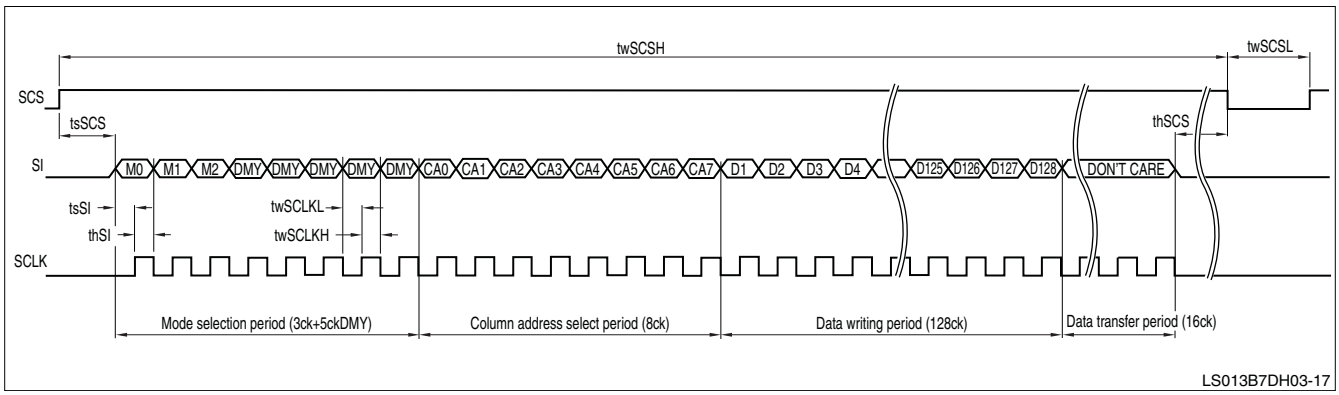


Figure 7. Dynamic Mode Timing Diagram, Writing a Single Line

Static Mode

Static Mode is the module's lowest-power mode, with data latches and other circuitry powered down. Static Mode can be held indefinitely; as long as the panel has power and VCOM is toggled periodically.

Sharp recommends keeping maximum time between VCOM toggles to no more than one second, and refreshing data every two hours, to prevent stuck pixels.

Static Mode is entered by sending M0 = L and M2 = L.

CLEAR ALL

CLEAR ALL will clear all data from pixel memories and the display will revert to its normal white color.

CLEAR ALL is invoked by sending M0 = L and M2 = H.

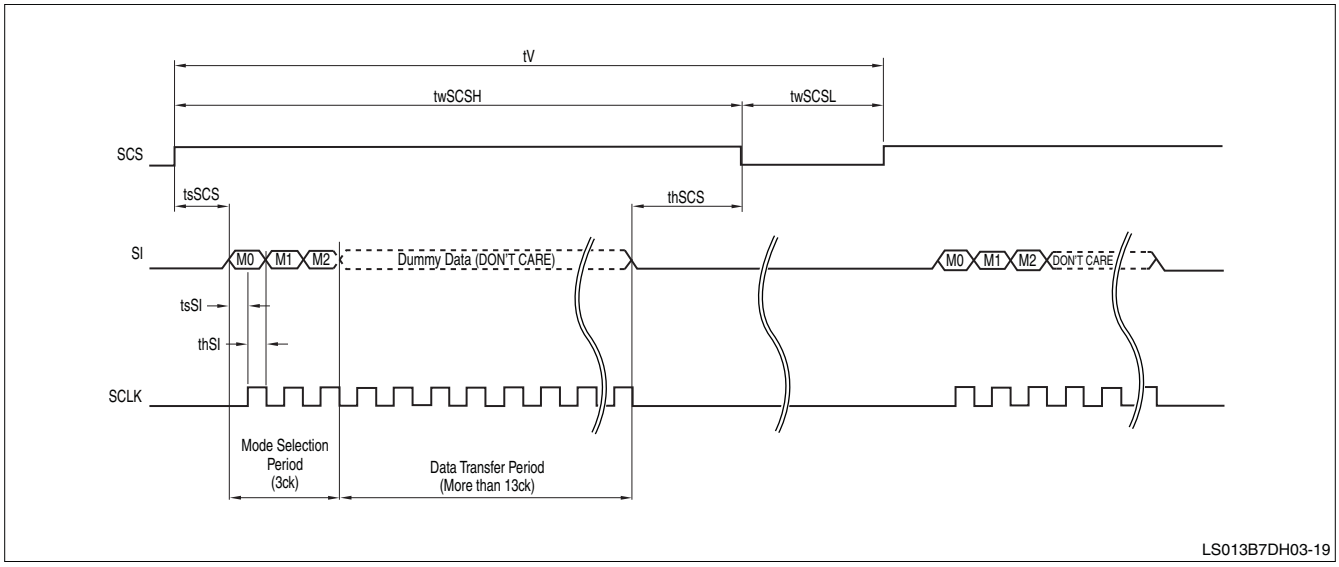


Figure 8. Static Mode Timing Diagram

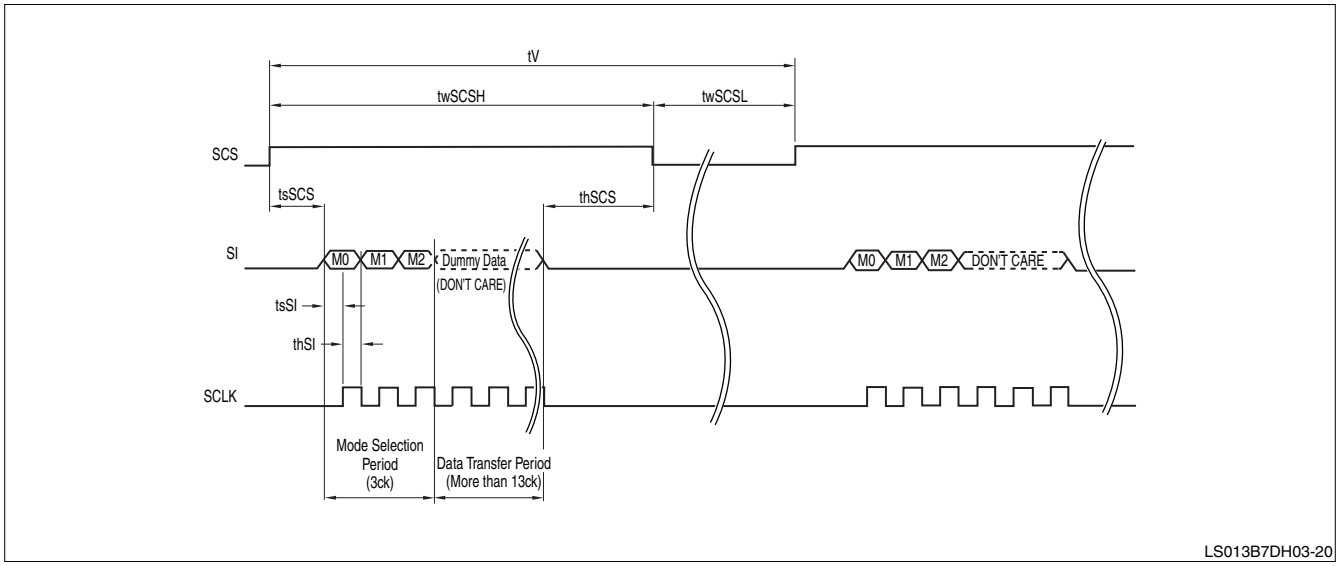


Figure 9. CLEAR ALL Timing Diagram

VCOM Inversion

Periodic VCOM (often known as just COM) inversion impresses a periodic polarity inversion across the panel to keep a latent charge from building up within the Liquid Crystal cell. It can be implemented either through software or through hardware. In either implementation, the positive and negative inversion intervals should be kept as equal as possible, and intervals should not exceed one second.

To implement VCOM inversion in software, the M1 bit is periodically toggled. When M1 is 'H' then VCOM = 'H' is output to the panel. If M1 is 'L' then VCOM = 'L' is output to the panel. To set the panel for software toggling of M1, tie EXTMODE to VSS as shown in Figure 10.

When implementing a VCOM toggle through hardware, EXTMODE is set to 'H', and the M1 value becomes XX (don't care). Hardware then toggles EXTCOMIN, and the timing between toggles of this line sets the VCOM inversion interval. Therefore, it's important not to allow the toggling interval of EXTCOMIN to exceed one second. To set the panel for software toggling of M1, tie EXTMODE to VDD as shown in Figure 11.

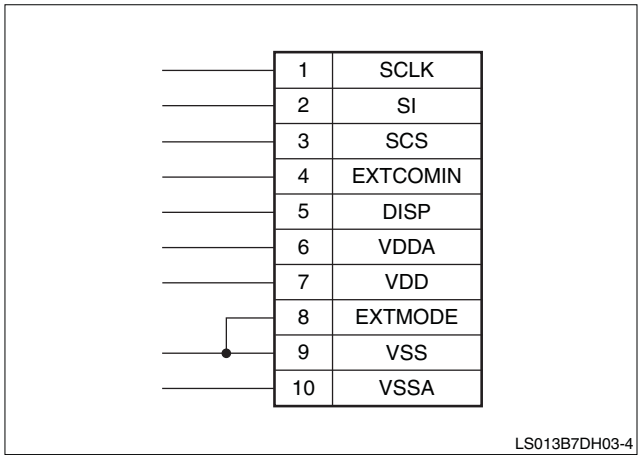


Figure 10. VCOM Software Input

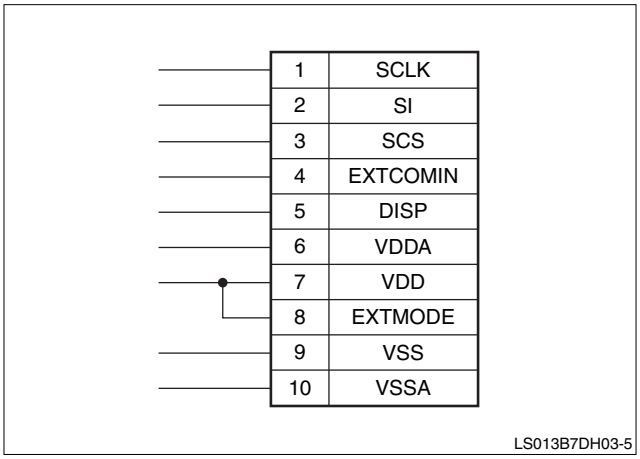


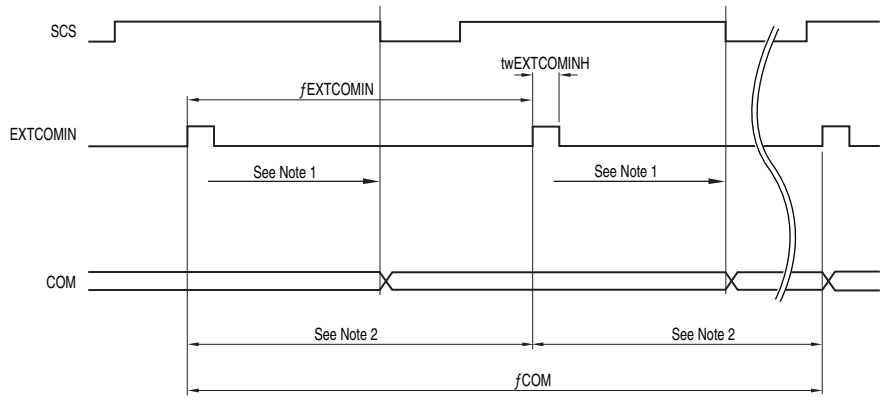
Figure 11. VCOM Hardware Input

IMPLEMENTATION

The LC cell inversion polarity toggle is armed when EXTCOMIN rises. Internal signal COMZ toggles with each rise of EXTCOMIN, and latches the VCOM transition. The VCOM transition takes place upon the next clock transition of SCS. Again, keep the duty cycle of EXTCOMIN at 50%. See Figure 12 and Figure 13.

These Truth Tables show how VCOM is implemented in both hardware and software. COMZ is an internal signal which toggles the display bias upon SCS or EXTMODE state change.

NOTE: COMZ is an internal signal, and is inverted with each rising of EXTMODE.



NOTES:
1. LC inversion polarity has been latched by a falling edge on SCS.
2. EXTCOMIN period should be constant.

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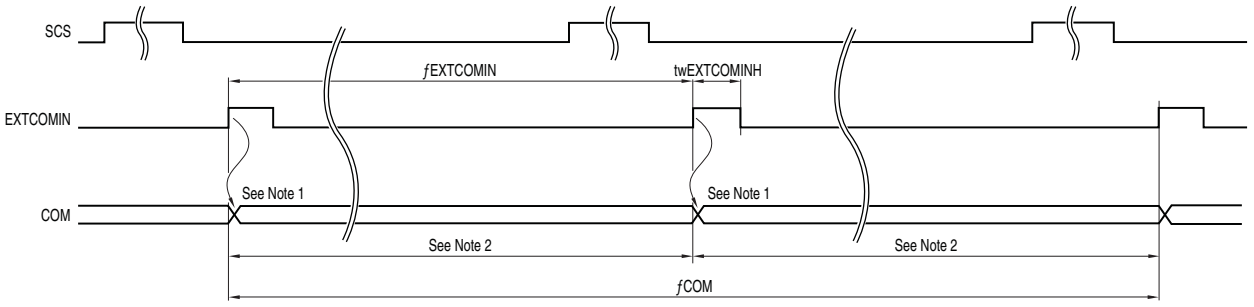
Figure 12. EXTMODE = L, Software VCOM Toggle



NOTES:
1. LC inversion polarity has been latched by the rising edge of EXTCOMIN.
2. EXTCOMIN period should be constant.

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Figure 13. EXTMODE = H, Hardware VCOM Toggle

Table 7. EXTMODE = L

EXTCOMIN	COM
L	Depends entirely on status of M1
L	
H (rising edge)	
H (rising edge)	

Table 8. EXTMODE = H, Relationship of COMZ to EXTCOMIN

EXTCOMIN	COMZ	
	Before Inversion	After Inversion
L	L	L
L	H	H
H (rising edge)	L	H
H (rising edge)	H	L

DESIGN NOTES

This device is static sensitive. Handle it only in a static-safe environment.

Light Sensitivity

1. Do not allow the finished design to expose the driver electronics on this module to light. Exposing these circuits to light can cause improper operation.
2. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

Surface Areas

1. The polarizer surface is easily damaged. Take precautions against scratching it, and do not allow the finished design to put pressure or torquing tensions on the glass exceeding that of the published Specifications.
2. Water droplets on the polarizer surface must be wiped off immediately, as they may cause color changes or other permanent damage.
3. Clean the polarizer surface by wiping it with absorbent cotton or other soft cloth. If further cleaning is necessary, use IPA (isopropyl alcohol) lightly on the surface. Do not use organic solvents as they may damage the terminal areas. If the terminal areas need cleaning, they may be cleaned with a soft cotton cloth or a cotton swab. Avoid directly touching them with fingers.
4. Keep fingerprints off the surface and the terminal areas of this module.
5. Do not press on the surface of the module, and do not stack modules in such a way that pressure will be applied to the surfaces or to the connector area. The safest place for temporary storage of modules is in their shipping tray.

Operation

1. When the final design will be used in areas of high static electricity, the image written to pixel memory may not be properly displayed. More frequent data updates are recommended to counter this.When inserting and removing the FPC (flex connector) always do so with the power OFF.
2. When inserting the module, make sure that stresses are within published Specifications, evenly distributed, and are not applying warping or torquing forces to the module. When embedding the module in a substance, make sure that no excess mechanical forces are applied to the module's surface.
3. In a design where the module face is 'bare' (no protective or anti-reflective sheet), there can be a risk of electrostatic damage to the module. Ensure that the final design has a grounded, conductive surface that mates to the polarizer's periphery. See Figure 14.
4. When displaying static images, Sharp recommends refreshing the image data every two hours to prevent stuck pixels.
5. Use of decoupling capacitors is recommended. See *Electrical Specifications.*

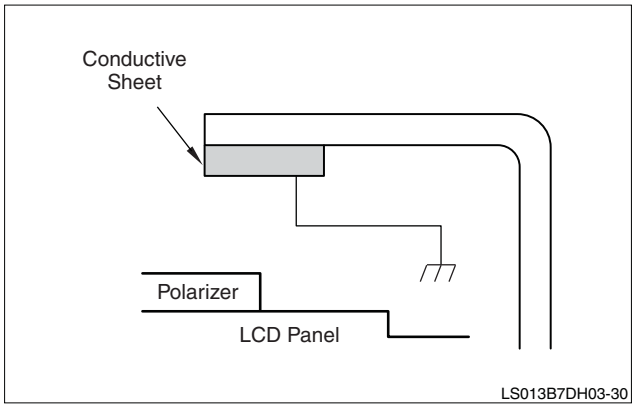

Figure 14. Bare Module Grounding

Environment

1. The liquid crystal material in this module will solidify if stored below the rated temperature, and will become an isotropic liquid if stored above the rated storage temperatures. After such storage, the material may not return to its original properties.
2. When handling this module in a production environment, do not store it in the presence of oxidation or deoxidation gases or near reagents, solvents, adhesives, resins, and materials which generate these gasses, as they may cause corrosion and discoloration of these modules.
3. Materials used in setting or epoxy resins such as amine hardening agents from packaging and silicon adhesives (dealcoholized or oximes) all release gasses which may affect the polarizer's quality. Always confirm the compatibility of these materials.
4. To avoid picture uniformity failures, do not put a seal or an adhesive material on the panel surface.
5. Do not use chloroprene rubber in the final design as it generates chlorine gas and will affect this module's reliability.

General

1. This set of Specifications gives definite environmental, electrical, and signal drive conditions for the operation of this module. Operating it outside of these given limits can reduce image quality, shorten its life, or cause it to fail altogether.
2. The connector on this module is designed for a limited number of insertions. Do not attempt to solder directly to the connector.
3. It is not a defect nor a failure to have a slight visible change in the displayed black level depending on the light source's angle of illumination and type of source.

HANDLING, STORAGE, AND PACKAGING

Handling

1. When inserting and removing the FPC (flex connector) always do so with the power OFF.
2. When inserting the module, make sure that stresses are within published Specifications, evenly distributed, and are not applying warping or torquing forces to the module. When embedding the module in a substance, make sure that no excess mechanical forces are applied to the module's surface.
3. In a design where the module face is 'bare' (no protective or anti-reflective sheet), there can be a risk of electrostatic damage to the module. Ensure that the final design has a grounded, conductive surface that mates to the polarizer's periphery.
4. This module is not made to be disassembled. Doing so may cause permanent damage.
5. The liquid crystal material in this module is injurious to humans. Do not allow it to get into the eyes or mouth. If any liquid crystal material gets on skin or clothing, immediately wash it out with soap and water.
6. This module is RoHS compliant, and does not use any ODS (1,1,1-Trichloroethane, CCL4) in its materials or in its production processes.
7. When discarding this module, dispose of it as glass waste. This LCD module contains no harmful substances. The liquid crystal panel contains no dangerous or harmful substances. The liquid crystal cell contains an extremely small amount of liquid crystal (approx.100 mg) and therefore will not leak; even if the panel should break.
8. The material used in this panel has a median lethal dose (LD50) of greater than 2,000 mg/kg and tests negative (Aims test) for mutagenic properties.

Storage

1. Store these devices at a temperature range between 0°C and 40°C, at 60% RH or less (non-condensing).
2. Use within 3 months.
3. Open the package within an area that has proper static control precautions, and more than 50% RH.
4. When storing this module, keep it from long periods of exposure to direct sunlight or other sources of ultraviolet light. Recommended storage is in a dark place.

Packaging

Figure 15 shows the serial number schema.

Figure 16 shows the location where the serial number is printed.

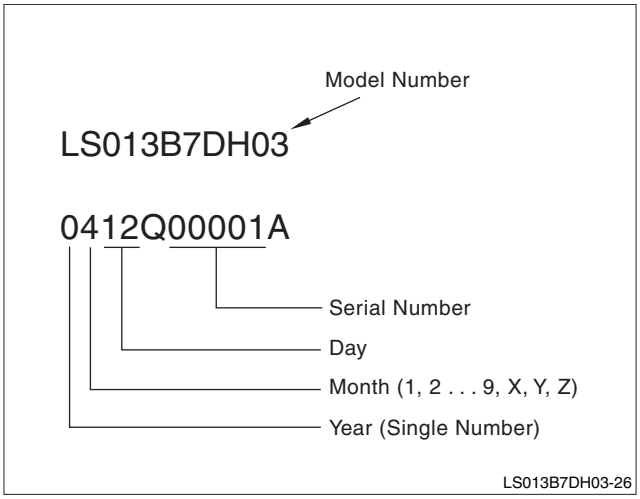

Figure 15. Serial Number

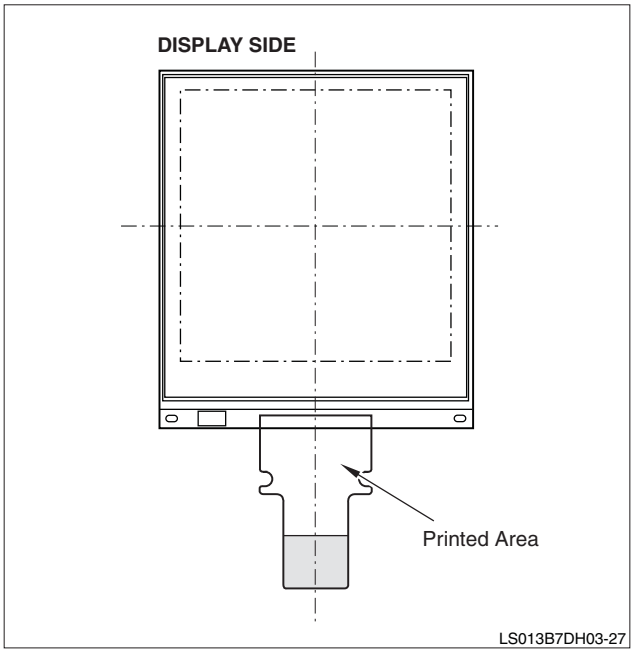

Figure 16. Serial Number Location

Packaging Diagrams

Stack no more than 12 cartons high. Product is packed in lots of 800.

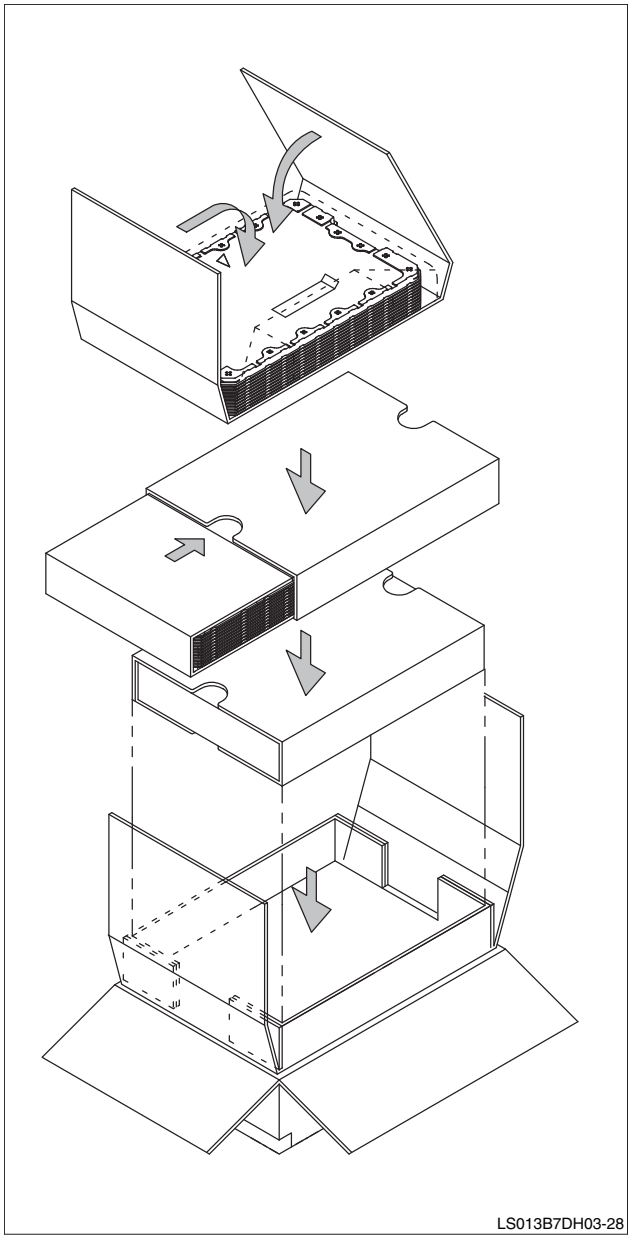

Figure 17. Packaging Format

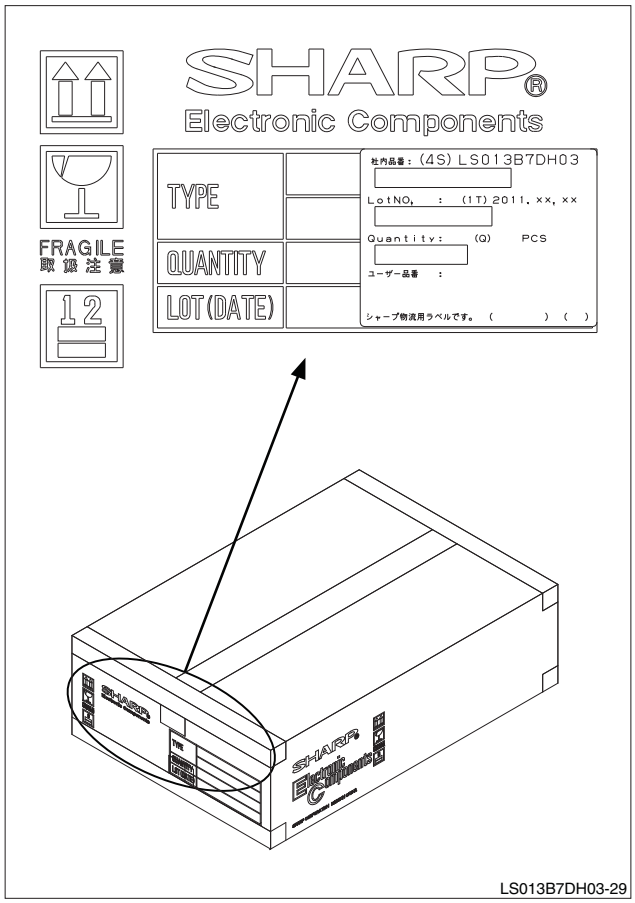

Figure 18. Package Labeling

RELIABILITY

Environmental Reliability

Table 5. Test Item Reliability

NO.	TEST ITEM	TEST CONDITION
1	High temperature storage test	Ta = 80°C, 240h
2	Low temperature storage test	Ta = -30°C, 240h
3	High temperature and high humidity operating test	Tp = 40°C/95% RH, 240h
4	High temperature operating test	Tp = 70°C, 240h
5	Low temperature operating test	Tp = -20°C, 240h
6	Shock test (non-operating)	Ta = -30°C (1h) to +80°C (1h) / 5 cycles
7	Electrostatic discharge test	±200 V, 200 pF (0 Ω) once per terminal

NOTES:
1. Ta = ambient temperature, Tp = panel temperature
2. Check for any items which impair display function.

Physical Reliability

The Panel surface stress specification parameter is the stress force [N] before image failure.

Load test: Minimum 120[N]; on an LCD panel with UV protection film, fixed to a test stage.

Pressure point is the center of the panel, with a φ10 mm column, at 1 mm/minute.

Full pressure is held for 5 seconds after achievement, then released.

SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE.

Suggested applications (if any) are for standard use; See Important Restrictions for limitations on special applications. See Limited Warranty for SHARP's product warranty. The Limited Warranty is in lieu, and exclusive of, all other warranties, express or implied. ALL EXPRESS AND IMPLIED WARRANTIES, INCLUDING THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR USE AND FITNESS FOR A PARTICULAR PURPOSE, ARE SPECIFICALLY EXCLUDED. In no event will SHARP be liable, or in any way responsible, for any incidental or consequential economic or property damage.

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