LCD Specification

LCD Group

LS028B7UX01 LCD Module

Product SpecificationJune 2007

Transflective 240 × 400 portrait-mode LCD Module featuring high integration and wide viewing angles. Full Specifications Listing.



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MOBILE LIQUID CRYSTAL DISPLAY DIVISION II SHARP CORPORATION

SPECIFICATION

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APPLICABLE GROUP Mobile LCD Group II

DEVICE SPECIFICATION FOR

CG-Silicon TFT-LCD module

MODEL No. LS028B7UX01

CUSTOMER'S APPROVAL

DATA

BY

PRESENTED

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(1) Application

This literature applies to LS028B7UX01.

(2) Overview

This module is a color transflective and active matrix LCD module incorporating CG silicon TFT (Thin Film Transistor), named mASV-TFT(mobile-ASV TFT). It is composed of a color TFT-LCD panel, a driver IC, a FPC, a back light and a back sealed casing.

Graphics and texts can be displayed on a 240×3×400 dots panel with 262,144 colors by supplying.

(3) General specifications

Table 1

Parameter	Specifications	Remarks
Screen size (Diagonal)	2.75" Diagonal	inch
Pixel format	240(H)×400(V)	
	(1 pixel = R+G+B dots)	
Pixel pitch	$0.050 \text{ (H) } \times 0.150 \text{ (V)}$	
Top Polarizer	3H Hardcoat	
Interface	8/16 bit CPU bus	
Display active area	36.00(H)×60.00(V) mm	
Unit outline dimension	$41.8(W) \times 70.5(H) \times 2.3 (D)$	[Note3-1]
Mass	10 grams	(TYP.)

[Note 3-1]

Excluding protrusion. For detailed measurements and tolerances, please refer to Fig. 1.

(4) Absolute Maximum Ratings

Table 2 $Ta=25^{\circ}C$

Parameter	Symbol	Condition	Ratings	Unit	Remark
Supply voltage for LCD	VDD	_	$-0.5 \sim +6.0$	V	VDD≧
Supply voltage for Logic	VDDIO	_	-0.5~+6.0	V	VDDIO
Input voltage (Digital)	Vin	_	-0.5~VDDIO+0.5	V	[Note4-1]
LED Power dissipation	$P_{D LED}$	_	123	mW	[Note4-2]
LED current	IL	_	30	mA	
Operating temperature (panel surface)	Тор	_	-10~60	$^{\circ}\!\mathbb{C}$	[Note4-3]
Storage temperature	Tstg	_	-30 ~ 70	$^{\circ}\! \mathbb{C}$	

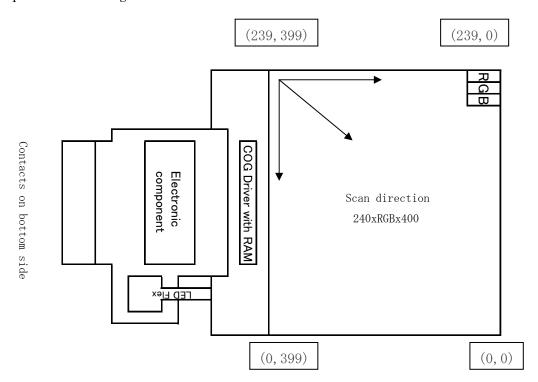
[Note4-1] Applies to RESET,RS,CS,/WR,/RD,D0 \sim D15

[Note4-2] Specification for LED per 1pcs

[Note4-3] Humidity: 95%RH Max.

(at Ta \leq 40°C). Maximum wet-bulb temperature is less than 39°C (at Ta > 40°C). Condensation of dew must be avoided.

(5)Pixel and polarization configuration



(6)Input/Output terminal

6-1)TFT-LCD panel driving section

Table3

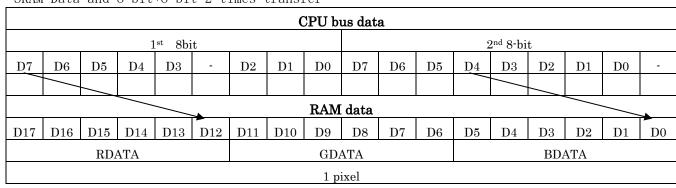
Pin No.	Symbol	I/O	Description	Remarks
1	VDDIO	-	Logic I/O power supply	-
2	VPP	-	Open or VDDIO	-
3	VDD	-	LCD power supply	-
4	BWS0	I	BWS0=L:16bit, BWS0=H:8bit	-
5	RESET	I	Reset signal input	"L" active
6	VSYNCO	О	Indicates start of frame	
7	VSS	-	GND	
8	CS	I	Chip select input	"L" active
9	RS	I	Register select input	-
10	/RD	I	Read control input	"L" active
11	/WR	I	Write control input	"L" active
12	VSS	-	GND	-
13	D0	I/O	Data bus(LSB)	-
14	D1	I/O	Data bus	•
15	D2	I/O	Data bus	•
16	D3	I/O	Data bus	-
17	D4	I/O	Data bus	-
18	D5	I/O	Data bus	-
19	D6	I/O	Data bus	-
20	D7	I/O	Data bus	•
21	VSS	-	GND	-
22	D8	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
23	D9	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
24	D10	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
25	D11	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
26	D12	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
27	D13	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
28	D14	I/O	Data bus If 8bit-I/F is used, connect to GND level.	-
29	D15	I/O	Data bus(MSB) If 8bit-I/F is used, connect to GND level.	-
30	VSS	-	GND	-
31	LED_AN	-	LED Anode	-
32	LED_CA	-	LED Cathode	-

Used connection: 0.5mm pitch FPC connector Correspondable connector: 32FLH-SM1-TB(JST)

(7)Color Input Reference & Data Transfer

Colors &	Gray)ata :	Signa	al							
Gray	scale	R	R	R	R	R	R	G	G	G	G	G	G	В	В	В	В	В	В
Scale	Level	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
	S																		
Black		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Blue		0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Green		0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Cyan		0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Red		1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Magenta		1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
Yellow		1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
White		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Î	↓				1					1	,					. ↓			
	\downarrow															. ↓			
Brighter	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
₩	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	\downarrow				\downarrow					J	,					\downarrow			
V Duianhtau	↓				↓					. ↓	,					. ↓			
Brighter	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
V	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
î	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Î	_				_						,								
V Prightor	1				_					<u>_</u>	,					_			
Brighter	GS61	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1
₩	GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
Blue	GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

SRAM Data and 8-bit+8-bit 2 times transfer



^{*}Disply RAM data D12 and D0 are complemented by CPU bus data DB7 of the first transfer and DB4 of the second transfer.

(8) Electrical characteristics

8-1)Recommended operating conditions

A) TFT-LCD panel driving section

Table 4 VSS=0V

10010 1							188 01
Parameter	Symbol	Conditions	Min.	Тур.	Max.	Unit	Applicable Pin
Supply voltage for LCD	VDD- VSS	Ta=-10∼60 °C	2.8	3.3	3.35	V	VDD
Supply voltage for Logic	VDDIO- VSS	14 10 00 0	1.6	3.3	3.35	V	VDDIO [Note8-1]
Input leakage current	${ m I_{LI}}$	Ta=-10 \sim 60 °C V_{IN} = VSS or VDDIO	-	-	10	μ A	[Na4a9 2]
"H" level input voltage	$V_{ m IH}$	Ta=-10∼60 °C	$0.8V_{\mathrm{DDIO}}$	-	-	V	[Note8-2]
"L" level input voltage	$V_{\rm IL}$	1a-10 00 C	-	-	$0.2V_{\mathrm{DDIO}}$	V	
"H" level output voltage	V_{OH}	Ta=-10∼60 °C	$0.8V_{\mathrm{DDIO}}$	-	-	V	[Note8-3]
"L" level output voltage	V_{OL}	I_{OH} =-1 00 μ A , I_{OL} = 1 00 μ A	-	_	$0.2V_{\rm DDIO}$	V	[110160-3]

【Note8-1】 V_{DD}≧V_{DDIO}

[Note8-2] Input mode of D0 \sim D15pins, RESET, RS, /RD, /WR, CS

[Note8-3] Output mode of D0~D15 pins,VSYNCO

B) Back light driving section

Table 5 Ta=25 $^{\circ}$ C

Parameter	Symbol	MIN	TYP	MAX	Units	Remarks terminal
LED voltage	VL1-VL2	_	16	17.5	V	
LED current	IL	_	20	25	mA	
Power consumption	WL	_	320	350	mW	[Note 8-4]

[Note 8-4] Measurement Conditions

4V applied to 5 LED's in series.

Calculated reference value($IL(TYP) \times (VL1-VL2)$)

8-2)Power consumption

Table 6 Ta=25 °C

14516 6							14 2 0 0
Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Remarks
Power consumption, Panel	P_{LCD}	VDD=3.3V VDDIO=3.3V	-	33	46.2	mW	[Note 8-5]
Power consumption, Standby	P_{ST}	VSS=0V	-	-	200	μ W	[Note 8-6]

[Note 8-5] Measurement Conditions

frame frequency= 60 Hz

262 k-color mode

All white pattern

No Host CPU access

[Note 8-6] Measurement Conditions

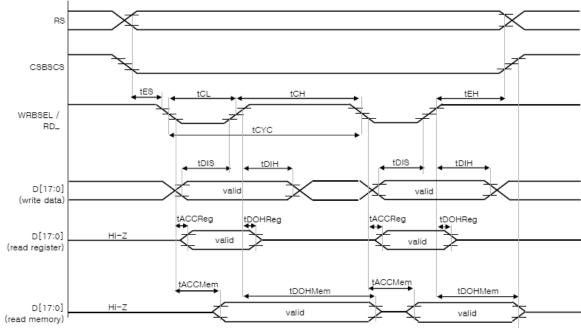
Standby mode (Oscillasion OFF/ Display OFF)

No Host CPU access

VDD & VDDIO present; RESET,/RD,/WR,CS are high, VPP=N.C.

8-3) Timing diagrams of input signals(80-family MPU access)

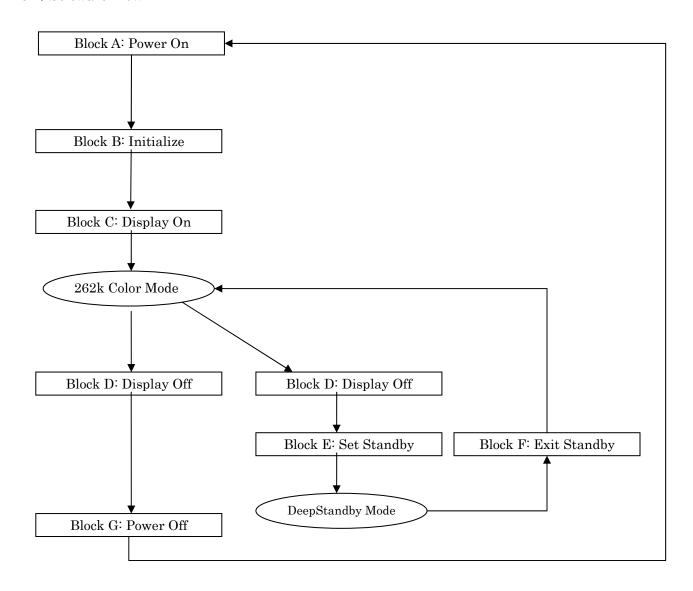
a)Write/Read timing



The read or write operation starts when both of the /CS and /WR(/RD) are low. (TA=25°C, DGND=AGND=0V, VDDC=VDDIO=Recommended Operating Conditions)

Item	記号	co	ndition	MIN	TYP	MAX	unit
enable Setup Time	tES	CS	BCS,RS	40			nS
enable Hold Time	tEH	CS	BCS,RS	40			nS
	tCYC	Write Register	80			nS	
		Write Memory		110			nS
		Read Register	VDDIO>=2.2V	125			nS
		CL=10pF	VDDIO<2.2V	160			nS
OL 1 O 1 D : 1		Read Register	VDDIO>=2.2V	180			nS
Clock Cycle Period		CL=30pF	VDDIO<2.2V	240			nS
		Read Memory	VDDIO>=2.2V	225			nS
		CL=10pF	VDDIO<2.2V	240			nS
		Read Memory	VDDIO>=2.2V	255			nS
		CL=30pF	VDDIO<2.2V	300			nS
	tCL	Write Register/M	emory	40			nS
		Read Register	VDDIO>=2.2V	85			nS
		CL=10pF	VDDIO<2.2V	120			nS
		Read Register	VDDIO>=2.2V	140			nS
Clock Low Width		CL=30pF	VDDIO<2.2V	200			nS
		Read Memory	VDDIO>=2.2V	155			nS
		CL=10pF	VDDIO<2.2V	170			nS
		Read Memory	VDDIO>=2.2V	185			nS
		CL=30pF	VDDIO<2.2V	230			nS
O1 1 771 1 777 1 1	tCH	Write/Read Regis	ter	40			nS
Clock High Width		Write/Read Memo	ory	70			nS
Write Data Setup Time	tDIS	D0-D17		40			nS
Write Data Hold Time	tDIH	D0-D17		30			nS
	tACCReg	D0-D17	VDDIO>=2.2V			75	nS
D 1		CL=10pF	VDDIO<2.2V			100	nS
Register Access Delay		D0-D17	VDDIO>=2.2V			130	nS
		CL=30pF	VDDIO<2.2V			190	nS
	tACCMem	D0-D17	VDDIO>=2.2V			135	nS
		CL=10pF	VDDIO<2.2V			150	nS
Memory Access Delay		D0-D17	VDDIO>=2.2V			165	nS
		CL=30pF	VDDIO<2.2V			210	nS
	tDOHReg	D0-D17					
Read Data(Register) Hold Time			10		50	nS	
Read Data(Memory) Hold Time	tDOHMem	D0-D17		10		50	nS
Rising/Falling Time	tr,tf	All signals				15	nS

9-1) Software Flow



9-2) Register Settings

Block A: Power On

Step	Register	Register Setting Operation						
1	RESETB=L							
2		VDDIO ON						
3	VDD ON							
4	Wait 10ms							
5	Logic initial state (CSB, WRB, RDB=H)							
6	Reset release. (RES = "L" \rightarrow "H")							
7		Wait 0.5ms						

Block B: Initialize

1 01 02 8bit 8/8 transfer 2 68 07 3 69 40 4 08 00 Normally black 5 10 F0 Panel X-size=240 6 11 90 Panel Y-size=400 7 12 01 8 1E 50 Number of vertical line=400 9 1D 07 RAM write direction:landscape 10 1A EF RAM pointer X 11 1B 8F RAM pointer Y 12 1C 01 13 30 81 Select the display-RAM data 14 33 02 Non-display data color 15 42 07 Vertical back poach=1h 16 43 01 Vertical back poach=1h 17 44 0F H sean interval=47clock 18 45 08 GSP start position=6clock 20 48 01 VCOM inversi	_		_	Block B. Initialize
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13 30 81 Select the display-RAM data 14 33 02 Non-display data color 15 42 07 Vertical front poach=7h 16 43 01 Vertical back poach=1h 17 44 0F H scan interval=47clock 18 45 08 GSP start position=4clock 19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30	11	1B	8F	RAM pointer Y
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15 42 07 Vertical front poach=7h 16 43 01 Vertical back poach=1h 17 44 0F H scan interval=47clock 18 45 08 GSP start position=4clock 19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min	13	30	81	Select the display-RAM data
16 43 01 Vertical back poach=1h 17 44 0F H scan interval=47clock 18 45 08 GSP start position=4clock 19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 3	14	33	02	Non-display data color
17 44 0F H scan interval=47clock 18 45 08 GSP start position=4clock 19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min <	15	42	07	Vertical front poach=7h
18 45 08 GSP start position=4clock 19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting <	16	43	01	Vertical back poach=1h
19 46 06 GCK start position=6clock 20 48 01 VCOM inversion position=1clock 21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	17	44	OF	H scan interval=47clock
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21 4A 01 Signal setting 22 4B A8 SSD setting 23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	19	46	06	GCK start position=6clock
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23 4C 07 ASW start position=7clock 24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	21	4A	01	Signal setting
24 5A 00 Battery pull-out detection off 25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	22	4B	A8	SSD setting
25 62 29 ASW width5, interval 1clock 26 65 02 AMP bias current setting 27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	23	4C	07	ASW start position=7clock
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27 66 05 VGM5.1V 28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	25	62	29	ASW width5, interval 1clock
28 6A 02 VCOM output 29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	26	65	02	AMP bias current setting
29 81 44 VR, VS boost clock setting 30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	27	66	05	VGM5.1V
30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	28	6A	02	VCOM output
30 82 15 DCK, DCKB timing setting 31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	29		44	•
31 83 27 DCDC dual, VS5.4V, DCDC drivability=min 32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting		82	15	
32 84 12 VR setting 33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting			27	
33 85 26 DCDC dual, VR5.3V, DCDC drivability=min 34 86 17 VS setting 35 90 25 Auto on timing setting	32	84	12	•
34 86 17 VS setting 35 90 25 Auto on timing setting				
35 90 25 Auto on timing setting				
50 51 U5 Auto On/Off Setting(17)	36	91	05	Auto ON/OFF setting(1V)
37 92 15 Auto OFF timing setting				
38 31 01 VAL	38			

Block C: Display On

Step	Register	Setting	Operation				
1	03		RAM write				
2	3E	01 Auto ON sequence					
3		Wait 120ms					

Block D: Display Off

	1 V						
Step	Register	Setting	Operation				
1	30	80	All black display				
2	Wait 50ms						
3	C0 00						
4	3E 02 Auto OFF sequence						
5	Wait 100ms						

Block E: Set Standby

Step	Register	Setting	Operation			
1	07	00	Sscillator OFF			
2	80	01	Deep standby			

Block F: Exit Standby

_								
Step	Register	Setting	Operation					
1	80	81	Deep standby out					
2	Wait 0.1ms							
3	07 01 Oscillator on							
4	Wait 1ms							
5	C0	02						
6	Wait 1ms							
7	3E 01 Auto ON sequence							
8	Wait 120ms							
9	30	81	Display ON					

Block G: Power Off

Step	Register Setting Operation					
1	RESETB=L					
2	VDD OFF (Analog voltage Off)					
3			VDDIO OFF (IO voltage OFF)			

(10)Optical characteristics

10-1)Not driving the Back light condition

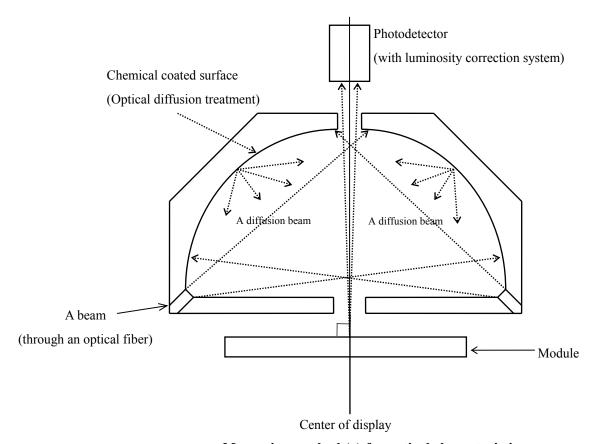
Table 7	VDD=3.3V	VDDIO=1.8V

Ta=25°C

Parameter		Symbol	Condition	Min	Тур	Max	Unit	Remarks
Viewing angle		θ21,22		40	50	-	degree	[Note 10-1,2]
range		θ11	CR≥2	40	50	-	degree	
				40	50	-	degree	
Contrast ratio		CR	$\theta = 0$ °	9	13	-	-	[Note 10-2,3]
Response	Rise	τr	0.00	-	20	30	ms	[Note 10-4]
time	Fall	τd	$\theta = 0_{\circ}$	-	10	15	ms	
White chromaticity		X	θ =0∘	-	0.31	-	-	
		у		-	0.34	-	-	
Reflection ratio		R	θ=0°	1.6	2.5	-	%	[Note 10-5]

^{*} The measuring method of the optical characteristics is shown by the following figure.

^{*} A measurement device is Otsuka luminance meter LCD5200.(With the diffusion reflection unit.)



Measuring method (a) for optical characteristics

10-2)Driving the Back light condition

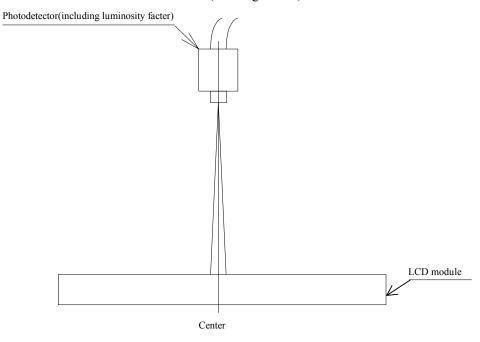
Table 8 VDD=3.0V, VDDIO=1.8V

Ta=25°C

Parameter		Symbol	Condition	Min	Тур	Max	Unit	Remarks
Viewing angle		θ11	CR≥5	55	80	-	degree	[Note 10-1,2]
range		θ12		55	80	-	degree	
		θ21		55	80	-	degree	
		θ22		55	80		degree	
Contrast ratio		CR	$\theta = 0_{\circ}$	280	400	-	-	[Note 10-2]
Response	Rise	τr	$\theta = 0_{\circ}$	-	25	35	ms	[Note 10-4]
time	Fall	τd		-	15	20	ms	
White chromaticity		X	$\theta = 0_{\circ}$	0.25	0.30	0.35	-	
		у		0.27	0.32	0.37	-	
Brightness		Y	$\theta = 0_{\circ}$	210	300	-	cd/m ²	IL=20mA
NTSC ratio				-	70	-	%	

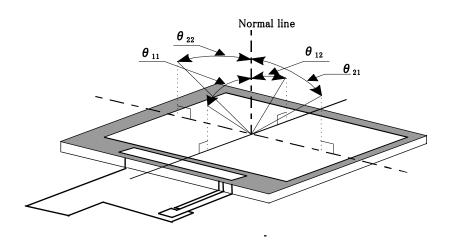
^{*} The measuring method of the optical characteristics is shown by the following figure.

^{*} A measurement device is TOPCON luminance meter SR-3.(Viewing cone 1)



Measuring method (c) for optical characteristics

[Note 10-1] Viewing angle range is defined as follows.



Definition for viewing angle

[Note10-2] Definition of contrast ratio:

The contrast ratio is defined as follows:

Photodetecter output with all pixels white(GS63)

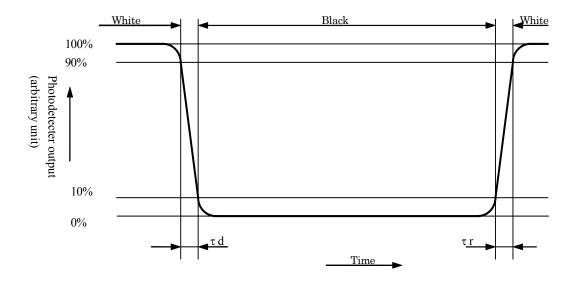
Contrast ratio(CR)=

Photodetecter output with all pixels black(GS0)

[Note10-3] A measurement device is Minolta CM-2002.

[Note10-4] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".



[Note10-5] Definition of reflection ratio Reflection ratio =

Light detected level of the reflection by the LCD module

Light detected level of the reflection by the standard white board

(11)Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standards for TFT-LCD.

(12)Mechanical characteristics

12-1) External appearance

See Fig. 1

12-2) FPC (for LCD panel) characteristics

(1)Specific connector

32FLH-SM1-TB(JST)

(13) Handling Precautions

13-1) Insertion and taking out of FPCs

Be sure insert and take out of the FPC into the connector of the set after turning off the power supply on the set side.

13-2) Handling of FPCs

The FPC for LCD panel shall be bent only slit portion. The bending slit shall be bent uniformly on the whole slit portion with bending radius larger than 0.6mm, and only inner side (back side of the module). Don't bend it outer side (display surface side).

Don't give the FPCs too large force, for example, hanging the module with holding FPC.

13-3) Installation of the module

On mounting the module, be sure to fix the module on the same plane. Taking care not to warp or twist the module.

13-4) Precaution when mounting

(1) If water droplets and oil attaches to it for a long time, discoloration and staining occurs.

Wipe them off immediately.

- (2) Glass is used for the TFT-LCD panel. If it is dropped or bumped against a hard object, it may be broken. Handle it with sufficient care.
- (3)As the CMOS IC is used in this module, pay attention to static electricity when handling it. Take a measure for grounding on the human body.

13-5) Others

- (1) The liquid-crystal is deteriorated by ultraviolet rays. Do not leave it in direct sunlight and strong ultraviolet rays for many hours.
- (2) If it is kept at a temperature below the rated storage temperature, it becomes coagulated and the panel may be broken. Also, if it is kept at a temperature above the rated storage temperature, it becomes isotropic liquid and does not return to its original state. Therefore, it is desirable to keep it at room temperature as much as possible.
- (3) If the LCD breaks, don't put internal liquid crystal into the mouth. When the liquid crystal sticks to the hands, feet and clothes, wash it out immediately.
- (4) Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.
- (5) Observe general precautions for all electronic components.

(14) Reliability Test Conditions for TFT-LCD Module

Table 9

No.	Test items	Test conditions	
1	Low temperature storage test	Ta=-30℃	240h
2	High temperature storage test	Ta=+70°C	240h
3	Thermal Shock storage test	Ta=-30°C:1h~70°C:1h	50cycles
4	Low temperature operating test	Ta=-10℃	240h
5	High temperature operating test	Ta=+60°C	240h
6	High temperature and high humidity operating test	Ta=+40°C , 95%RH (But no condensation of dew)	240h
7	Electro static discharge test	$\pm 2 \mathrm{kV} \cdot 100 \mathrm{pF} (1.5 \mathrm{k}\Omega)$ 1 time for each	ach terminals
8	Shock test	980 m/s ² , 6 ms $\pm X, \pm Y, \pm Z$ 3 times for each direct (JIS C0041, A-7 Condition	
9	Vibration test	Frequency range: 10Hz~55Hz Stroke: 1.5 mm Sweep: 10Hz~55I X,Y,Z 2 hours for each direction (to	Hz tal 6 hours)

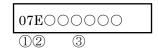
[Note] Ta = Ambient temperature

[Check items] Test No.1 \sim 9 : In the standard condition, there shall be no practical problems that may affect the display function.

(15) Others

15-1) Indication of lot number

The lot number is printed in the position shown in Fig. 1. (Outline Dimensions).



①product year 2007:7, 2008:8

②product month Jan:A, Feb:B, Mar:C, ·····Oct:J, Nov:K, Dec:L

3serial number

15-2) Used Regulation of Chemical Substances Breaking Ozone Stratum

Substances with the object of regulating: CFCS, Carbon tetrachloride, Halon

1,1,1-Trichloro ethane (Methyl chloroform)

- (a) This LCD module, Constructed part and Parts don't contain the above substances.
- (b) This LCD module, Constructed part and Parts don't contain the above substances in processes of manufacture.
- 15-3) If some problems arise about mentioned items in this document and other items, the user of the TFT-LCD module and Sharp will cooperate and make efforts to solve the problems with mutual respect and good will.

(16) Forwarding form

a) Piling number of cartons: 8 deep

b) Package quantity in one cartons: 400(pcs)

c) Carton size: (w) 382×(D) 578×(H) 255 (mm)

d) Total mass of 1 carton filled with full modules: approximately 9.5 (Kg)

Conditions for storage

Environment

(1)Temperature $0 \sim 40^{\circ}$

(2) Humidity : 60%RH or less (at 40°C)

No dew condensation at low temperature and high humidity.

(3)Atmosphere : Harmful gas, such as acid or alkali which bites electronic

components and/or wires, must not be detected.

(4)Period : about 3 months

(5)Opening of the package: In order to prevent the LCD module from breakdown by

electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as

earth, etc.

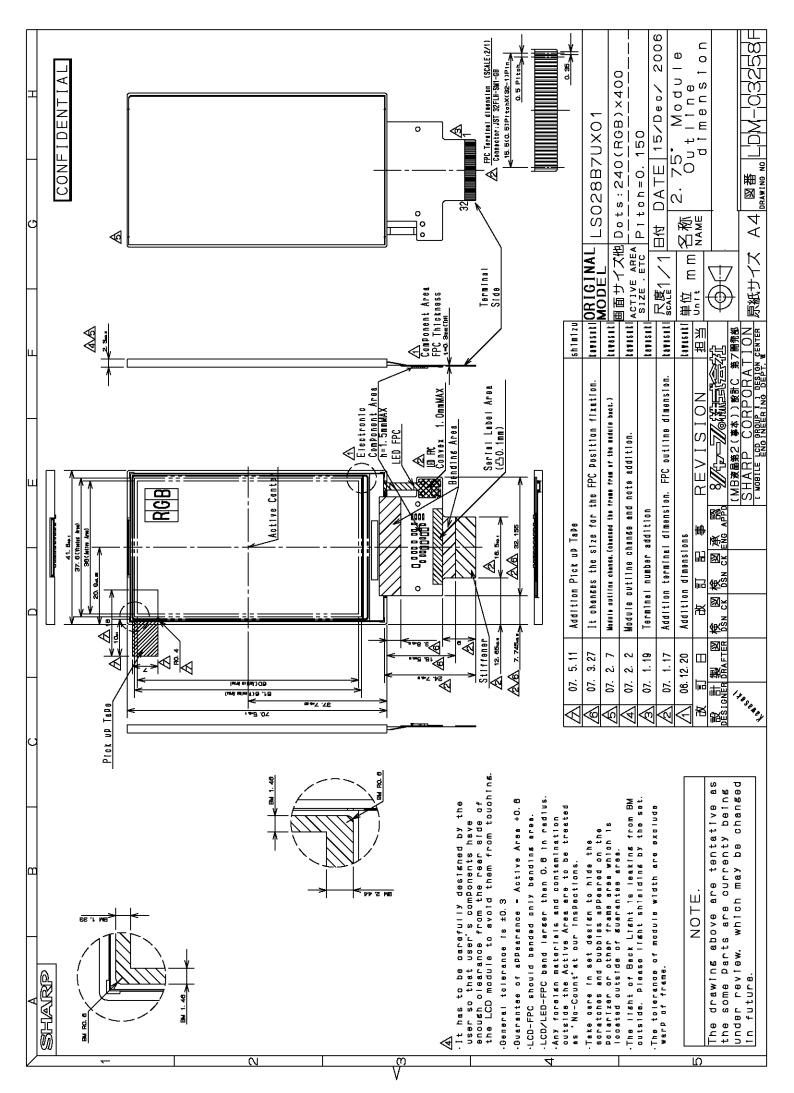


Fig. 1 Outline Dimensions

LCD Specification

LCD Group

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