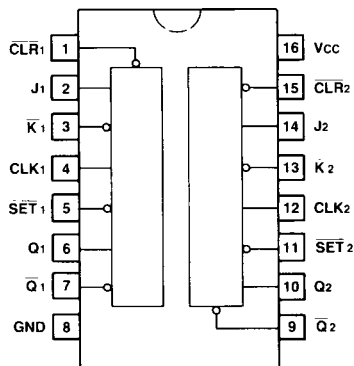


Dual J-K Positive-Edge-Triggered Flip-Flop

The LS109 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package.



Truth Table

Inputs					Outputs	
Set	Clear	Clock	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q}_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q	\bar{Q}

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level

H = High level (steady state)

L = Low level (steady state)

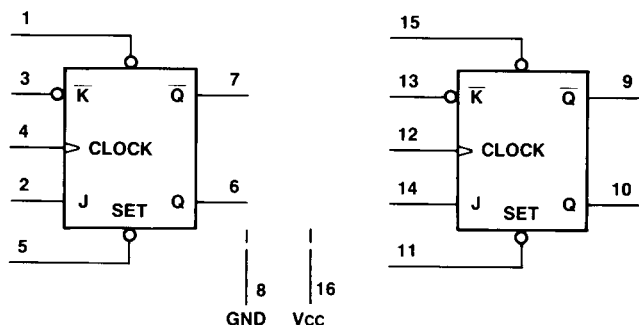
↑ = Transition from low to high level

X = Irrelevant (any input, including transitions)

Q₀ = Level of Q before the indicated steady-state input conditions were established

\bar{Q}_0 = Complement of Q₀ or level of \bar{Q} before the indicated steady-state input conditions were established

TOGGLE = Each output changes to the complement of its previous level on each active transition indicated by ↑



VCC = 5.0 ±0.5 V, TA = -55 to +125°C (WA-LS)
VCC = 5.0 ±0.25 V, TA = 0 to 70°C (WP90224L13)
VCC = 5.0 ±0.5 V, TA = -40 to +85°C (WA-LSD, WP91398L4)

		WA-LS		WP, WA-LSD		
Parameter	Symbol	Min	Max	Min	Max	Units
Output Voltage, $V_{CC} = 4.5\text{ V}$						
Low, $I_{OL} = 4.0\text{ mA}$	V_{OL}	—	0.4	—	0.4	V
$I_{OL} = 8.0\text{ mA}$	V_{OL}	—	0.5	—	0.5	V
High, $I_{OH} = -0.4\text{ mA}$	V_{OH}	2.5	—	2.7	—	V
Input Voltage, $V_{CC} = 4.5\text{ V}$						
Low	V_{IL}	—	0.7	—	0.8*	V
High	V_{IH}	2.0	7.5	2.0	5.5	V
Clamp, $I_{IN} = -18.0\text{ mA}$	V_{IK}	—	-1.5	—	-1.5	V
Input Current, $V_{CC} = 5.5\text{ V}$						
Low, $V_{IL} = 0.4\text{ V}$						
J, K	I_{IL}	—	-0.4	—	-0.4	mA
Clock, Set	I_{IL}	—	-0.8	—	-0.8	mA
Clear	I_{IL}	—	-1.6	—	-1.6	mA
High, $V_{IH} = 2.7\text{ V}$						
J, K	I_{IH}	—	20.0	—	20.0	μA
Clock, Set	I_{IH}	—	40.0	—	40.0	μA
Clear	I_{IH}	—	80.0	—	80.0	μA
@ V_I max, $V_I = 7.0\text{ V}$, $V_I = 5.5\text{ V}$ (WP, WA-LSD)						
J, K	I_I	—	0.1	—	0.1	mA
Clock, Set (Set, $V_I = 5.5\text{ V}$, WA-LS)	I_I	—	0.2	—	0.2	mA
Clear ($V_I = 5.5\text{ V}$, WA-LS)	I_I	—	0.4	—	0.4	mA
Output Current, $V_{CC} = 5.5\text{ V}$						
Short-Circuit	I_{OS}	-20.0	-100.0	-20.0	-100.0	mA
Supply Current, $V_{CC} = 5.5\text{ V}$	I_{CC}	—	8.0	—	8.0	mA

Timing Characteristics

VCC = 5.0 V, TA = 25°C, CL = 15 pF

Parameter	Symbol	WA-LS		WP, WA-LSD		Units
		Min	Max	Min	Max	
Propagation Delay						
Clock-to-Output, Low-to-High	tPLH	—	20.0	—	25	ns
High-to-Low	tPHL	—	30.0	—	40	ns
Clear- or Set-to-Output, Low-to-High	tPLH	—	18.0	—	25	ns
Clear- or Set-to-Output (Clock Low), High-to-Low	tPHL	—	24.0	—	40	ns
Clear- or Set-to-Output (Clock High), High-to-Low	tPHL	—	35.0	—	40	ns
Operating Conditions						
Clock, Clear, Set Pulse Width	tw _{OH}	25.0	—	25	—	ns
Setup Time, Low	tdSL	20.0	—	25	—	ns
High	tdSH	20.0	—	35	—	ns
Hold Time, Low	tdHL	5.0	—	5	—	ns
High	tdHH	5.0	—	5	—	ns
Maximum Clock Frequency	f _{max}	30.0	—	25	—	ns

Maximum Ratings

Power supply voltage (VCC) 7.0 V

Operating temperature (TA) WA-LS: -55 to +125°C

WP90224L13: 0 to 70°C

WA-LSD, WP91398L4: -40 to +85°C

Storage temperature (Tstg) -65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

The timing diagram illustrates the relationship between the Input, Clock, and two Outputs of the 74VHC00. The Input signal is a square wave with a high level of 3.0 V and a low level of 0.0 V. The Clock signal is a square wave with a high level of 1.3 V and a low level of 0.0 V. The two Output signals are also square waves, with high levels labeled V_{OH} and low levels labeled V_{OL} . The diagram shows the propagation delay from the Input to the Outputs, the setup and hold times for the Clock, and the output transition times. Key timing parameters are labeled: t_{DHL} (output delay from Input high to low), t_{DHH} (output delay from Input high to high), t_{DSL} (output delay from Input low to low), t_{DHL} (output delay from Input low to high), $t_{w(OH)}$ (output high pulse width), t_{PHL} (output delay from Clock high to low), t_{PLH} (output delay from Clock low to high), t_{PLH} (output delay from Clock high to low), and t_{PHL} (output delay from Clock low to high).

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