LINEAR INTEGRATED CIRCUIT

LS159

HIGH RELIABILITY TRANSISTOR ARRAY

The LS159 is an array of 5 NPN transistors on a common monolithic substrate in an SO-14 (14-lead plastic micropackage). This package is easily mounted on thick and thin film hybrid circuits. Two transistors are internally connected to form a differential amplifier. The transistors of the LS159 are well suited to low noise general purposes and to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete components in conventional circuits; in addition they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The device is also available with a ermetic goldchip (LS8159M) that is particularly suitable for professional and telecom applications, wherever very high MTBF are required. This performance is guaranteed by silicon nitride sealing of chip surface and Ti-Pt-Au metallization, protected with a double passivated layer, providing resistance against contamination, electrolytic corrosion and electromigration.

ABSOLUTE MAXIMUM RATINGS

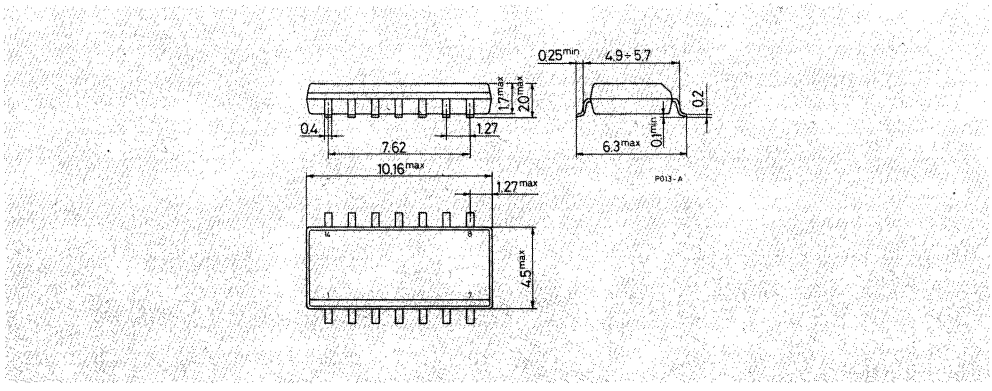
		Each transistor	Total package
V_{CBO}	Collector-base voltage ($I_E = 0$)	20 V	–
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	15 V	–
V_{CSS}*	Collector--substrate voltage	20 V	–
V_{EBO}	Emitter-base voltage ($I_C = 0$)	5 V	–
I_C	Collector current	50 mA	–
P_{tot}	Total power dissipation at $T_{amb} = 25°C$	250 mW	500 mW
T_{stg}, T_j	Storage, and junction temperature	-55 to 150 °C	
	Soldering dip or wave at 5 s	260 °C	
	11 s	235 °C	

*) The collector of each transistor of the LS159 is isolated from the substrate by an integrated diode. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ORDERING NUMBERS: LS 159M – LS 8159M

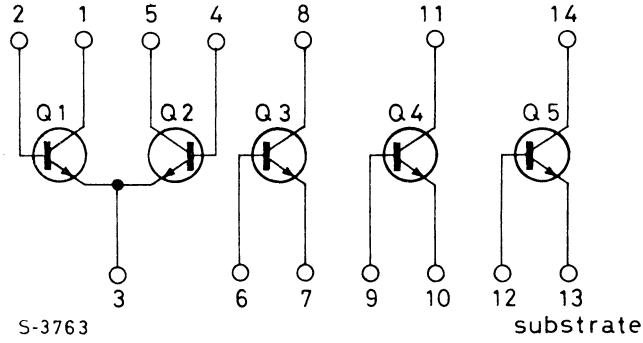
MECHANICAL DATA

Dimensions in mm



LS159

SCHEMATIC DIAGRAM



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	250	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb}= 25°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
I_{CBO}	Collector cutoff current (I_E = 0)	V_{CB}= 10V		0.002	40	nA	1
I_{CEO}	Collector cutoff current (I_B = 0)	V_{CE}= 10V		see curve	0.5	μA	2
$\lvert I_{B1}-I_{B2}\rvert$	Input offset current	I_C = 1 mA V_{CE}= 3V		0.3	2	μA	7
V_{CBO}	Collector-base voltage (I_E = 0)	I_C = 10 μA	20	60		V	—
V_{CEO}	Collector-emitter voltage (I_B = 0)	I_C = 1 mA	15	24		V	—
V_{CSS}	Collector-substrate voltage (I_{CSS}= 0)	I_C = 10 μA	20	60		V	—
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 10 mA I_B = 1 mA		0.23		V	—

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig.
V_{EBO}	Emitter-base voltage ($I_C = 0$)	$I_E = 10\ \mu A$	5	7		V	–
V_{BE}	Base-emitter voltage	$I_E = 1$ mA $V_{CE} = 3V$ $I_E = 10$ mA $V_{CE} = 3V$		0.71 0.8		V V	4
$\lvert V_{BE1}-V_{BE2}\rvert$	Input offset voltage	$I_C = 1$ mA $V_{CE} = 3V$		0.45	5	mV	4-6
$\lvert V_{BE3}-V_{BE4}\rvert$	Input offset voltage						
$\lvert V_{BE4}-V_{BE5}\rvert$	Input offset voltage						
$\lvert V_{BE5}-V_{BE4}\rvert$	Input offset voltage						
$\frac{\Delta V_{BE}}{\Delta T}$	Base-emitter voltage temperature coefficient	$I_C = 1$ mA $V_{CE} = 3V$		-1.9		mV/°C	5
$\frac{\lvert V_{BE1}-V_{BE2}\rvert}{\Delta T}$	Input offset voltage temperature coefficient	$I_C = 1$ mA $V_{CE} = 3V$		1.1		µV/°C	6
h_{FE}	DC current gain	$I_C = 10$ mA $V_{CE} = 3V$ $I_C = 1$ mA $V_{CE} = 3V$ $I_C = 10\ \mu A$ $V_{CE} = 3V$	40	100 100 54		– – –	3
f_T	Transition frequency	$I_C = 3$ mA $V_{CE} = 3V$	300	550		MHz	14
NF	Noise figure	$I_C = 100\ \mu A$ $V_{CE} = 3V$ $R_g = 1\ k\Omega$ $f = 1$ kHz		3.25		dB	8
h_{ie}	Input impedance	$I_C = 1$ mA $V_{CE} = 3V$ f = 1 KHz		3.5		kΩ	9
h_{fe}	Forward current transfer ratio			110		–	
h_{re}	Reverse voltage transfer ratio			1.8×10^{-4}		–	
h_{oe}	Output admittance			15.6		µS	
y_{ie}	Input admittance	$I_C = 1$ mA $V_{CE} = 3V$ f = 1 MHz		0.3+j0.04		mS	11
y_{fe}	Forward transadmittance			31-j1.5		mS	10
y_{re}	Reverse transadmittance			see curve		mS	13
y_{oe}	Output admittance			0.001+j0.03		mS	12
C_{EBO}	Emitter-base capacitance	$I_C = 0$ $V_{EB} = 3V$		0.6		pF	–
C_{CBO}	Collector-base capacitance	$I_E = 0$ $V_{CB} = 3V$		0.58		pF	–
C_{CSS}	Collector-substrate capacitance	$I_C = 0$ $V_{CSS} = 3V$		2.8		pF	–

Fig. 1 - Collector cutoff current vs. ambient temperature

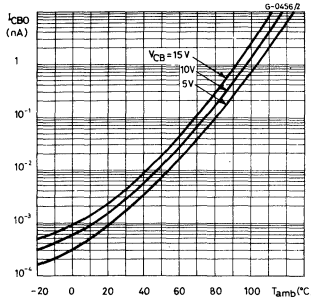


Fig. 2 - Collector cutoff current vs. ambient temperature

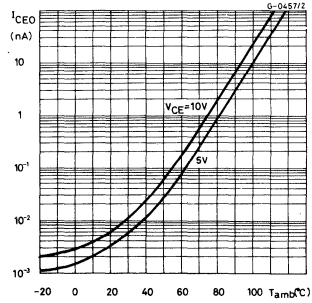


Fig. 3 - DC current gain

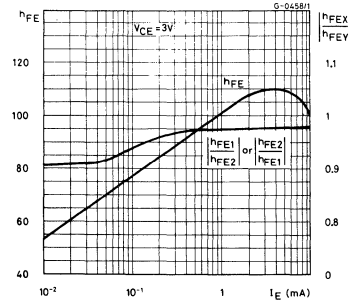


Fig. 4 - Input voltage and input offset voltage vs. emitter current

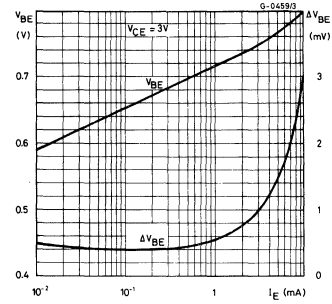


Fig. 5 - Input characteristics for each transistor

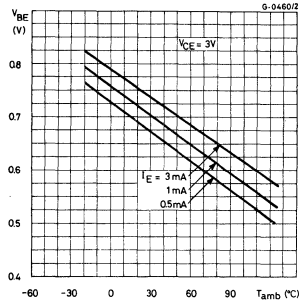


Fig. 6 - Input offset voltage vs. ambient temperature

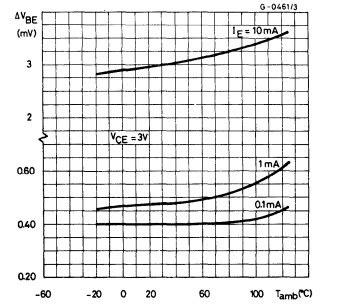


Fig. 7 - Input offset current for matched transistor pair

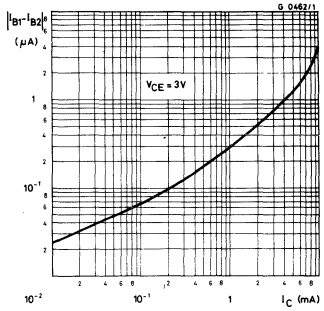


Fig. 8 - Noise figure vs. collector current

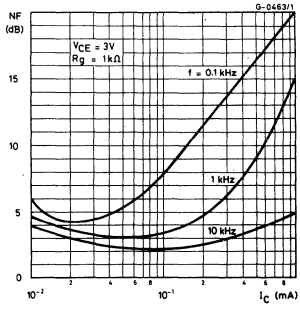


Fig. 9 - Normalized h parameters vs. collector current

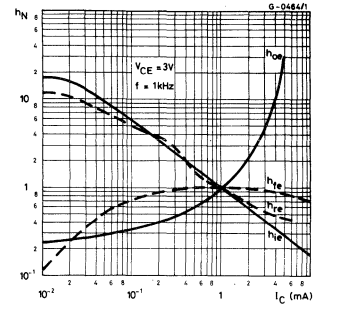


Fig. 10 - Forward admittance vs. frequency

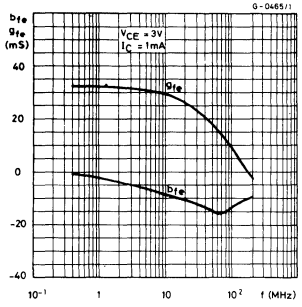


Fig. 11 - Input admittance vs. frequency

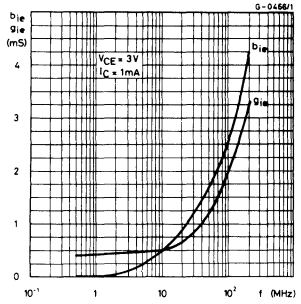


Fig. 12 - Output admittance vs. frequency

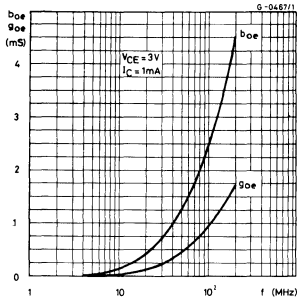


Fig. 13 - Reverse admittance vs. frequency

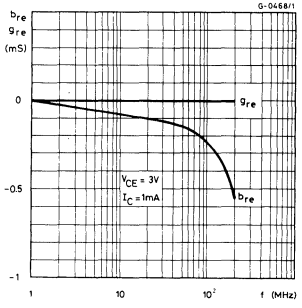


Fig. 14 - Transition frequency vs. collector current