

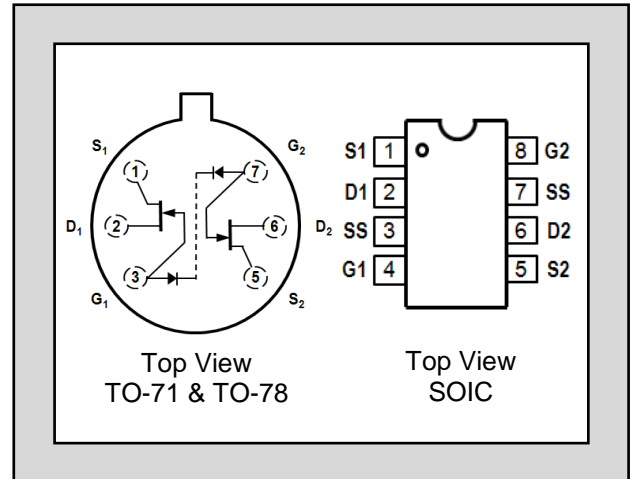
LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

LS3954A LS3954 LS3955 LS3956 LS3958

LOW NOISE LOW DRIFT
MONOLITHIC DUAL N-CHANNEL
JFET AMPLIFIER

FEATURES	
LOW DRIFT	$ dV_{GS1-2}/dT = 5\mu V/^{\circ}C$ max.
LOW LEAKAGE	$I_G = 20pA$ TYP.
LOW NOISE	$e_n = 10Nv/\sqrt{Hz}$ TYP.
ABSOLUTE MAXIMUM RATINGS ¹ @ 25 °C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Operating Junction Temperature	-55 to +150°C
Maximum Voltage and Current for Each Transistor ¹	
-V _{GSS}	Gate Voltage to Drain or Source 60V
-I _{G(f)}	Gate Forward Current 50mA
Maximum Power Dissipation	
Device Dissipation @ Free Air - Total	400mW @ 25°C ²

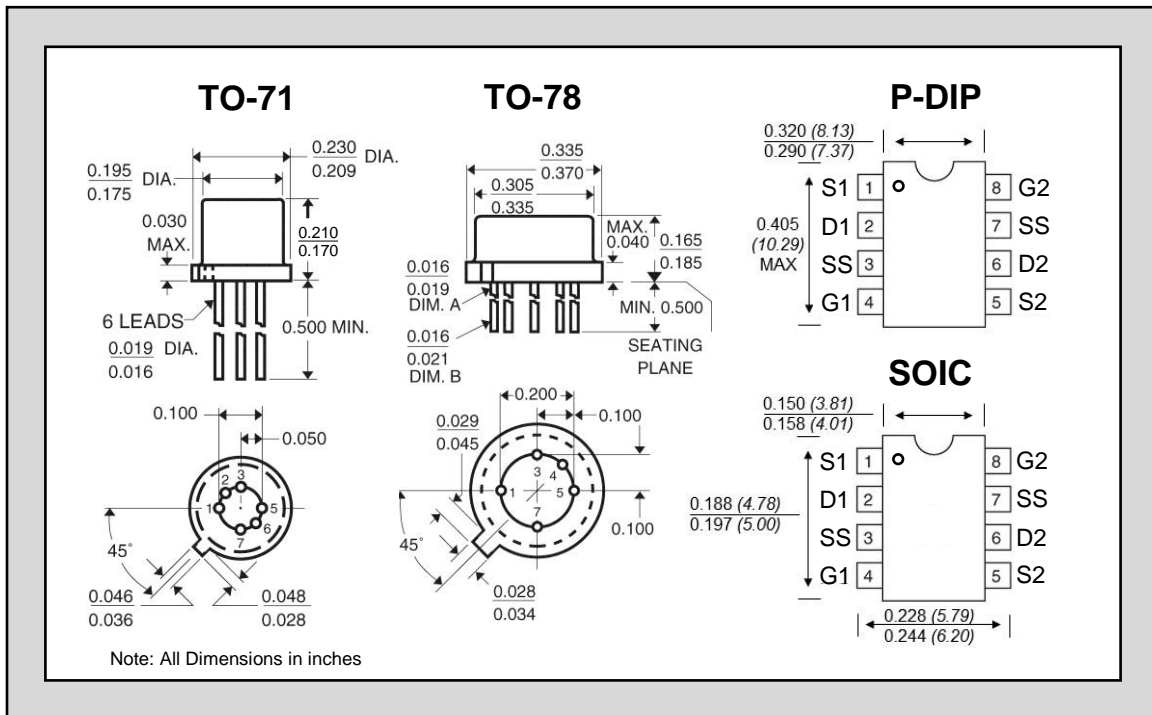


ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS3954A	LS3954	LS3955	LS3956	LS3958	UNITS	CONDITIONS
$ dV_{GS1-2}/dT $ max.	Drift vs. Temperature	5	10	25	50	100	$\mu V/^{\circ}C$	$V_{DG} = 20V, I_D = 200\mu A$ $T_A = -55^{\circ}C$ to $+125^{\circ}C$
$ V_{GS1-2} $ max.	Offset Voltage	5	5	10	15	25	mV	$V_{DG} = 20V, I_D = 200\mu A$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	60	--	--	V	$V_{DS} = 0, I_G = 1\mu A$
BV _{GGO}	Gate-to-Gate Breakdown	60	--	--	V	$I_{GG} = \pm 1\mu A, I_D = 0, I_S = 0$
TRANSCONDUCTANCE						
g_{fss}	Full Conduction	1000	2000	4000	μS	$V_{DG} = 20V, V_{GS} = 0, f = 1kHz$
g_{fs}	Typical Operation	500	700	1250	μS	$V_{DG} = 20V, I_D = 200\mu A$
$ g_{fs1-2}/g_{fs} $	Differential	--	± 0.6	± 3	%	
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	2	5	mA	$V_{DS} = 20V, V_{GS} = 0$
$ I_{DSS1-2}/I_{DSS} $	Differential	--	± 1	± 5	%	
GATE VOLTAGE						
$V_{GS(off)}$	Pinchoff Voltage	-1	-2	-4.5	V	$V_{DS} = 20V, I_D = 1nA$
V_{GS}	Operating Range	-0.5	--	-4	V	$V_{DS} = 20V, I_D = 200\mu A$
GATE CURRENT						
-I _G	Operating	--	20	50	pA	$V_{DG} = 20V, I_D = 200\mu A$
-I _G	High Temperature	--	--	50	nA	$V_{DG} = 20V, I_D = 200\mu A, T_A = +125^{\circ}C$
-I _G	Reduced V _{DG}	--	5	--	pA	$V_{DG} = 10V, I_D = 200\mu A$
-I _{GSS}	At Full Conduction	--	--	100	pA	$V_{DG} = 20V, V_{DS} = 0$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
OUTPUT CONDUCTANCE						
g_{oss}	Full Conduction	--	--	35	μS	$V_{DG}=20V$ $V_{GS}=0$
g_{os}	Operating	--	0.5	1	μS	$V_{DG}=20V$ $I_D=200\mu A$
$ g_{os1-2} $	Differential	--	0.05		μS	
COMMON MODE REJECTION						
CMRR	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	100	--	dB	$\Delta V_{DS}=10$ to $20V$ $I_D=200\mu A$
CMRR	$-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	--	75	--	dB	$\Delta V_{DS}=5$ to $10V$ $I_D=200\mu A$
NOISE						
NF	Figure	--	--	0.5	dB	$V_{DS}=20V$ $V_{GS}=0$ $R_G=10M\Omega$ $f=100Hz$ $NBW=6Hz$
e_n	Voltage	--	--	15	nV/\sqrt{Hz}	$V_{DS}=20V$ $I_D=200\mu A$ $f=10Hz$ $NBW=1Hz$
CAPACITANCE						
C_{ISS}	Input	--	--	6	pF	$V_{DS}=20V$ $V_{GS}=0$ $f=1MHz$
C_{RSS}	Reverse Transfer	--	--	2	pF	
C_{DD}	Drain-to-Drain	--	0.1	--	pF	$V_{DG}=20V$ $I_D=200\mu A$



NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate $4mW/^\circ C$ above $25^\circ C$

Information furnished by Linear Integrated Systems is believed to be accurate and reliable. However, no responsibility is assumed for its use; nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Linear Integrated Systems.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.