LINEAR SYSTEMS

LS3N191
P-CHANNEL MOSFET

micross

The LS3N191 is a monolithic dual enhancement mode P-Channel Mosfet

The LS3N191 is a dual enhancement mode P-Channel Mosfet and is ideal for space constrained applications and those requiring tight electrical matching.

The hermetically sealed TO-78 package is well suited for high reliability and harsh environment applications.

(See Packaging Information).

LS3N191 Features:

- Very high Input Impedance
- High Gate Breakdown Voltage
- Low Capacitance

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL LS3N191	
LOW GATE LEAKAGE CURRENT	$I_{GSS} \leq \pm 10pA$
LOW TRANSFER CAPACITANCE	$C_{rss} \leq 1.0pF$
ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	-55°C to +135°C
Maximum Power Dissipation	
Continuous Power Dissipation (one side)	300mW
Continuous Power Dissipation (one side)	525mW
MAXIMUM CURRENT	
Drain to Source[2]	50mA
MAXIMUM VOLTAGES	
Drain to Gate or Drain to Source[2]	-30V
Transient Gate to Source[2,3]	±125V
Gate-Gate Voltage	±80V

LS3N191 ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP.	MAX	UNITS	CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40	--	--	V	I_D = -10µA
BV_{SDS}	Source to Drain Breakdown Voltage	-40	--	--		I_S = -10µA, V_{BD} = 0V
V_{GS}	Gate to Source Voltage	-3.0	--	-6.5		V_{DS} = -15V, I_D = -500µA
$V_{GS(th)}$	Gate to Source Threshold Voltage	-2.0	--	-5.0		V_{DS} = -15V, I_D = -500µA
		-2.0	--	-5.0		V_{DS} = V_{GS}, I_D = -10µA
I_{GSSR}	Gate Reverse Leakage Current	--	--	10	pA	V_{GS} = 40V
I_{GSSF}	Forward Gate Leakage Current	--	--	-10		V_{GS} = -40V
I_{DSS}	Drain to Source Leakage Current	--	--	-200		V_{DS} = -15V
I_{SDS}	Source to Drain Leakage Current	--	--	-400		V_{SD} = -15V V_{DB} = 0
$I_{D(on)}$	Drain Current "On"	-5.0	--	-30	mA	V_{DS} = -15V, V_{GS} = -10V
$r_{DS(on)}$	Drain to Source "On" Resistance	--	--	300	Ω	V_{DS} = -20V, I_D = -100µA
g_{fs}	Forward Transconductance[4]	1500	--	4000	µS	V_{DS} = -15V, I_D = -5mA, f = 1kHz
Y_{os}	Output Admittance	--	--	300		
C_{iss}	Input Capacitance	--	--	4.5	pF	V_{DS} = -15V, I_D = -5mA, f = 1MHz
C_{rss}	Reverse Transfer Capacitance	--	--	1.0		
C_{oss}	Output Capacitance	--	--	3.0		

MATCHING CHARACTERISTICS LS3N191

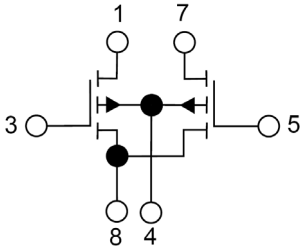
SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS MAX	UNITS	CONDITIONS
g_{fs1}/g_{fs2}	Forward Transconductance Ratio	0.85	1.0	ns	V_{DS} = -15V, I_D = -500µA, f = kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential[5]	--	100	mV	V_{DS} = -15V, I_D = -500µA
$\Delta V_{GS1-2}/\Delta T$	Gate Source Threshold Voltage Differential Change with Temperature[5]	--	100	µV/°C	V_{DS} = -15V, I_D = -500µA, T_S = -55°C to +25°C
					V_{DS} = -15V, I_D = -500µA, T_S = +25°C to +125°C

SWITCHING CHARACTERISTICS

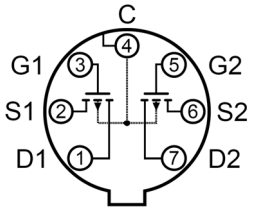
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$t_{d(on)}$	Turn On Delay Time	--	--	15	ns	V_{DD} = -15V, $I_{D(on)}$ = -5mA, $R_G = R_L$ = 1.4KΩ
t_r	Turn On Rise Time	--	--	30		
t_{off}	Turn Off Time	--	--	50		

Note 1 - Absolute maximum ratings are limiting values above which LS3N191 serviceability may be impaired.
Note 2 – Per Transistor
Note 3 – Approximately doubles for every 10°C in T_A
Note 4 – Measured at end points, T_A and T_B
Note 5 – Pulse: t= 300µS, Duty Cycle ≤ 3%

Device Schematic



TO-78 (Bottom View)



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Available Packages:

LS3N191 in TO-72
LS3N191 in bare die.

Please contact Micross for full package and die dimensions