

LIGHTNING

Semiconductor
Devices

⚡ LS4558N/D/F

DUAL OPERATIONER AMPLIFIER

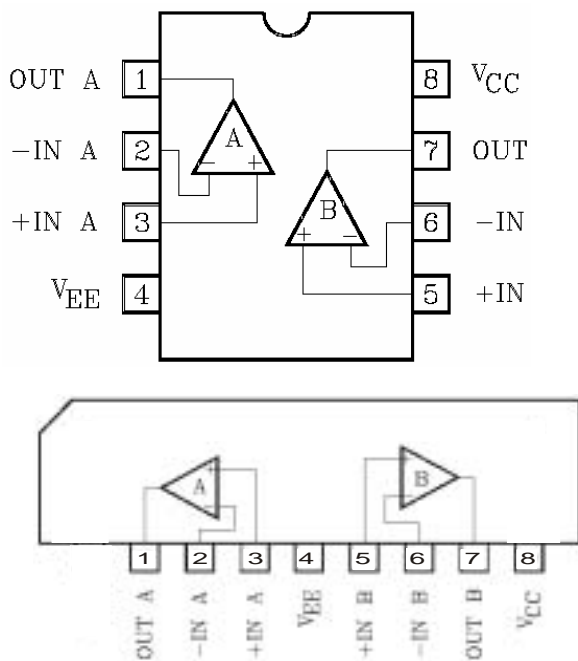
GENERAL DESCRIPTION

The LS4558N/D/F is a dual high-gain operational amplifier internally compensated and constructed on a single silicon chip using an advanced epitaxial process. It offers high speed, a wide band width, and low noise. Outstanding thermal characteristics and voltage gain band width make these ICs ideal for use in a wide variety of electronic circuits.

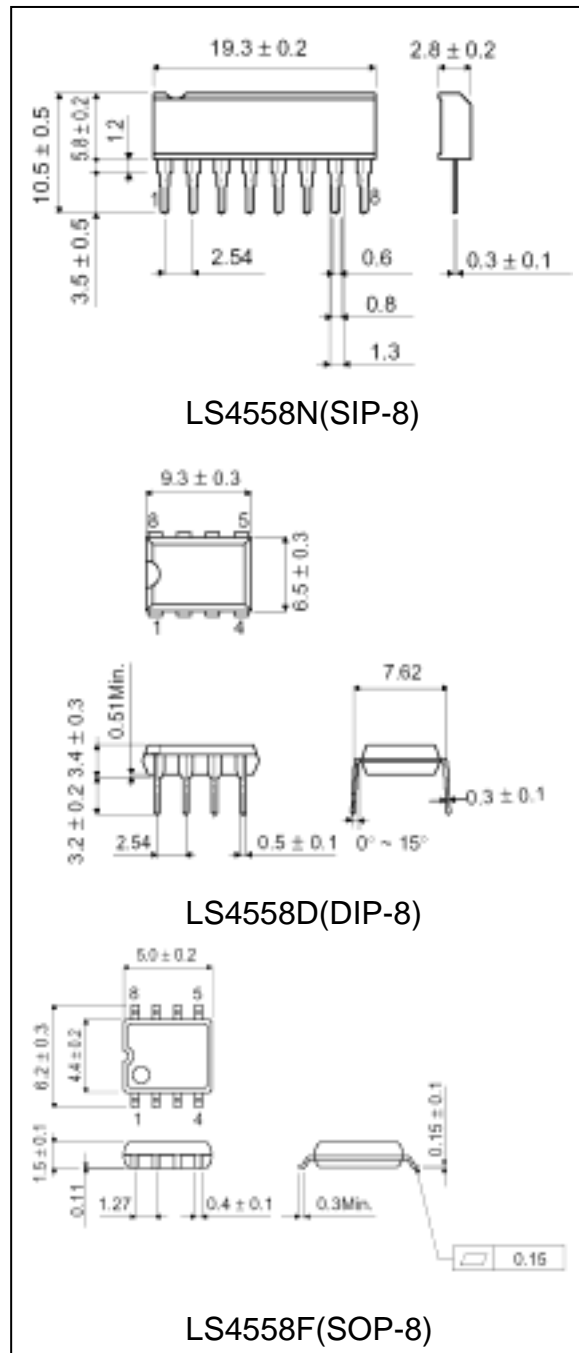
FEATURES

- Operating Voltage ($\pm 4V \sim \pm 18V$)
- High Voltage Gain (100dB typ.)
- High Input Resistance (5M typ.)
- Package Outline DIP8, SIP8, SOP8
- Bipolar Technology

PIN CONNFIGURATION



PACKAGE OUTLINE

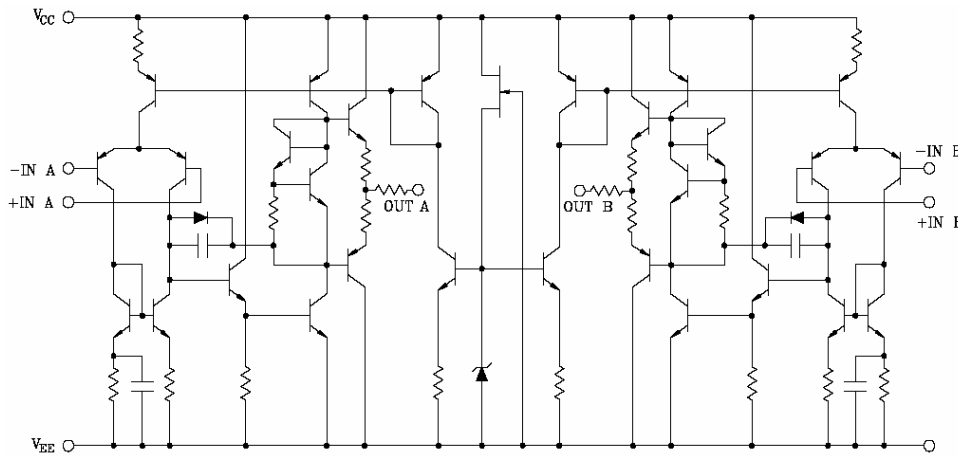


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EQUIVALENT CIRCUIT



**ABSOLUTE
MAXIMUM
RATINGS**


PARAMETER	SYMBOL	RATINGS		UNIT
Supply Voltage	V_{CC}	± 18		V
Differential Input Voltage	$V_{I(DIFF)}$	± 15		V
Input Voltage	V_{IC}	± 15		V
Power Dissipation	P_D	DIP8	500	mW
		SIP8	800	
		SOP8	300	
Operating Temperature Range	T_{opr}	0~+70		
Storage Temperature Range	T_{stg}	-45~+125		

ELECTRICAL CHARACTERISTICS ($T_{amb}=25$, $V_{CC}=15$, $V_{EE}=-15V$, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	LIMITED			UNIT
			MIN	TYP	MAX	
Operating Current		I_{CC}		3.5	5.6	mA
Input Offset Voltage	R_S 10k Ω	V_{IO}	-	2	6.0	mV
Input offset Current		I_{IO}		5	200	nA
Input Bias Current		I_{BIAS}	-	30	500	nA
Large Signal Voltage Gain	R_L 2k Ω , V_o (p-p) = $\pm 10V$,	A_v	86	100		dB
Input Common Mode Voltage Range		V_{ICM}	± 12	± 14	-	V
Maximum Output Voltage Swing	R_L 10k Ω	V_o (p-p)	± 12	± 14	-	V
	R_L 2k Ω		± 10	± 13	-	
Common Mode Rejection Ratio	R_S 10k Ω	$CMRR$	70	90	-	dB
Supply Voltage Rejection Ratio	R_S 10k Ω	$PSRR$	75	90	-	dB
slew rate		SR	-	2	-	V/ μ S
Equivalent Input Noise Voltage	$R_s=1k\Omega, 30kHz$ LPF	V_{NI}	-	1.5	-	V/ μ S
Gain Bandwidth Product		GB	-	3	-	MHz

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TYPICAL CHARACTERISTICAL

图 1 Burst Noise vs Rs

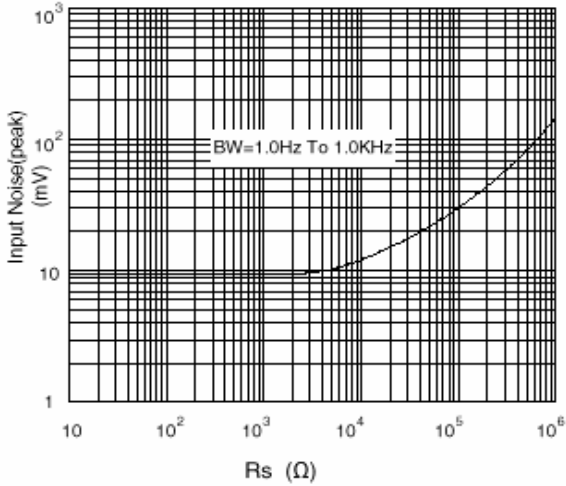


图 2 RMS Noise vs Rs

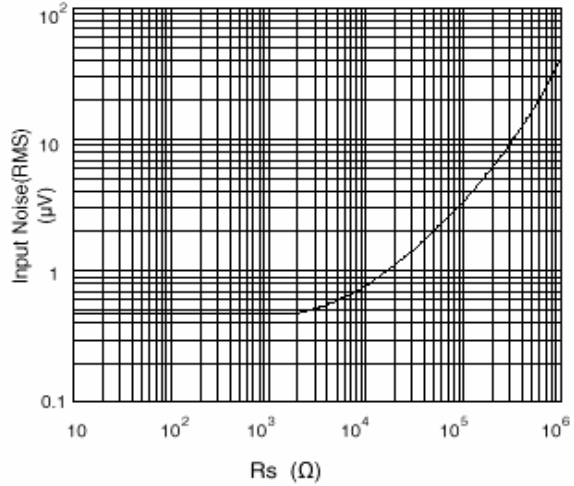


图 3 Output Noise vs Rs

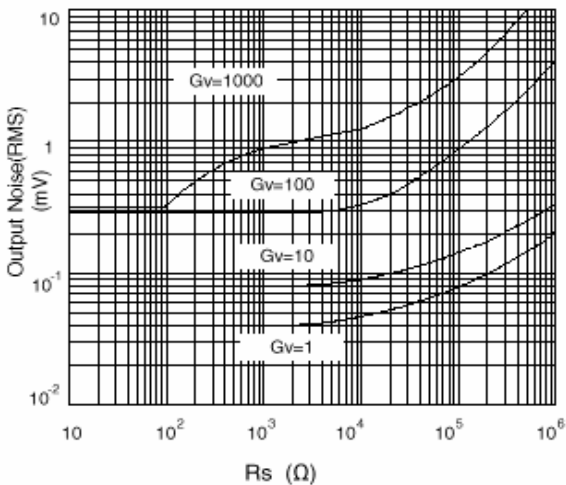


图 4 Spectral Noise Density

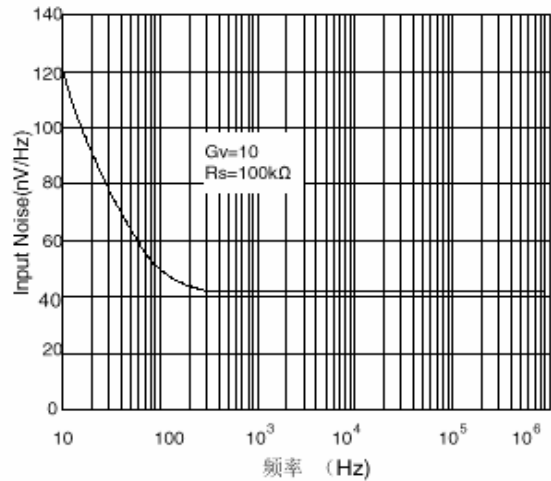


图 5 开环频率响应

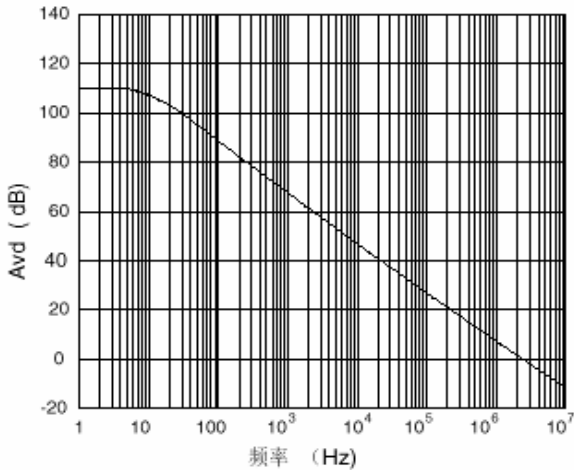
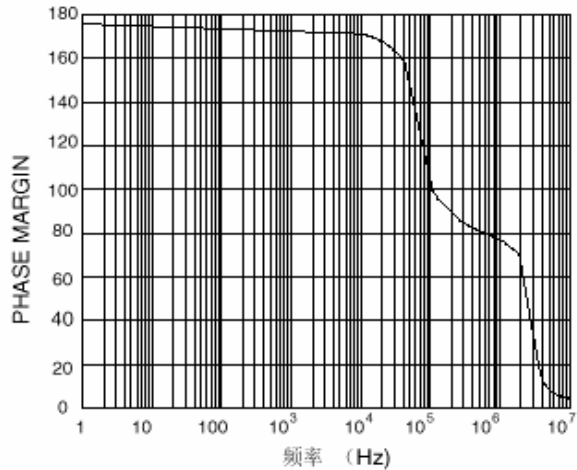


图 6 PHASE MARGIN vs FREQUENCY



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图 7 正输出逻辑摆幅与负载电阻的关系

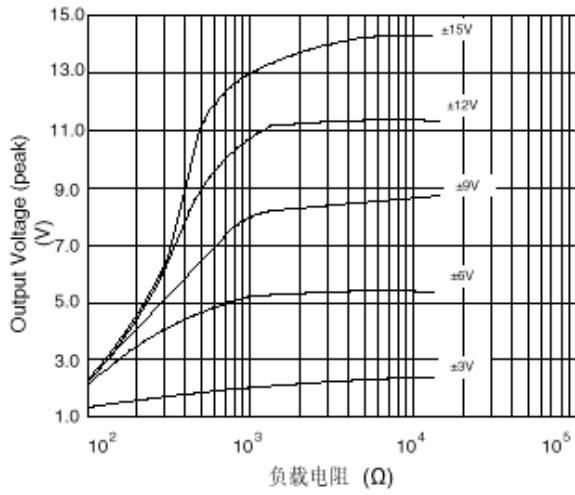


图 8 负输出逻辑摆幅与负载电阻的关系

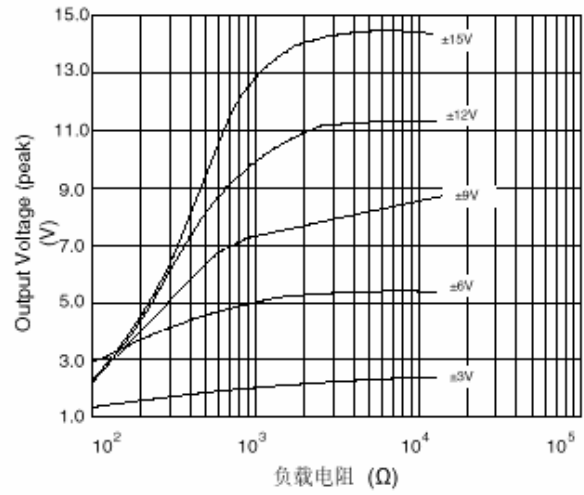


图 9 大信号输出与频率的关系

