LS521

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ILLUMINATION-TO-DIGITAL CONVERTER

with SMBUS INTERFACE

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ILLUMINATION-TO-DIGITAL CONVERTERS

GENERAL DESCRIPTION

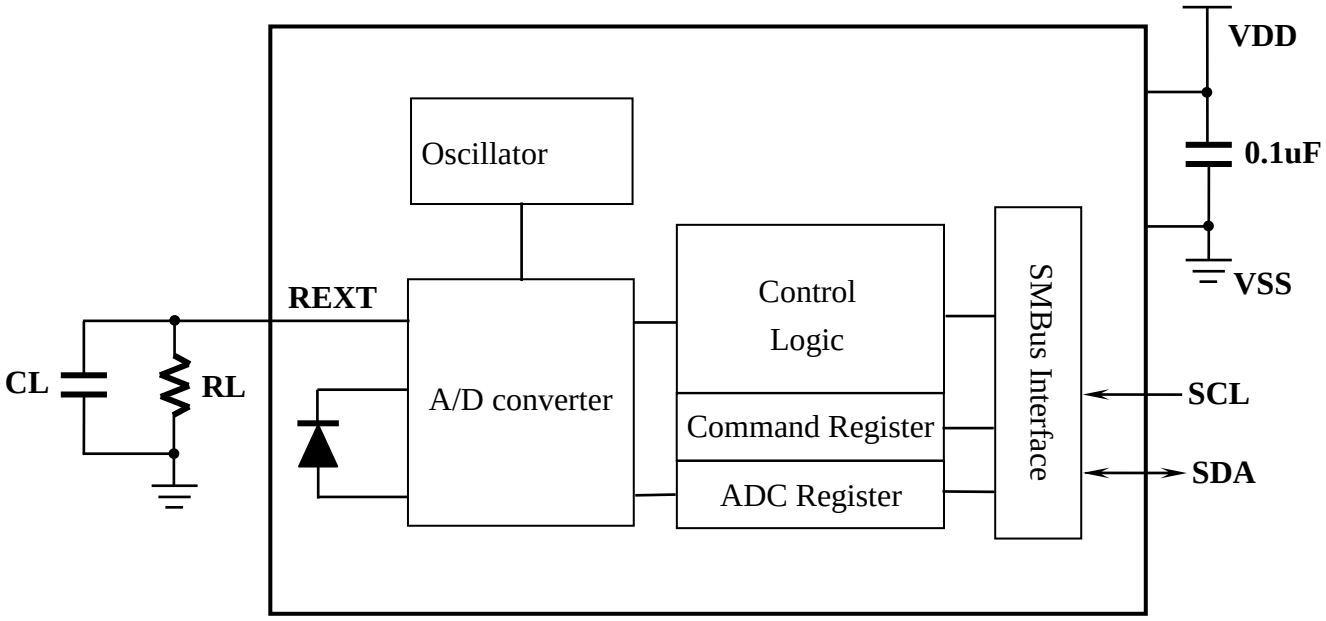
The LS521 is a low-noise, high-sensitivity and illumination-to-digital converter with two-wire SMBus serial interface. The device integrates a photodiode, a trans-impedance amplifier, and 8-bits analog-to-digital converter (ADC) in a single IC to provide illumination information over an effective 8-bit dynamic range. The digital output is directly proportional to ambient illumination. The LS521 is characterized with the C.I.E. response as the human eye's visual response, which peaks at 555nm.

Illumination information can be used to control display panel backlighting with the purpose of extending battery life and providing optimum viewing in diverse lighting conditions. Also, illumination information can further be used to manage exposure control in digital cameras and camcorders. The LS521 device is ideal in notebook/tablet PCs, flat-panel televisions, cellular phones, LCD monitors, digital cameras, camcorder, and street/room lighting control, etc.

FEATURES

1. Characterized with the C.I.E. response as the human eye's response
2. 8-bit linear digital output for ambient illumination with two wire SMBus interface.
3. Tunable illumination sensitivity by an external resistor
4. Rejection of 50Hz/60Hz light ripple by an external resistor (R_L) and an external capacitor (C_L)
5. Wide power supply range (2.7~5.5V)
6. Low power dissipation in shut-down mode.
7. Tiny SMD type package:
   Width: 3.0mm/Height: 3.0 mm/Depth: 1.1mm
   Width: 2.0mm/Height: 2.0 mm/Depth: 0.63mm
8. High sensing illuminance range (0~14000 lux).

FUNCTIONAL BLOCK DIAGRAM and APPLICATION



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	-0.4 ~ 6	V
Input Voltage for SCLK, SDA, REXT	V_{IN}	-0.4 ~ V_{DD}+0.4	mA
Input Current for SCLK, SDA	I_{IN}	+20	mA
Output Current for SDA	I_{OUT}	-1	mA
Operating Temperature	Topr	-25 to +85	℃
Storage Temperature	Tstg	-40 to +125	℃
Electrostatic Damage, (HBM)	ESD	3	kV

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	2.7		5.5	V
Operating Temperature	Topr	-25		85	℃
Input Low Voltage for SCLK, SDA	V_{IL}			0.8	V
Input High Voltage for SCLK, SDA	V_{IH}	2.1		VDD	V
Operating Frequency for SCLK	f_{SCLK}	10		400	KHz

ELECTRICAL CHARACTERISTICS (V_{DD}=3V, T_A=25℃ if not mentioned)

Item	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
SMBus Output Low Voltage	V_{OL}	I_O =10uA		-	0.01	-	V
		I_O =350uA		-	-	0.4	V
Supply Current	I_{DD}	Power-up, V_{SMBCLK} =V_{SMBDAT}=V_{DD}, Ee =0,	V_{DD} =3V	-	0.38	0.43	mA
			V_{DD} =5.5V	-	0.65	0.75	
		Power-down, V_{SMBCLK}=V_{SMBDAT}= V_{DD}, Ee =0	V_{DD} =3V	-	30	35	uA
			V_{DD} =5.5V	-	80	92	
		Shut-down ADC, V_{SMBCLK}=V_{SMBDAT}=V_{DD}, Ee =0	V_{DD} =3V	-	0.33	0.38	mA
			V_{DD} =5.5V	-	0.6	0.7	
High Level Input Current	I_{IH}	V_{SDA}(or V_{SCL})=V_{DD}		-	-	5	uA
Low Level Input Current	I_{IL}	V_{SDA}(or V_{SCL})= 0V		-	-	-5	uA

DC OPERATING CHARACTERISTICS (V_{DD}=3V, T_A=25℃, RL=11.9kΩ, CL=100uF, unless otherwise noted)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Full scale ADC count	-	-	-	-	255	counts
ADC count value	D_{OUT}	Ee =0	-	0	2	counts
		Ee =400 lux, Fluorescent light (note.1)	83	104	125	
Illuminance responsivity	Rv	Fluorescent light (note.1)	0.208	0.26	0.312	counts/ lux

NOTE: 1. Using a white LED as the fluorescent light source.

MAXIMUM ILLUMINANCE RANGE SETTING

Max. illuminance range(LUX)	1000	2000	5000	14000
R_L(KΩ)	12	6	2.4	0.857

Table 1. Maximum illuminance range vs R_L

For example, if we need the maximum illuminance range to be 2000 lux, then

$$RL = \frac{1200}{0.1 \times 2000} = 6(K\Omega)$$ where 1200 and 0.1 are constants, 2000 is max. lux

REJECTION OF LIGHT RIPPLE

Cut off frequency(Hz)	60		1	
R_L (kΩ)	6	2.4	6	2.4
C_L (uF)	0.45	1.2	27	67

Table 2. R_L , C_L setting

For example, if light ripple(f)=60Hz, R_L=6kΩ , then

$$CL > \frac{1}{2\pi R \times f} = \frac{1}{2\pi \times 6000 \times 60} = 0.4421(uF)$$

AC OPERATING CHARACTERISTICS (V_{DD}=3V, T_A=25℃ unless otherwise noted)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$f_{(SMBCLK)}$	10	-	400	kHz
Bus free time between start and stop condition	$t_{(BUF)}$	4.7	-	-	us
Hold time after (repeated) start condition. After this period, the first clock is generated.	$t_{(HDSTA)}$	4	-	-	us
Repeated start condition setup time	$t_{(SUSTA)}$	4.7	-	-	us
Stop condition setup time	$t_{(SUSTO)}$	4	-	-	us
Data hold time	$t_{(HDDAT)}$	300	-	-	ns
Data setup time	$t_{(SUDAT)}$	250	-	-	ns
SMBCLK clock low period	$t_{(LOW)}$	4.7	-	-	us
SMBCLK clock high period	$t_{(HIGH)}$	4	-	50	us
Detect clock low timeout	$t_{(TIMEOUT)}$	25	-	35	ms
Clock/data fall time	t_F	-	-	300	ns
Clock/data rise time	t_R	-	-	1000	ns
Input pin capacitance	C_i	-	-	10	pF

PARAMETER MEASUREMENT INFORMATION

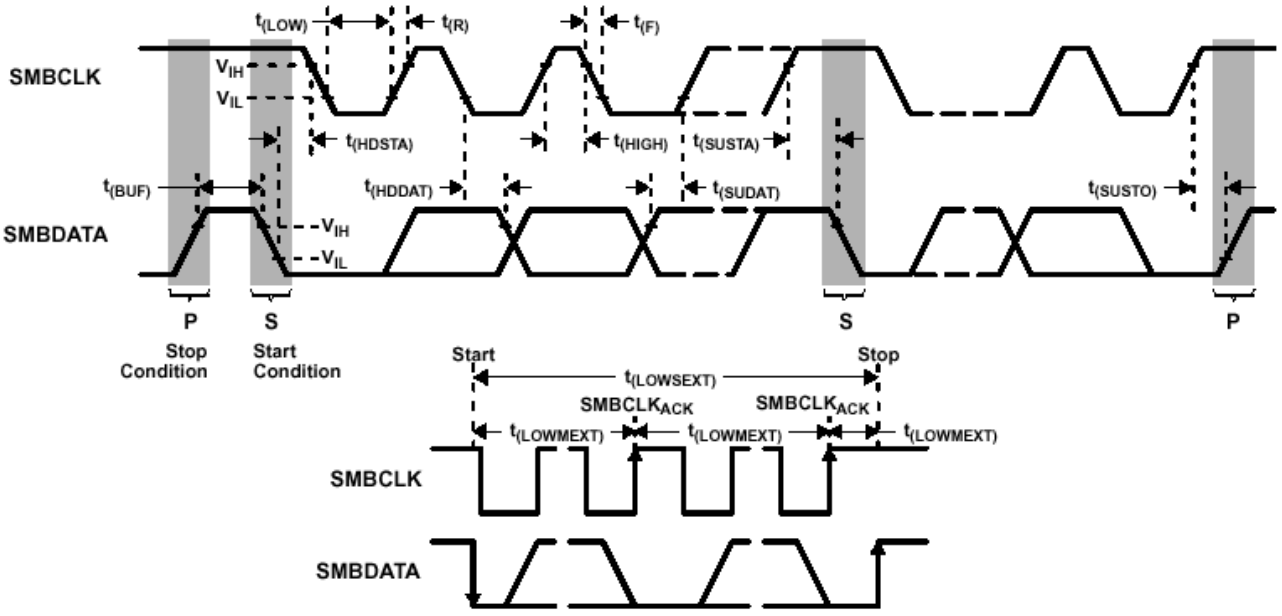


Figure 1. SMBus Timing Diagrams

SMBUS TIMING DIAGRAM

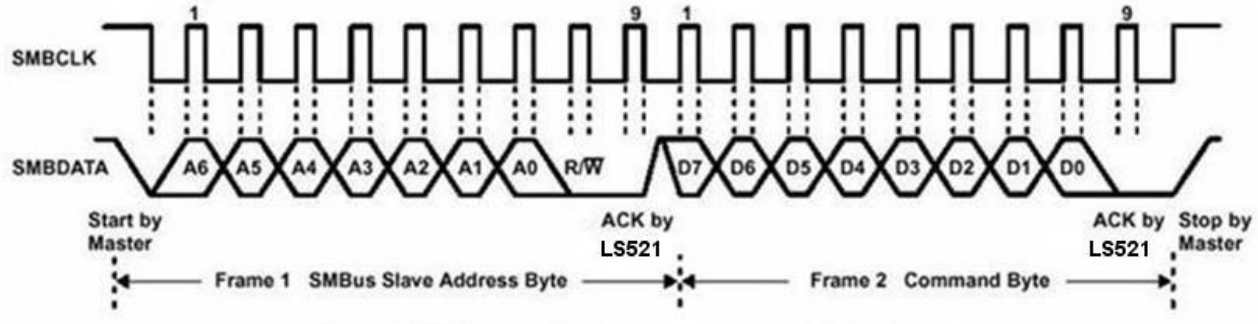


Figure 2. SMBus Timing Diagram for Send Byte Format

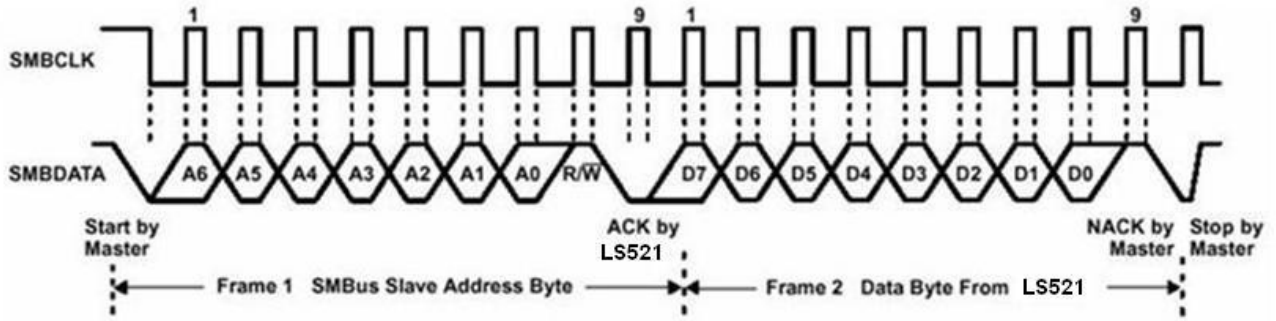


Figure 3. SMBus Timing Diagram for Receive Byte Format

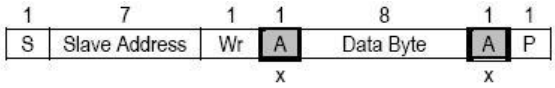
SLAVE ADDRESS SELECTION

Address	Description
0010000	Address of LS521.

COMMAND SELECTION

Command	Description
0x00h	Power-up mode/Read Data Register
0x01h	Power-down mode
0x02h	Shut down ADC
0x80h	Read Command Register

SMBUS PROTOCOLS(For more detail about SMBUS protocols, please refer to the website http://www.smbus.org/specs/)



S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
x	Shown under a field indicates that that field is required to have the value of 'x'
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
PEC	Packet Error Code
	Master-to-Slave
	Slave-to-Master
...	Continuation of protocol

Figure 4. SMBUS packet protocol diagram element key

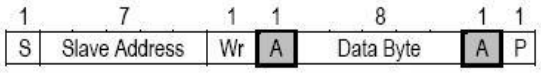


Figure 5. SMBUS send byte protocol

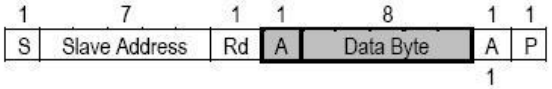


Figure 6. SMBUS receive byte protocol

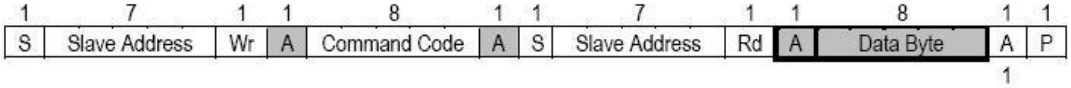


Figure 7. SMBUS read byte protocol

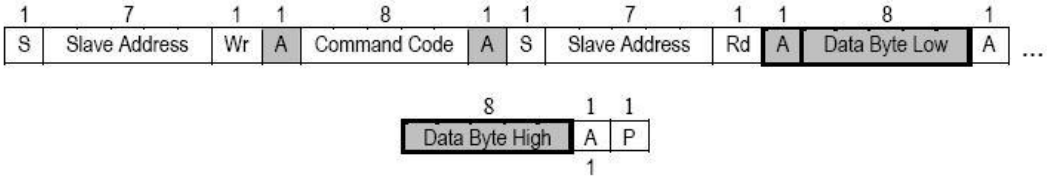
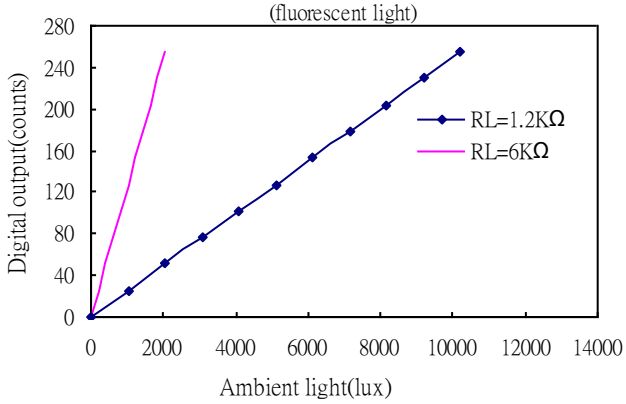
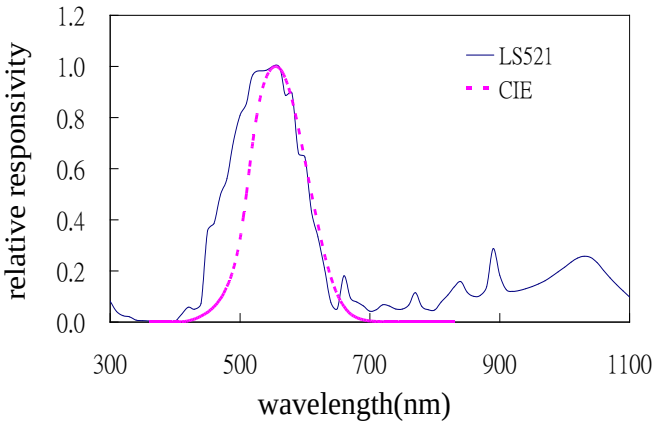


Figure 8. SMBUS read word protocol

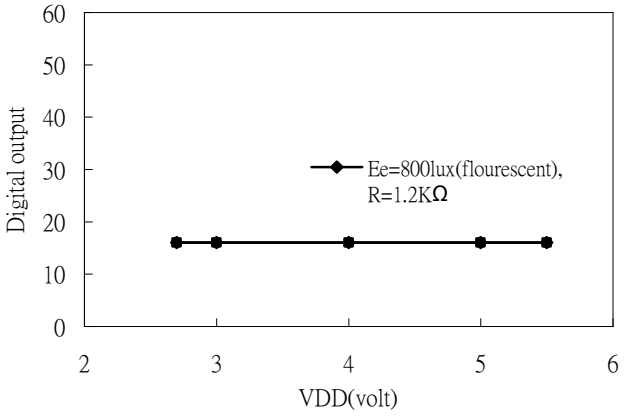
LIGHT TO DIGITAL@VDD=3V
(fluorescent light)



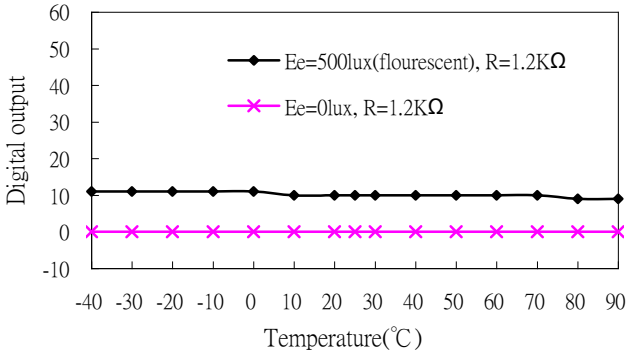
Spectral response



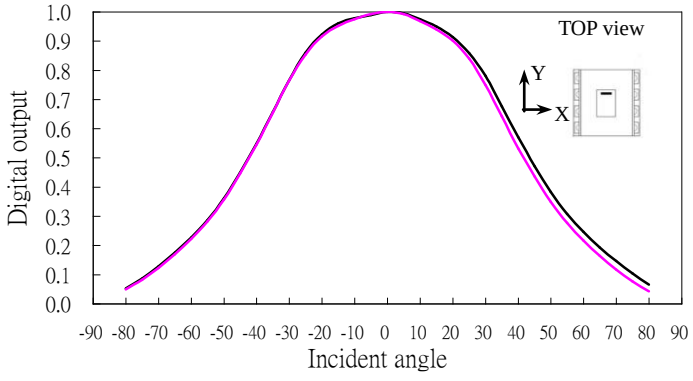
Digital variation



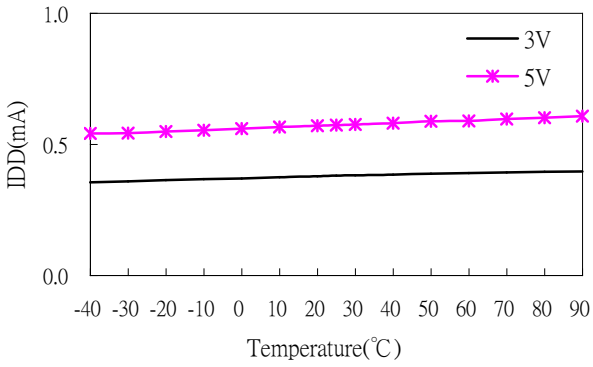
Temperature variation@VDD=3V



Incident angle vs Responsivity@VDD=3V
fluorescent light Ee=500lux



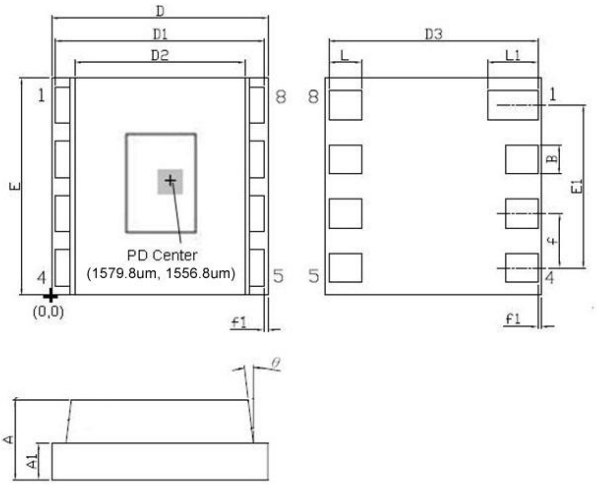
IDD vs Temp.@Ee=0lux



PACKAGE DESCRIPTIONS

- **IPLCC8 3mm x 3mm x 1.1mm**

• Top View • Bottom View

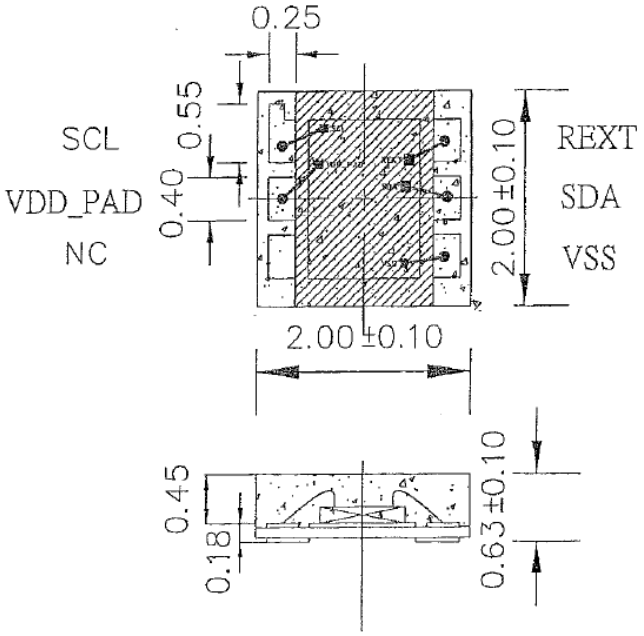


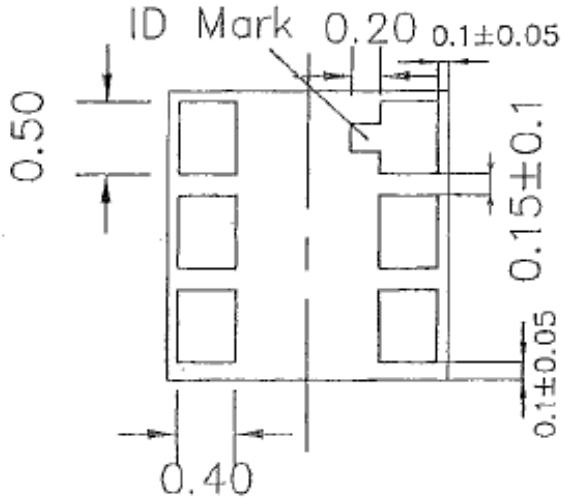
SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.900	1.100	1.300	35	43	51
A1	0.400	0.500	0.600	16	20	24
B	0.350	0.400	0.450	14	16	18
D	2.900	3.000	3.100	114	118	122
D1	2.800	2.900	3.000	110	114	118
D2	2.425	2.500	2.575	95	98	101
D3	2.800	2.900	3.000	110	114	118
E	2.900	3.000	3.100	114	118	122
E1	2.150	2.250	2.350	85	89	93
e	0.750 BASIC			30 BASIC		
f1	0.00	0.05	0.100	0	2	4
L	0.400	0.450	0.500	16	18	20
L1	0.650	0.700	0.750	26	28	30
θ	6°	7°	8°	6°	7°	8°

PAD DESCRIPTIONS

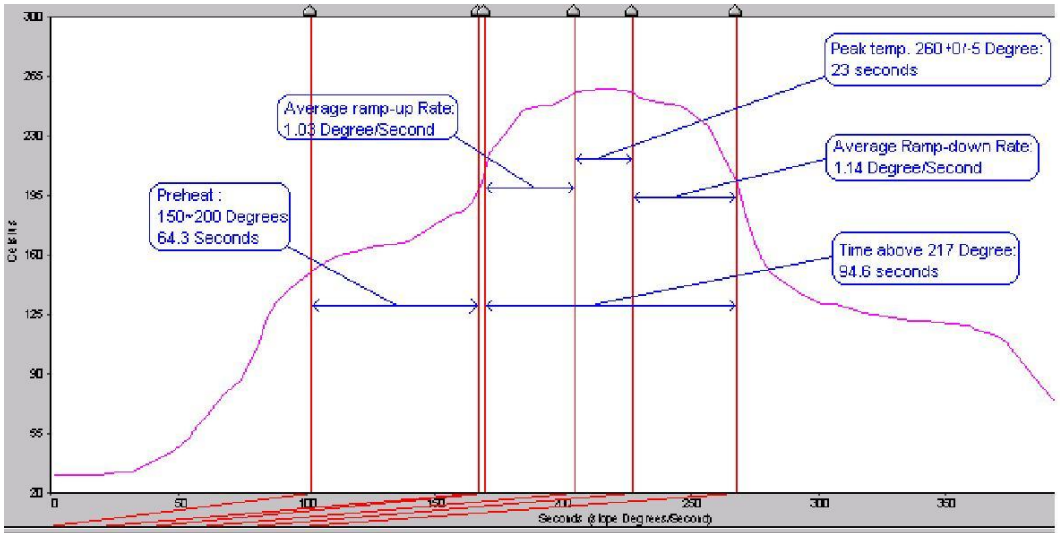
PIN NO.	PIN NAME	DESCRIPTIONS
1	SCL	Serial Clock IN
2	VDD	Power
3	VSS	Ground
4	--	--
5	--	--
6	SDA	Serial Data I/O
7	--	--
8	Rext	External Resistor

- **IPLCC6 2mm x 2mm x 0.63mm**





REFLOW SOLDERING



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