LINEAR SYSTEMS

Twenty-Five Years Of Quality Through Innovation

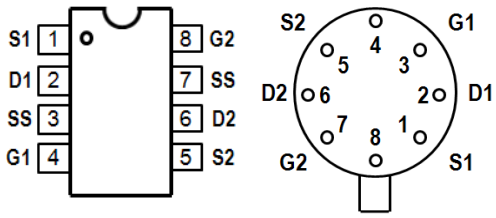
LS5905 LS5906 LS5907 LS5908 LS5909

LOW LEAKAGE LOW DRIFT MONOLITHIC DUAL N-CHANNEL JFET AMPLIFIER

FEATURES	
LOW DRIFT	$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ =5µV/°C max.
ULTRA LOW LEAKAGE	I_G=150fA TYP.
LOW PINCHOFF	V_P=2V TYP.

ABSOLUTE MAXIMUM RATINGS[1] @ 25°C (unless otherwise noted)		
Maximum Temperatures		
Storage Temperature		-55 to +150°C
Operating Junction Temperature		-55 to +150°C
Maximum Voltage and Current for Each Transistor[1]		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10µA
Maximum Power Dissipation		
Device Dissipation @ TA=25ºC - Total		500mW[2]

Case & Body



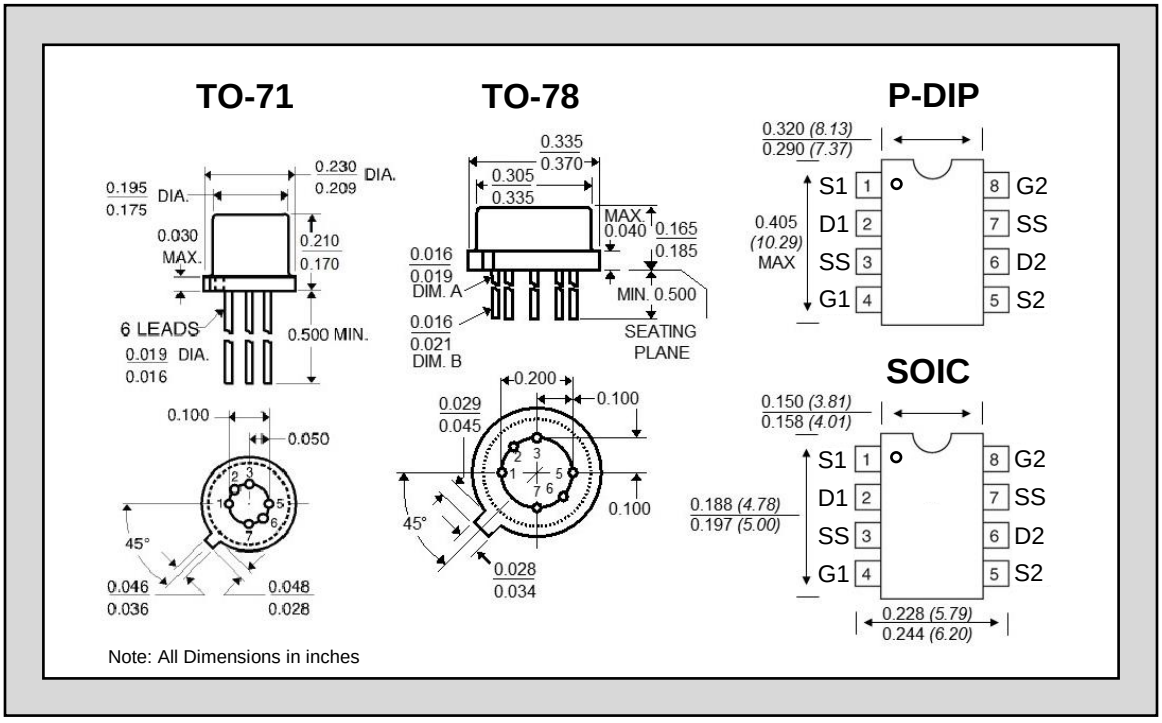
Top View SOIC **Top View TO-78**

ELECTRICAL CHARACTERISTICS @ 25ºC (unless otherwise noted)

SYMBOL	CHARACTERISTIC	LS5906	LS5907	LS5908	LS5909	LS5905	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	Drift vs. Temperature	5	10	20	40	40	µV/ºC	V_{DG} = 10V, I_D=30µA T_A = -55ºC to +125ºC
$\lvert V_{GS1-2}\rvert$ max.	Offset Voltage	5	5	10	15	15	mV	V_{DG} =10V I_D=30µA
$-I_G$ Max	Operating	1	1	1	1	3	pA	
$-I_G$ Max	High Temperature	1	1	1	1	3	nA	T_A=+125 ºC
$-I_{GSS}$ Max	Gate Reverse Current	2	2	2	2	5	pA	V_{DS}=0V V_{GS}=-20V
$-I_{GSS}$ Max	Gate Reverse Current	5	5	5	5	10	nA	T_A=+125 ºC

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	-40	-60	--	V	V_{DS}= 0 I_D= -1µA
BV_{GGO}	Gate-to-Gate Breakdown	±40	--	--	V	I_{GG}= ±1µA I_D= 0 I_S= 0
	TRANSCONDUCTANCE					
G_{fss}	Full Conduction	70	300	500	µS	V_{DG}= 10V V_{GS}= 0 f = 1kHz
G_{fs}	Typical Operation	50	100	200	µS	V_{DG}= 10V I_D= 30µA f = 1kHz
$\lvert G_{fs1}/G_{fs2}$[3]$\rvert$	Transconductance Ratio	--	1	5	%	
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	400	1000	µA	V_{DG}= 10V V_{GS}= 0
$\lvert I_{DSS1}/I_{DSS2}$[3]$\rvert$	Drain Current Ratio	--	2	5	%	
	GATE VOLTAGE					
V_{GS}(off)	Gate-Source Cutoff Voltage	-0.6	-2	-4.5	V	V_{DS}= 10V I_D= 1nA
V_{GS}	Operating Range	--	--	-4	V	V_{DS}= 10V I_D= 30µA
	GATE CURRENT					
I_{GGO}	Gate-to-Gate Leakage	--	±1	--	pA	V_{GG}= 20V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	OUTPUT CONDUCTANCE					
g_{oss}	Full Conduction	--	--	5	µS	V_{DG}= 10V V_{GS}= 0
g_{os}	Operating	--	0.1	--	µS	V_{DG}= 10V I_D= 30µA
$\lvert g_{os1-2} \rvert$	Differential	--	0.01	0.2	µS	
	COMMON MODE REJECTION					
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 10 to 20V I_D=30µA
CMRR	-20 log $\lvert \Delta V_{GS1-2}/\Delta V_{DS} \rvert$	--	90	--	dB	ΔV_{DS}= 5 to 10V I_D=30µA
	NOISE					
NF	Figure	--	--	1	dB	V_{DS}= 10V V_{GS}= 0 R_G=10MΩ f= 100Hz NBW=6Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DS}= 10V I_D= 30µA f= 10Hz NBW=1Hz
	CAPACITANCE					
C_{ISS}	Input	--	--	3	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	V_{DS}= 10V V_{GS}= 0 f= 1MHz
C_{DD}	Drain-to-Drain	--	--	0.1	pF	V_{DG}= 20V I_D= 30µA f= 1MHz



Note: All Dimensions in inches

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor may be impaired.
2. Derate 4mWºC above 25ºC
3. Assume smaller value in the numerator.

Linear Integrated Systems (LIS) is a 25-year-old, third-generation precision semiconductor company providing high-quality discrete components. Expertise brought to LIS is based on processes and products developed at Amelco, Union Carbide, Intersil and Micro Power Systems by company President John H. Hall. Hall, a protégé of Silicon Valley legend Dr. Jean Hoerni, was the director of IC Development at Union Carbide, Co-Founder and Vice President of R&D at Intersil, and Founder/President of Micro Power Systems.