LSI/CSI

LS8292
LS8293

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PRELIMINARY **MICRO-STEPPING MOTOR CONTROLLER** June 2013

FEATURES:

- Controls Bipolar and Unipolar stepper motors
- Step modes: Full, 1/2, 1/4, 1/8, 1/16 and 1/32
- PWM outputs for external H-bridge drivers
- Precision DAC reference for PWM sense comparators
- Fast, Slow and mixed decay modes
- Power saving holding torque for idling motor
- Automatic switching to holding torque with programmable delay when motor idles
- Programmable delay for sense input blanking
- Programmable delay for mixed decay cycles
- Input for Step command
- Input for Direction control
- Input for Reset to HOME
- Input for disabling PWM outputs
- Input/output for external clock or built-in oscillator
- Supply current < 400uA
- Supply voltage 4.5V to 5.5V
- **LS8292** (DIP), **LS8292-S** (SOIC), **LS8292-TS** (TSSOP)
- **LS8293** (DIP), **LS8293-S** (SOIC), **LS8293-TS** (TSSOP)

DESCRIPTION:

LS8292 and **LS8293** are stepper motor controllers with selectable resolutions from Full to 1/32 step. There are four phase drive outputs and two inhibit outputs for controlling 2-phase bipolar or 4-phase unipolar motors. These outputs are designed to drive two external H-bridge drivers for bipolar motor windings or four external transistors for center-tapped unipolar motor windings. These outputs can also be configured to drive discrete external transistors for bipolar motor windings. A lookup table sources the PWM duty cycle digital data for the two motor windings corresponding to the step sequence. Two internal DACs convert the PWM data to analog voltages as percentages of the reference voltage applied at the Vref input. Currents through the motor windings are monitored at the SENSE inputs as voltage drops across fractional-Ohm resistors in series with the H-bridge drivers. Upon turning on a PWM drive, when the voltage at the SENSE input reaches the DAC reference level, the PWM output is switched off for remainder of the cycle. The PWM cycle is fixed at Tpwm = 256/fc, where fc is the clock frequency at the XTLI input. The PWM cycles for the two drives are started simultaneously but terminated separately per individual DAC references.

An input is provided for the holding torque state at lower winding current in the motor idle state. The holding-torque current level is adjusted with a separate reference voltage applied at the Vrefh input. The Vrefh is automatically switched in if the motor idles for a programmable specified delay following a micro-step.

PWM chopping can be applied either to the PHASE or to the INHIBIT outputs. The chopping mode affects the manner in which the winding current decays during a PWM cycle.

There are four selectable decay modes: Fast-decay, Slow-decay, Single-mixed-decay and Dual-mixed-decay.

In the Fast-decay mode the diagonal high side and low side transistors of the H-bridge are both turned off during the PWM off period. This causes the inductive current to be dissipated through the bypass diodes in a direction opposing the motor supply voltage resulting in fast decay.

In the Slow-decay mode the low side transistor of the H-bridge is turned off keeping the high side transistor on during the PWM off period. This causes the inductive current to re-circulate through the high side transistor and diode loop. The current decays slowly because of the low loop voltage. The Slow-decay can be useful for motors that do not store enough energy in the windings leading to an average current too low for any useful torque.

In the Single-mixed-decay mode, slow and fast decays are combined in the following way:

♦ When the motor is idle, slow decay is applied to both windings to guarantee lowest current ripple in a holding state.

♦ When the motor is stepping, if the step requires the current in a winding to decrease, fast decay is applied to the winding for a programmable duration followed by slow decay. If the step requires the current in a winding to increase, slow decay is applied to the winding.

In Dual-mixed-decay mode, mixed decay is applied to both windings for every step with fast decay being followed by slow decay.

One of six stepping modes can be selected by two input pins: Full, 1/2, 1/4, 1/8, 1/16 and 1/32. An internal oscillator generates the system clock and sets the PWM period. The oscillator pin can also be driven by an external clock. Other available inputs are for step command, direction control, resetting to home position, disabling the H-bridge drives, SENSE input blanking delay control and fast to slow switching delay control in the mixed decay modes.

INPUT/OUTPUT DESCRIPTION:

XTLI, XTLO
A crystal connected between these two pins sets the system clock frequency. Alternatively, XTLI pin can be driven by an external clock for providing the system clock. The PWM period Tpwm, is related to the system clock frequency as follows: Tpwm = 256/fc, where,
fc is the system clock frequency applied at the XTLI input.

M0, M1
M0 is a 3-state input amd M1 is a 2-state input; together they select the step mode as follows:

Table 1

M1	M0	Step Mode
0	0	Full Step
1	0	1/2 Step
0	float	1/4 Step
1	float	1/8 Step
0	1	1/16 Step
1	1	1/32 Step

RESET/
When low, RESET/ input clears the step pointer to HOME position per table 4. This input has an internal pull-up resistor.

STEP/
A low pulse at the STEP/ input causes the motor to advance one step forward or reverse. The step size is selected per Table 1.

FWD
When high, the FWD input causes the motor to step in the forward direction per incremental step sequence of Table 4. When low, the motor steps in the reverse direction per decremental step sequence of Table 4.

EN/
When high, EN/ input causes all motor drive outputs to be disabled bringing INH1/, INH2/, PHA, PHB, PHC and PHD low. When ENABLE/ is low, all motor drive outputs are enabled.

HOME/
HOME/ is an open drain output to indicate step0 per Table 4 with an active low.

Vref
Input for the chopper circuit DAC reference voltage. It regulates the peak motor winding current by regulating the PWM duty cycle. The DAC modifies the Vref input voltage for the current sensing comparators at every sequential motor step which can be estimated with the following equations:

$$Vsens1 = | (Vref/7) \times \cos((90/32) \times (n + 16))^\circ |$$

$$Vsens2 = | (Vref/7) \times \sin((90/32) \times (n + 16))^\circ |$$

Where, n is the 1/32 column step number in Table 6. The sense resistors should satisfy the relation: Rs1 = Rs2 = Vref/(7 x Imax) where, Imax is the maximum motor winding current and Rs1 and Rs2 are the fractional-Ohm sense resistors in series with each phase of the H-bridge driver transistors.

Vrefh
Input for the holding torque reference voltage when the holding torque mode is enabled. The holding torque reference voltage should satisfy the relation:
Vrefh = 7 x Rs1 x Imaxh = 7 x Rs2 x Imaxh,
Where, Imaxh is the maximum winding current intended in the holding state and Rs1 and Rs2 are the fractional Ohm sense resistors in series with each phase of the H-bridge driver transistors.

SENSE1, SENSE2
Inputs for motor winding current sense. A fractional-Ohm resistor connected in series with each of the H-bridge drivers produce SENSE1 and SENSE2 voltages. These voltages are compared with the DAC modulated reference voltages for generating the PWM phase or inhibit outputs.

PHA, PHB, PHC, PHD
Phase drive outputs for power stages. In a bipolar motor, PHA and PHB are used for one H-bridge while PHC and PHD are used for the other. In the slow-decay mode the phase outputs are chopped by means of the current sense comparators. In the fast-decay mode the phase outputs are kept enabled while the inhibit outputs are chopped.

INH1/, INH2/
These outputs are active low inhibit controls for motor drive outputs. INH1/ controls driver stage using PHA and PHB outputs while INH2/ controls driver stage using PHC and PHD outputs. In the fast-decay mode inhibit outputs are chopped by means of the current sense comparators. In the slow-decay mode the inhibit outputs are enabled while the phase outputs are chopped.

SYNC/
This open drain output produces a negative-going pulse occurring at the beginning of every PWM cycle which can be use to drive an external slope compensation circuit. Slope compensation may be useful at PWM duty cycle exceeding 50%, particularly in the fast-decay mode.

TBLNK
A resistor-capacitor pair connected to the TBLNK input controls the delay for which the sense input sampling is inhibited at the beginning of each PWM cycle. The delay is given by:

$$Tblnk = 1.2 \times RbCb$$

Where, Rb and Cb are the resistor and the capacitor connected to the TBLNK pin.

THLD
A resistor-capacitor pair connected to this pin produces the holding torque initiation delay following a step command. Upon delay timeout the normal torque reference voltage Vref is switched out from the sense comparators, being replaced with the holding torque reference voltage Vrefh. The holding torque at lower dissipation prevails as long as the motor remains idle. The delay is given by:

$$Thld = 1.4 \times RhCh$$

Where, Rh and Ch are the resistor and the capacitor connected to the THLD pin. If the pin is tied low, holding torque mode is disabled and normal torque prevails in both dynamic and idle motor states.

DCYM, TDCYD, TDCYU

DCYM and TDCYD inputs control the PWM decay modes for the LS8292 as follows:

Table 2

DCYM	TDCYD	Decay Mode
1	0	Fast
1	1	Slow
0	RdCd	Single-Mixed

DCYM, TDCYD and TDCYU inputs control the PWM decay modes for the LS8293 as follows:

Table3

DCYM	TDCYD	TDCYU	Decay Mode
1	0	x	Fast
1	1	x	Slow
0	RdCd	0	Single-Mixed
0	RdCd	RuCu	Dual-Mixed

Fast-Decay. Phase output are enabled while inhibit outputs are chopped in both dynamic and idle motor states.

Slow-Decay. Inhibit output are enabled while phase outputs are chopped in both dynamic and idle motor states.

Single-Mixed-Decay. Following a stepping event, if the step requires the current in a winding to decrease, fast decay is applied to the winding for a programmable duration followed by slow decay. The duration is given by: Tdcyd = 1.2 x RdCd, where Rd and Cd are the resistor and the capacitor connected to the TDCYD pin.

If the step requires the current in a winding to increase, slow decay is applied to the winding. If motor is idle, slow decay is applied to both windings.

Dual-Mixed-Deacy. Following a stepping event fast decay is applied to both windings for programmable durations followed by slow decay. The duration of the fast decay for the winding requiring lower current following a stepping event is given by: Tdcyd = 1.2 x RdCd and the duration of the fast decay for the winding requiring higher current following a stepping event is given by: Tdcyu = 1.2 x RuCu. Ru and Cu are the resistor and the capacitor connected to the TDCYU pin.

If motor is idle, slow decay is applied to both windings.

VDD

Supply voltage positive terminal.

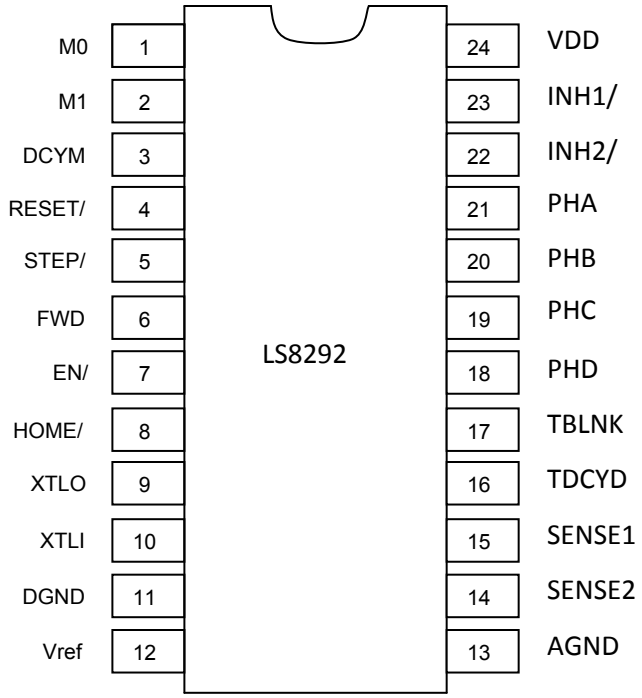
DGND

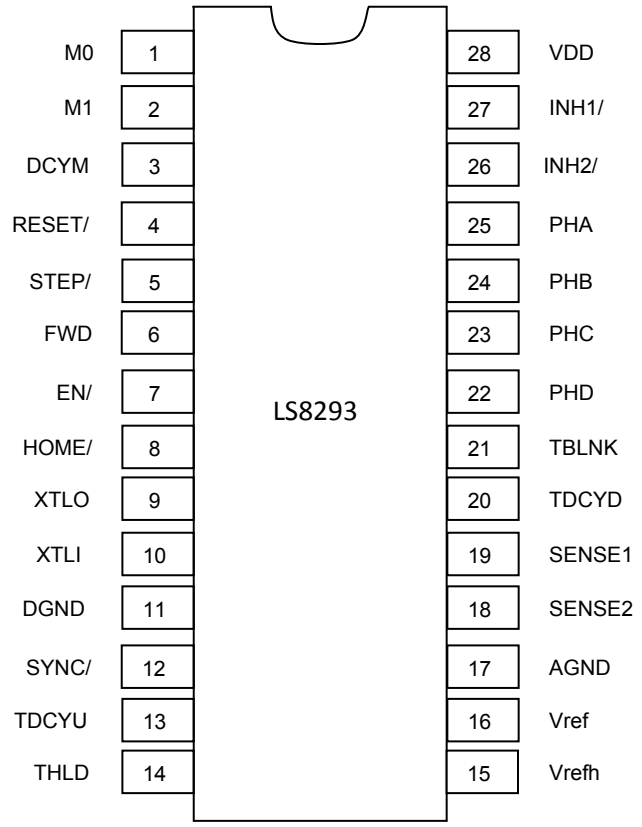
Supply negative terminal for digital ground.

AGND

Analog ground; must be connected together with DGND on the PCB.

PIN ASSIGNMENT
TOP VIEW





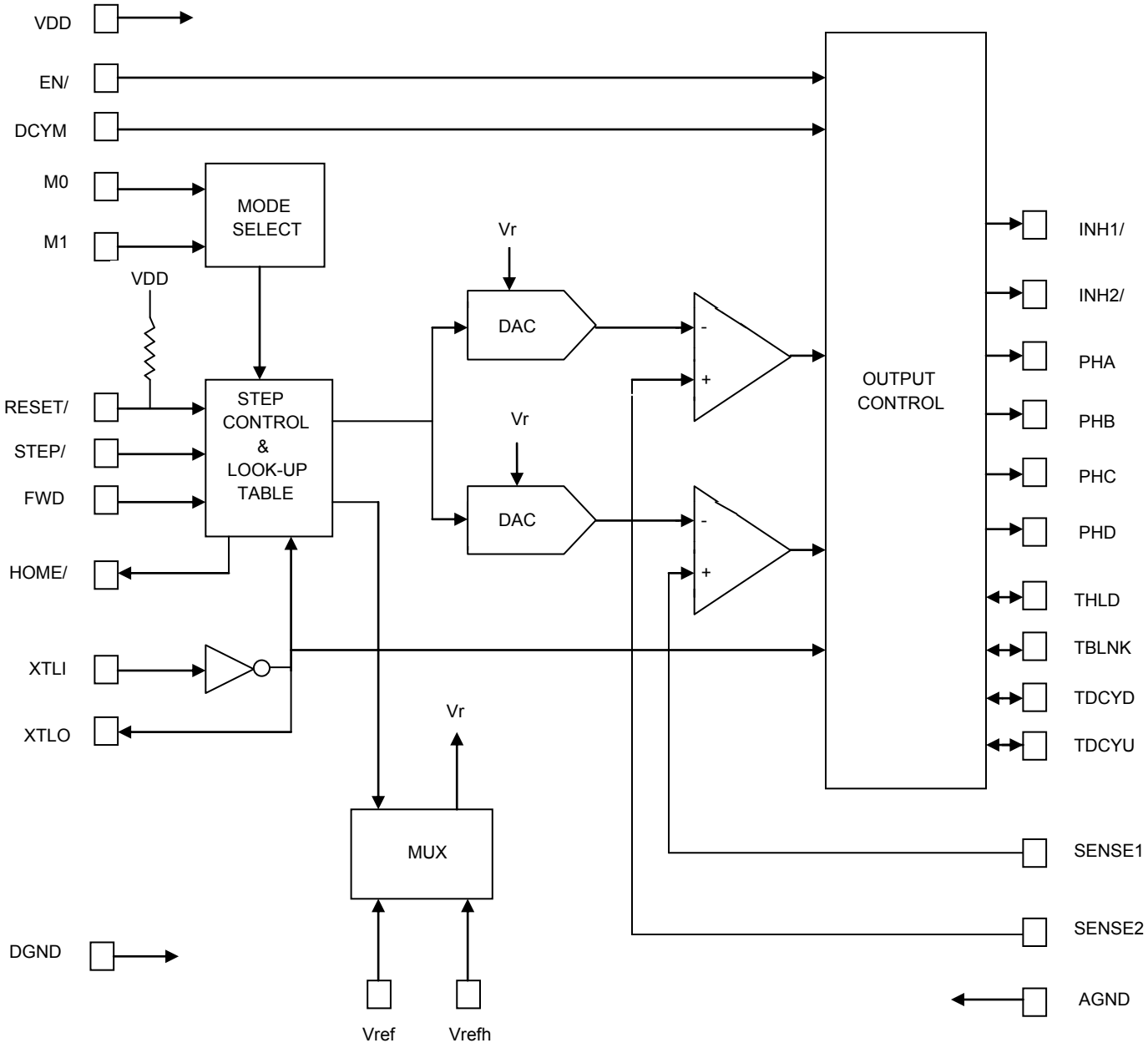


FIG 2. LS8292/LS8293 BLOCK DIAGRAM

TABLE 4			
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage	VDD	+7	V
Input Voltage (all inputs)	Vin	GND – 0.3 to VDD + 0.3	V
Operating Temperature	T_A	-25 to +85	ºC
Storage Temperature	T_{STG}	-65 to +125	ºC

TABLE 5						
ELECTRICAL AND TRANSIENT CHARACTERISTICS (VDD = 5V, T_A = -25 ºC TO +85 ºC)						
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITION**
Supply Voltage	VDD	4.5	5.0	5.5	V	-
Supply Current	IDD	-	-	500	uA	Outputs floating, Inputs high
M0 Input Logic High	V_{MH}	4.0	-	-	V	-
M0 Input Logic Low	V_{ML}	-	-	0.6	V	
Input Voltage Logic High (all other inputs)	V_{IH}	2.0	-	-	V	-
Input Voltage Logic Low (all other inputs)	V_{IL}	-	-	0.8	V	-
Input Current: RESET/ logic high	I_{IRH}	-	-	30	uA	V_{IH} = 2V
Input Current: RESET/ logic low	I_{IRL}	-	-	40	uA	V_{IL} = 0.8V
Input Current: M0 logic high	I_{MH}	-	5	-	uA	V_{IH} = 5V
Input Current: M0 logic low	I_{ML}	-	5	-	uA	V_{IL} = 0V
Input Current: logic high (all other inputs)	I_{IH}	-	-	50	nA	Leakage Current
Input Current: logic low (all other inputs)	I_{IL}	-	-	50	nA	Leakege Current
Output Current: Sink (Phase & Inhibit outputs)	I_{OPIL}	10	-	-	mA	V_{out} = 0.4V
Output Current: Source (Phase & Inhibit outputs)	I_{OPIH}	-5	-	-	mA	V_{out} = 4.6V
Output Current: Sink (SYNC/ output)	I_{OSL}	10	-	-	mA	V_{out} = 0.4V
Output Current: Sink (HOME/ output)	I_{OHL}	10	-	-	mA	V_{out} = 0.4V
Output Current: source (HOME/ output)	I_{OHH}	-5	-	-	mA	V_{out} = 4.6V
Input Reference Voltage (Vref & Vrefh)	Vrf	2.5	-	4.5	V	-
Sense Comparators Offset Voltage	Vos	-	50	200	uV	Vrf = 2V
TDCYD Input Timing Resistpr	R_d	2	-	-	kΩ	-
TDCYU Input Timing Resistor	R_u	2	-	-	kΩ	-
THLD Input Timing Resistor	R_h	4	-	-	kΩ	-
TBLNK Input Timing Resistor	R_b	6	-	-	kΩ	-
XTLI Input Frequency	fc	-	5.0	8.0	MHz	-
FWD Input set-up time for STEP/	tfd	0	0	0	nS	-
STEP/ Input Pulse Width	Tspw	-	8/fc	-	uS	-
RESET/ Input Pulse Width	Trpw	-	8/fc	-	uS	-
SYNC/ Output Pulse Width	Tsypw	-	16/fc	-	uS	-
PWM period	Tpwm	-	255/fc	-	uS	-

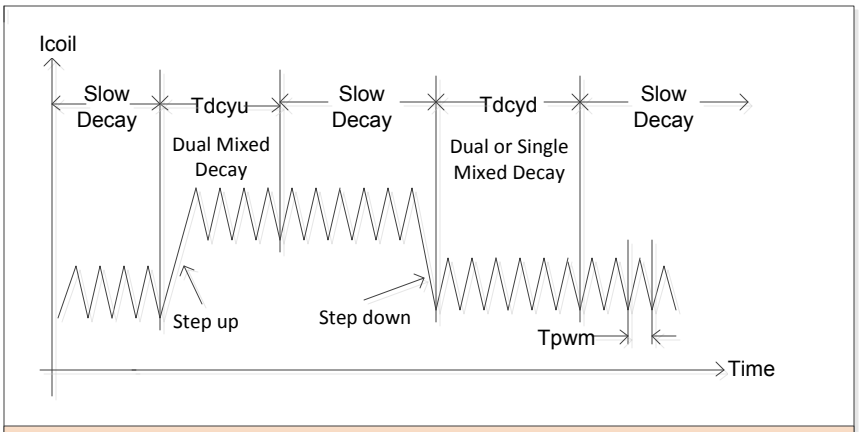
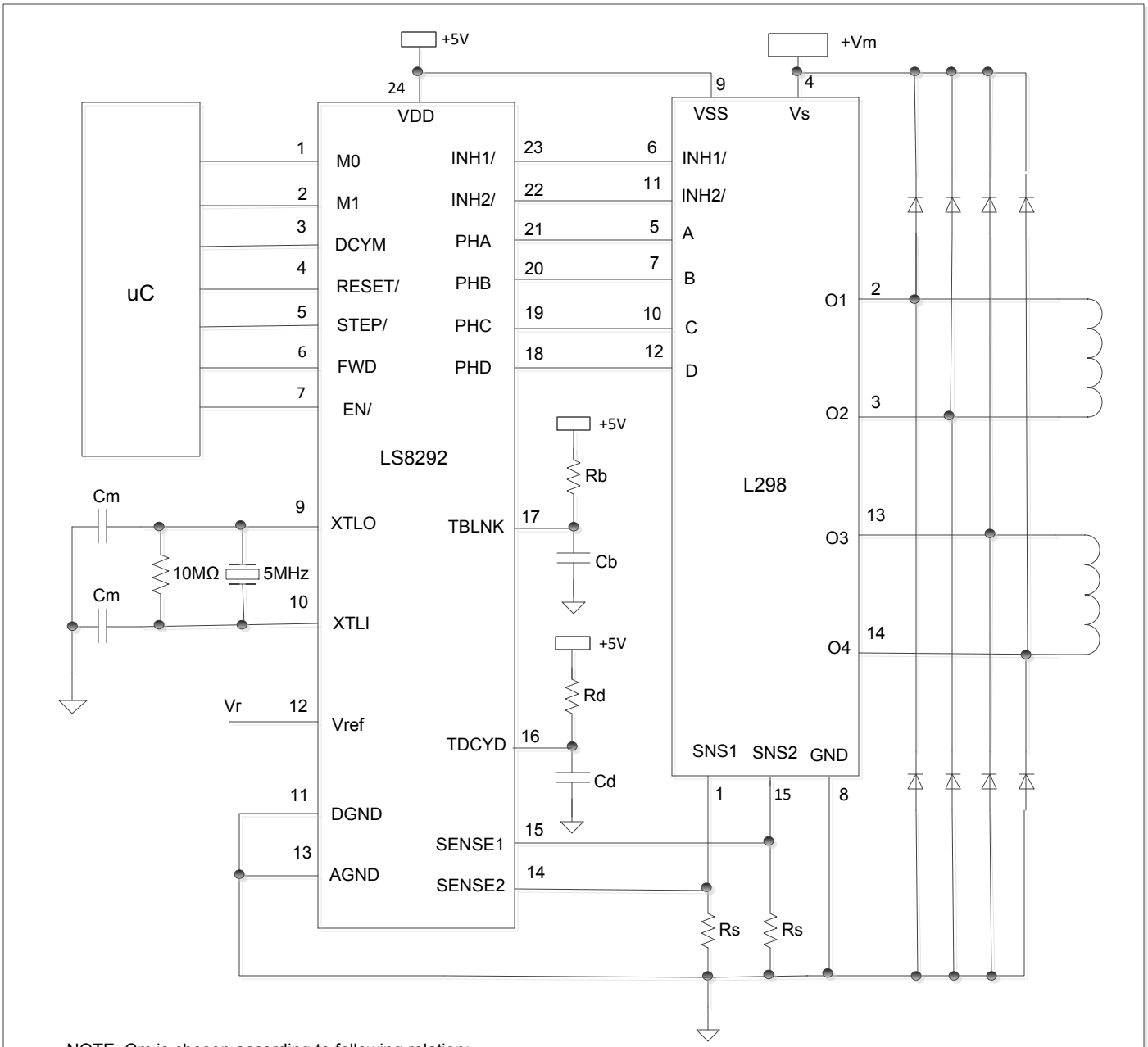
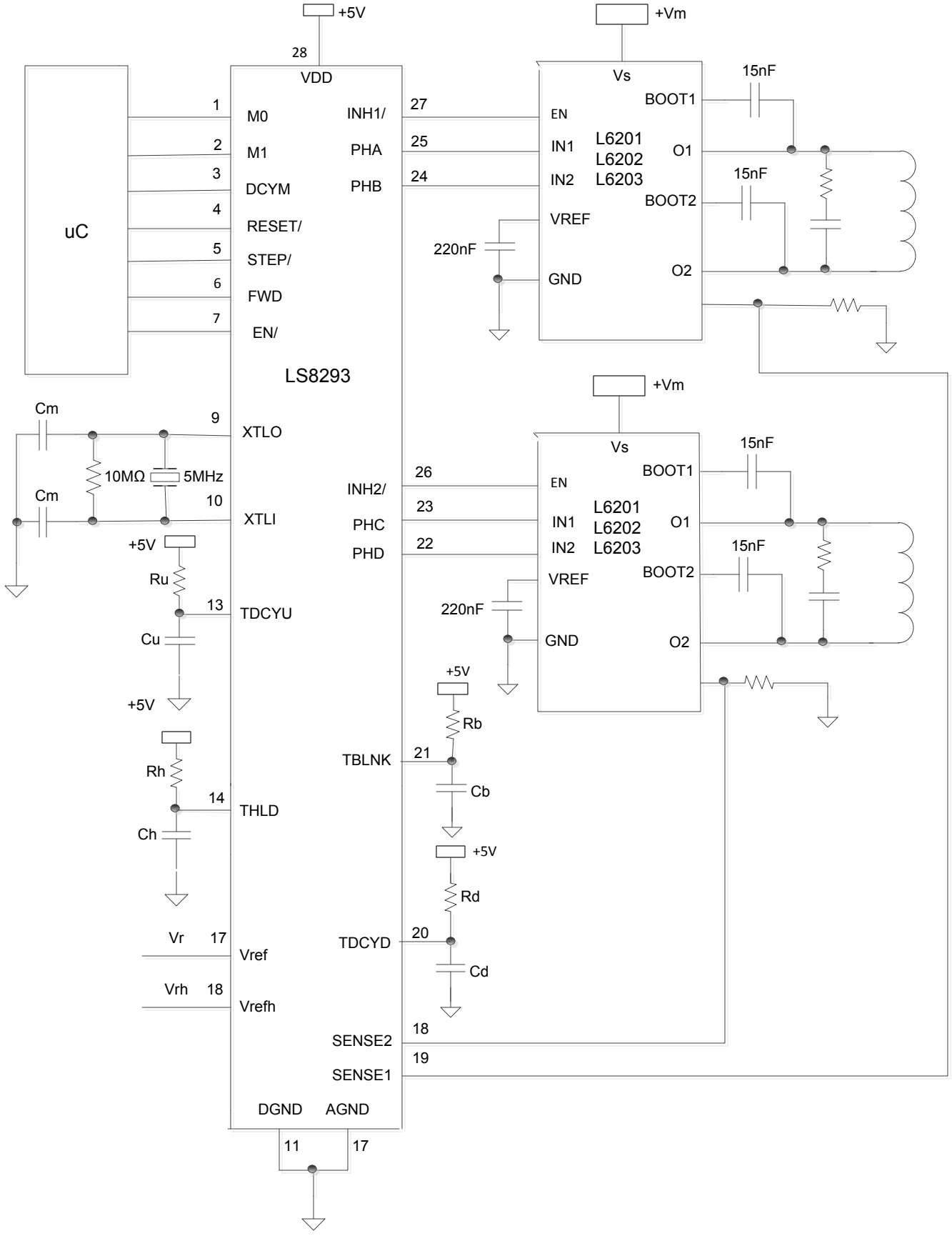


Fig 3. SINGLE AND DUAL MIXED-DECAY MODES



NOTE. Cm is chosen according to following relation:
Cm = 2(Cl – Cp) – 10pF, where Cl = Crystal load capacitance and Cp = parasitic capacitance

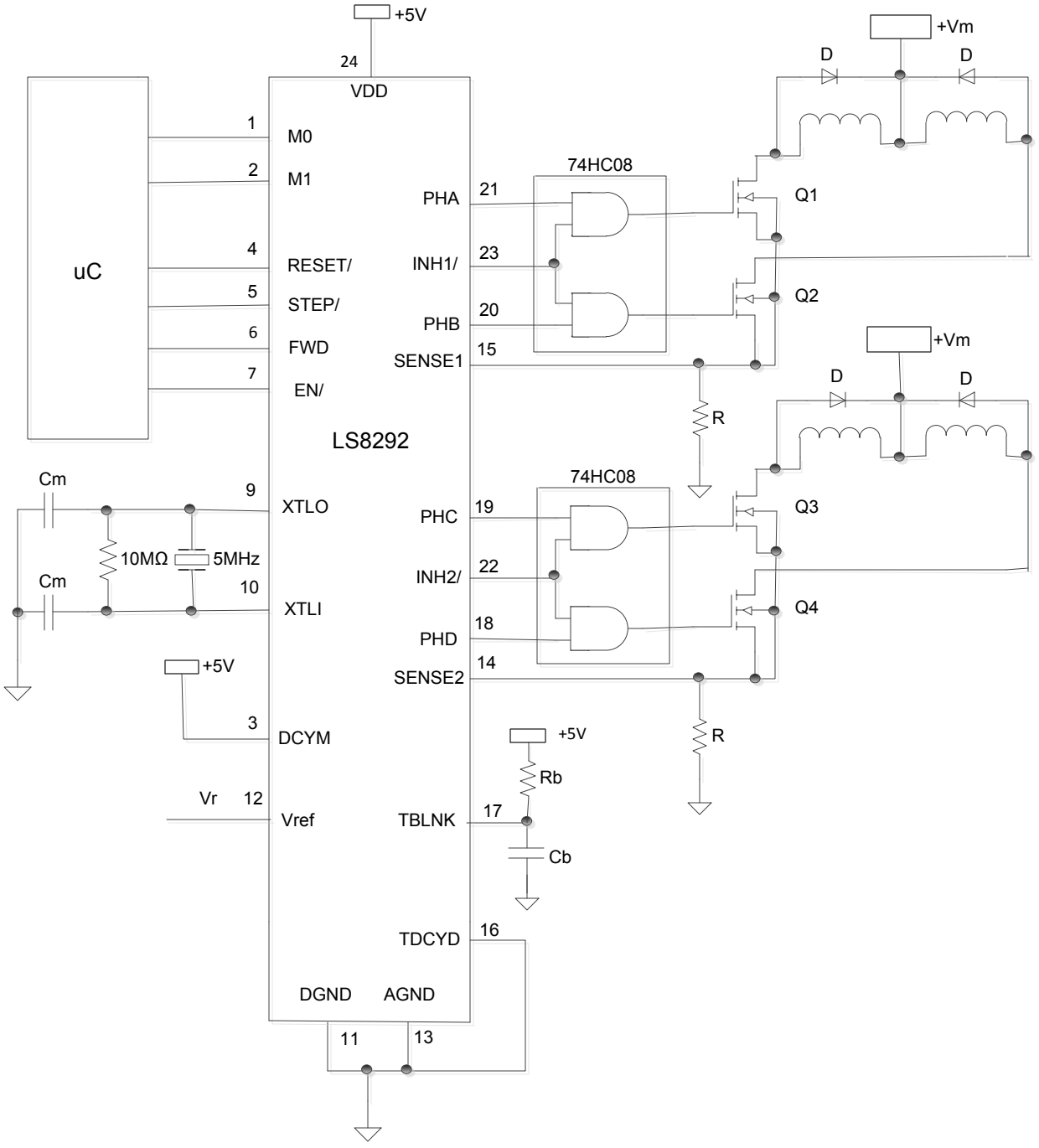
Fig 4. LS8292 DRIVING TWO-PHASE BIPOLAR MOTOR



NOTE1. All functional options have been implemented in this application. If all options are not used, following components can be deleted:
~Rd, Ru, Cd and Cu: if no mixed-decay mode id selected.
~Rh and Ch: if holding torque is not selected. In this case Vrefh pin is tied to GND.

NOTE2. Cm is chosen according to following relation:
Cm = 2(Cl – Cp) – 10pF, where Cl = Crystal load capacitance and Cp = parasitic capacitance

Fig.5. LS8293 APPLICATION FOR TWO PHASE MOTOR USING TWO SEPARATE DRIVERS



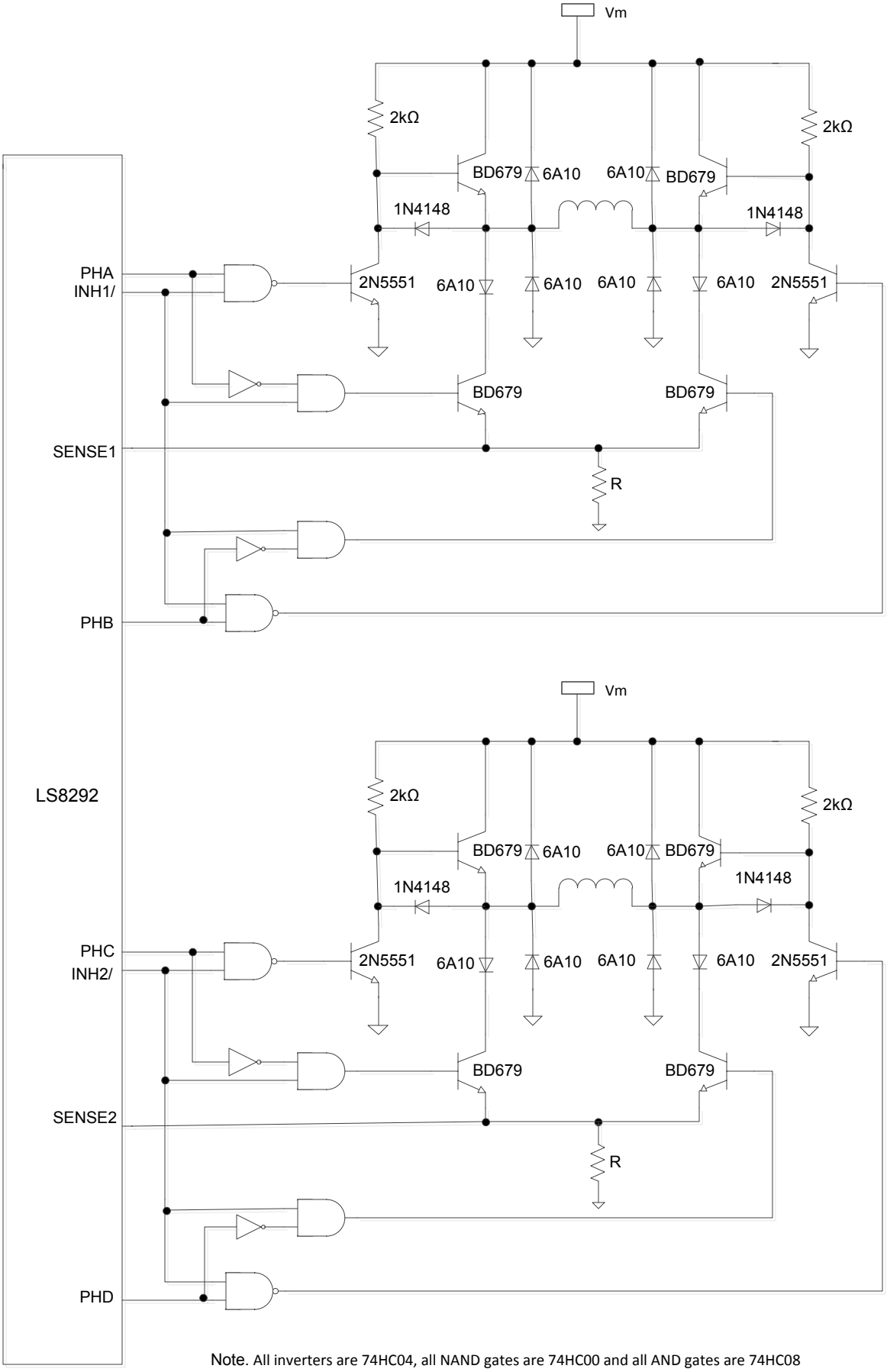
NOTE 1. This design can operate in the Slow-decay mode only.

NOTE 2. Q1, Q2, Q3 and Q4 are power MOSFETS suitable for 5V gate drive. Typical part numbers: IRLZ44N and IRF3708

NOTE 3. For higher pre-drive capability, 74HC08 can be replaced with MIC4468

NOTE 4. Cm is chosen according to following relation:
Cm = 2(Cl – Cp) – 10pF, where Cl = Crystal load capacitance and Cp = parasitic capacitance

Fig 6. TYPICAL APPLICATION FOR FOUR PHASE UNIPOLAR MOTOR USING DISCRETE MOSFETS



Note. All inverters are 74HC04, all NAND gates are 74HC00 and all AND gates are 74HC08

Fig.7. DISCRETE COMPONENT DRIVER

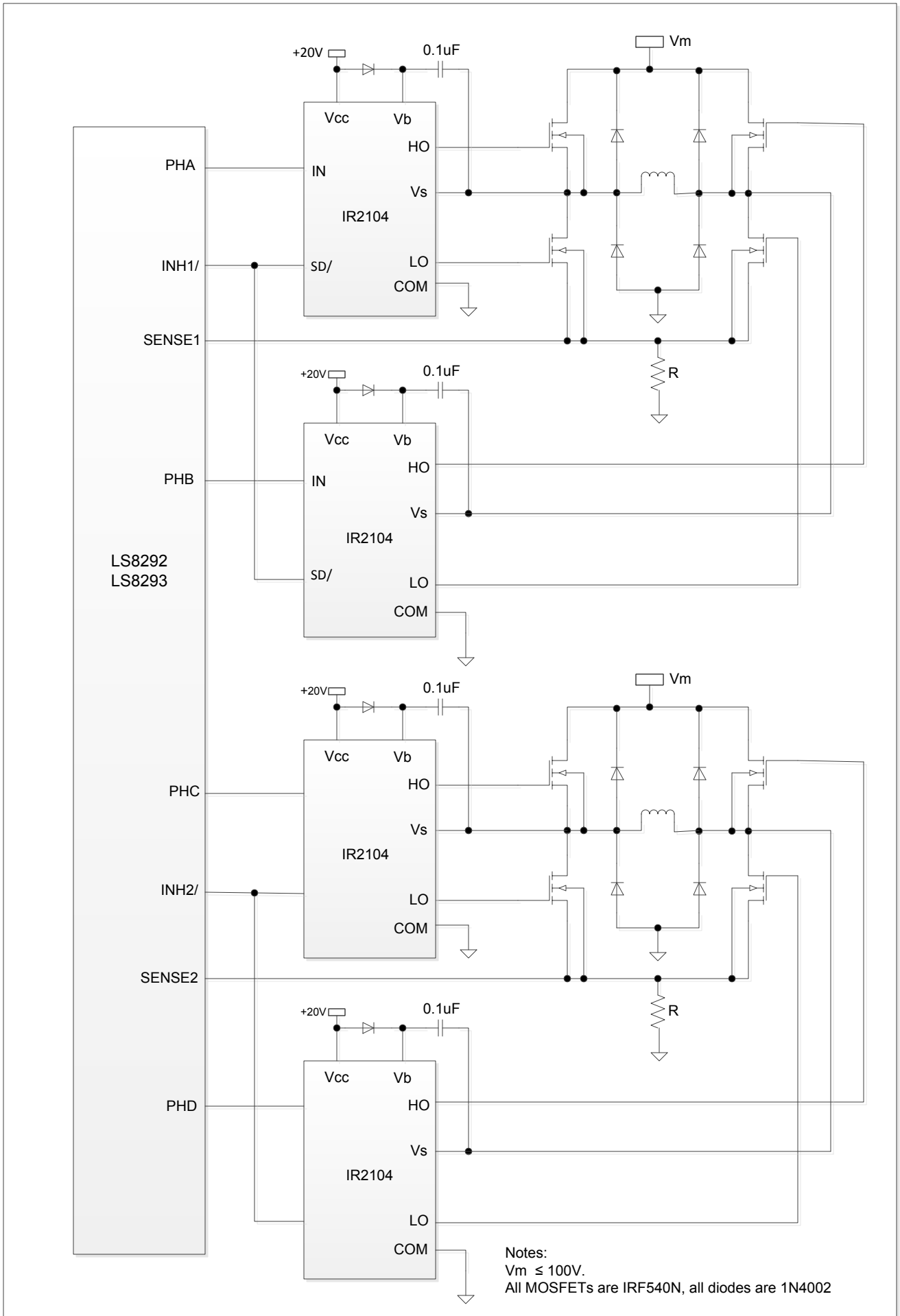


Fig.8. BIPOLAR DRIVER USING N-CHANNEL MOSFETS

Table 6

Step Number						PWM Duty Cycle (%)						
Full	1/2	1/4	1/8	1/16	1/32	INH1/	INH2/	PHA	PHB	PHC	PHD	Step Angle (º)
0	0	0	0	0	0	70.7	70.7	1	0	1	0	HOME
					1	67.2	74.1	1	0	1	0	2.81
				1	2	63.4	77.3	1	0	1	0	5.63
					3	59.6	80.3	1	0	1	0	8.44
			1	2	4	55.6	83.1	1	0	1	0	11.25
					5	51.4	85.8	1	0	1	0	14.06
				3	6	47.1	88.2	1	0	1	0	16.88
					7	42.8	90.4	1	0	1	0	19.69
		1	2	4	8	38.3	92.4	1	0	1	0	22.50
					9	33.7	94.2	1	0	1	0	25.31
				5	10	29.0	95.7	1	0	1	0	28.13
					11	24.3	97.0	1	0	1	0	30.94
			3	6	12	19.5	98.1	1	0	1	0	33.75
					13	14.7	98.9	1	0	1	0	36.56
				7	14	9.8	99.5	1	0	1	0	39.38
					15	4.9	99.9	1	0	1	0	42.19
	1	2	4	8	16	0.0	100	0	1	1	0	45.00
					17	4.9	99.9	0	1	1	0	47.81
				9	18	9.8	99.5	0	1	1	0	50.63
					19	14.7	98.9	0	1	1	0	53.44
			5	10	20	19.5	98.1	0	1	1	0	56.25
					21	24.3	97.0	0	1	1	0	59.06
				11	22	29.0	95.7	0	1	1	0	61.88
					23	33.7	94.2	0	1	1	0	64.69
		3	6	12	24	38.3	92.4	0	1	1	0	67.50
					25	42.8	90.4	0	1	1	0	70.31
				13	26	47.1	88.2	0	1	1	0	73.13
					27	51.4	85.8	0	1	1	0	75.94
			7	14	28	55.6	83.1	0	1	1	0	78.75
					29	59.6	80.3	0	1	1	0	81.56
				15	30	63.4	77.3	0	1	1	0	84.38
					31	67.2	74.1	0	1	1	0	87.19
1	2	4	8	16	32	70.7	70.7	0	1	1	0	90.00
					33	74.1	67.2	0	1	1	0	92.81
				17	34	77.3	63.4	0	1	1	0	95.63
					35	80.3	59.6	0	1	1	0	98.44
			9	18	36	83.1	55.6	0	1	1	0	101.25
					37	85.8	51.4	0	1	1	0	104.06
				19	38	88.2	47.1	0	1	1	0	106.88
					39	90.4	42.8	0	1	1	0	109.69
		5	10	20	40	92.4	38.3	0	1	1	0	112.50
					41	94.2	33.7	0	1	1	0	115.31
				21	42	95.7	29.0	0	1	1	0	118.13
					43	97.0	24.3	0	1	1	0	120.94
			11	22	44	98.1	19.5	0	1	1	0	123.75
					45	98.9	14.7	0	1	1	0	126.56
				23	46	99.5	9.8	0	1	1	0	129.38
					47	99.9	4.9	0	1	1	0	132.19
	3	6	12	24	48	100	0.0	0	1	0	1	135.00
					49	99.9	4.9	0	1	0	1	137.81
				25	50	99.5	9.8	0	1	0	1	140.63
					51	98.9	14.7	0	1	0	1	143.44
			13	26	52	98.1	19.5	0	1	0	1	146.25
					53	97.0	24.4	0	1	0	1	149.06
				27	54	95.7	29.0	0	1	0	1	151.88
					55	94.2	33.7	0	1	0	1	154.69
		7	14	28	56	92.4	38.3	0	1	0	1	157.50
					57	90.4	42.8	0	1	0	1	160.31
				29	58	88.2	47.1	0	1	0	1	163.13

Continued on next page

Step Number						PWM Duty Cycle (%)						
Full	1/2	1/4	1/8	1/16	1/32	INH1/	INH2/	PHA	PHB	PHC	PHD	Step Angle (º)
					59	85.8	51.4	0	1	0	1	165.94
			15	30	60	83.1	55.6	0	1	0	1	168.75
					61	80.3	59.6	0	1	0	1	171.56
				31	62	77.3	63.4	0	1	0	1	174.38
					63	74.1	67.2	0	1	0	1	177.19
2	4	8	16	32	64	70.7	70.7	0	1	0	1	180.00
					65	67.2	74.1	0	1	0	1	182.81
				33	66	63.4	77.3	0	1	0	1	185.63
					67	59.6	80.3	0	1	0	1	188.44
			17	34	68	55.6	83.1	0	1	0	1	191.25
					69	51.4	85.8	0	1	0	1	194.06
				35	70	47.1	88.2	0	1	0	1	196.88
					71	42.8	90.4	0	1	0	1	199.69
		9	18	36	72	38.3	92.4	0	1	0	1	202.50
					73	33.7	94.2	0	1	0	1	205.31
				37	74	29.0	95.7	0	1	0	1	208.13
					75	24.3	97.0	0	1	0	1	210.94
			19	38	76	19.5	98.1	0	1	0	1	213.75
					77	14.7	98.9	0	1	0	1	216.56
				39	78	9.8	99.5	0	1	0	1	219.38
					79	4.9	99.9	0	1	0	1	222.19
	5	10	20	40	80	0.0	100	1	0	0	1	225.00
					81	4.9	99.9	1	0	0	1	227.81
				41	82	9.8	99.5	1	0	0	1	230.63
					83	14.7	98.9	1	0	0	1	233.44
			21	42	84	19.5	98.1	1	0	0	1	236.25
					85	24.4	97.0	1	0	0	1	239.06
				43	86	29.0	95.7	1	0	0	1	241.88
					87	33.7	94.2	1	0	0	1	244.69
		11	22	44	88	38.3	92.4	1	0	0	1	247.50
					89	42.8	90.4	1	0	0	1	250.31
				45	90	47.1	88.2	1	0	0	1	253.13
					91	51.4	85.8	1	0	0	1	255.94
			23	46	92	55.6	83.1	1	0	0	1	258.75
					93	59.6	80.3	1	0	0	1	261.56
				47	94	63.4	77.3	1	0	0	1	264.38
					95	67.2	74.1	1	0	0	1	267.19
3	6	12	24	48	96	70.7	70.7	1	0	0	1	270.00
					97	74.1	67.2	1	0	0	1	272.81
				49	98	77.3	63.4	1	0	0	1	275.63
					99	80.3	59.6	1	0	0	1	278.44
			25	50	100	83.1	55.6	1	0	0	1	281.25
					101	85.8	51.4	1	0	0	1	284.06
				51	102	88.2	47.1	1	0	0	1	286.88
					103	90.4	42.8	1	0	0	1	289.69
		13	26	52	104	92.4	38.3	1	0	0	1	292.50
					105	94.2	33.7	1	0	0	1	295.31
				53	106	95.7	29.0	1	0	0	1	298.13
					107	97.0	24.3	1	0	0	1	300.95
			27	54	108	98.1	19.5	1	0	0	1	303.75
					109	98.9	14.7	1	0	0	1	306.56
				55	110	99.5	9.8	1	0	0	1	309.38
					111	99.9	4.9	1	0	0	1	312.19
	7	14	28	56	112	100	0.0	1	0	1	0	315.00
					113	99.9	4.9	1	0	1	0	317.81
				57	114	99.5	9.8	1	0	1	0	320.63
					115	98.9	14.7	1	0	1	0	323.44
			29	58	116	98.1	19.5	1	0	1	0	326.25

Continued on next page

Step Number						PWM Duty Cycle (%)						
Full	1/2	1/4	1/8	1/16	1/32	INH1/	INH2/	PHA	PHB	PHC	PHD	Step Angle (º)
					117	97.0	24.4	1	0	1	0	329.06
				59	118	95.7	29.0	1	0	1	0	331.88
					119	94.2	33.7	1	0	1	0	334.69
		15	30	60	120	92.4	38.3	1	0	1	0	337.50
					121	90.4	42.8	0	1	0	1	340.31
				61	122	88.2	47.1	0	1	0	1	343.13
					123	85.8	51.4	0	1	0	1	345.95
			31	62	124	83.1	55.6	0	1	0	1	348.75
					125	80.3	59.6	0	1	0	1	351.56
				63	126	77.3	63.4	0	1	0	1	354.38
					127	74.1	67.2	0	1	0	1	357.19
0	0	0	0	0	0	70.7	70.7	0	1	0	1	HOME

NOTE:
In Table4 the PWM duty cycles are indicated for Fast Decay mode which causes INH1/ and INH2/ outputs to be chopped.
In Slow Decay mode INH1/ and INH2/ outputs remain high while PHA, PHB, PHC and PHD outputs are chopped.