

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS831 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS831 features a 25-mV offset and 10- μ V/ $^{\circ}$ C drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS831 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

ULTRA LOW DRIFT	$ V_{GS1-2}/T \leq 10 \mu V/^{\circ}C$
ULTRA LOW LEAKAGE	$I_G = 80 fA$ TYP.
LOW NOISE	$e_n = 70 nV/\sqrt{Hz}$ TYP.
LOW CAPACITANCE	$C_{ISS} = 3 pF$ MAX.

ABSOLUTE MAXIMUM RATINGS @ 25 $^{\circ}$ C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65 $^{\circ}$ C to +150 $^{\circ}$ C
Operating Junction Temperature	+150 $^{\circ}$ C

Maximum Voltage and Current for Each Transistor – Note 1

-V _{GSS}	Gate Voltage to Drain or Source	40V
-V _{DSO}	Drain to Source Voltage	40V
-I _{G(f)}	Gate Forward Current	10mA
-I _G	Gate Reverse Current	10 μ A

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	400mW @ +125 $^{\circ}$ C
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MATCHING CHARACTERISTICS @ 25 $^{\circ}$ C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	DRIFT VS. TEMPERATURE	10	$\mu V/^{\circ}C$	V _{DG} =10V, I _D =30 μ A T _A = -55 $^{\circ}$ C to +125 $^{\circ}$ C
$ V_{GS1-2} $ max.	OFFSET VOLTAGE	25	mV	V _{DG} =10V, I _D =30 μ A

ELECTRICAL CHARACTERISTICS @ 25 $^{\circ}$ C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	40	60	--	V	V _{DS} = 0 I _D =1nA
BV _{GGO}	Gate-To-Gate Breakdown	40	--	--	V	I _G = 1nA I _D = 0 I _S = 0
TRANSCONDUCTANCE						
Y _{FSS}	Full Conduction	70	300	500	μ mho	V _{DG} = 10V V _{GS} = 0V f = 1kHz
Y _{FS}	Typical Operation	50	100	200	μ mho	V _{DG} = 10V I _D = 30 μ A f = 1kHz
Y _{FS1-2} /Y _{FS}	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I _{DSS}	Full Conduction	0.5	--	10	mA	V _{DG} = 10V V _{GS} = 0V
I _{DSS1-2} /I _{DSS}	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
V _{GS(off)} or V _p	Pinchoff voltage	0.6	2	4.5	V	V _{DS} = 10V I _D = 1nA
V _{GS(on)}	Operating Range	--	--	4	V	V _{DS} =10V I _D =30 μ A
GATE CURRENT						
-I _G max.	Operating	--	--	0.1	pA	V _{DG} = 10V I _D = 30 μ A
-I _G max.	High Temperature	--	--	0.1	nA	T _A = +125 $^{\circ}$ C
-I _{GSS} max.	At Full Conduction	--	--	0.2	pA	V _{DS} =0
-I _{GSS} max.	High Temperature	5	5	0.5	nA	V _{GS} = 0V, V _{GS} = -20V, T _A = +125 $^{\circ}$ C
I _{GGO}	Gate-to-Gate Leakage	--	1	--	pA	V _{GG} = 20V
OUTPUT CONDUCTANCE						
Y _{OSS}	Full Conduction	--	--	5	μ mho	V _{DG} = 10V V _{GS} = 0V
Y _{OS}	Operating	--	--	0.5	μ mho	V _{DG} = 10V I _D = 30 μ A
COMMON MODE REJECTION						
CMR	-20 log V _{GS1-2} /V _{DS}	--	90	--	dB	$\Delta V_{DS} = 10$ to 20V I _D =30 μ A
	-20 log V _{GS1-2} /V _{DS}	--	90	--	dB	$\Delta V_{DS} = 5$ to 10V I _D =30 μ A
NOISE						
NF	Figure	--	--	1	dB	V _{DS} = 10V V _{GS} = 0V R _G = 10M Ω f = 100Hz NBW= 6Hz
e _n	Voltage	--	20	70	nV/ $\sqrt{Hz}$	V _{DS} =10V I _D =30 μ A f=10Hz NBW=1Hz
CAPACITANCE						
C _{ISS}	Input	--	--	3	pF	V _{DS} = 10V, V _{GS} = 0V, f= 1MHz
C _{RSS}	Reverse Transfer	--	--	1.5	pF	V _{DS} = 10V, V _{GS} = 0V, f= 1MHz
C _{DD}	Drain-to-Drain	--	--	0.1	pF	V _{DS} = 10V, I _D =30 μ A

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS831 / LS831 in PDIP & SOIC
LS831 / LS831 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP & SOIC (Top View)

