SAMSUNG TFT-LCD

MODEL: LSC550HQ05-G

The Information described in this specification is for the first draft and can be changed without prior notice

Samsung Display Co., LTD

General Description

Description

This model uses a liquid crystal display (LCD) of amorphous silicon TFT as switching components. This model is composed of a TFT LCD panel, a driver circuit, and an ass'y KIT of source PBA. This 32.0" model has a resolution of a 1366 x 768 and can display up to 16.7 million colors with the wide viewing angle of 89° or a higher degree in all directions. This panel is designed to support applications by providing a excellent performance function of the flat panel display such as home-alone multimedia TFT-LCD TV and a high definition TV.

General Information

Features

- RoHS compliance (Pb-free)
- High contrast ratio & aperture ratio with the wide color gamut
- SPVA(Super patterned vertical align) mode
- Wide viewing angle (±178°)
- High speed response
- FHD resolution (16:9)
- Low power consumption
- DE (Data enable) mode
- The interface (2pixel/clock) of 2ch LVDS (Low voltage differential signaling)

Items	Specification	Unit	Note
Active Display Area	1209.6(H) x 680.4(V)	㎜	
Switching Components	a-Si TFT Active matrix		
Display Colors	1.07Billion (10bit Dithering)	color	
Number of Pixels	1,920 × 1,080	pixel	16 : 9
Pixel Arrangement	RGB Horizontal Stripe		
Display Mode	Normally Black		
Pixel Pitch	0.210(H) X 0.630(W)		
Hardness	S-POL. A/G(Haze: 2%)		

1. Absolute Maximum Ratings

If the figures on measuring instruments exceed maximum ratings, it can cause the malfunction or the unrecoverable damage on the device.

Item	Symbol	Min.	Max.	Unit	Note
Power supply voltage	V_{DD}	10.8	13.2	V	(1)
Temperature for storage (Temperature of glass surface)	T_{STG}	5	40	℃	(2),(4)
Operating temperature	T_{OPR}	0	50	℃	(2),(5)
Humidity for storage	H_{STG}	35	75	%RH	(2),(4)
Operating humidity	H_{STG}	20	90	%RG	(2),(5)
Endurance on static electricity			150	V	(3)

Note (1) The power supply voltage at Ta= 25 ± 2 °C

(2) Temperature and the range of relative humidity are shown in the figure below.

a. 90 % RH Max. (Ta ≤ 39 °C)

b. The relative humidity is 90% or less. (Ta > 39 °C)

c. No condensation

(3) Keep the static electricity under 150V in Polarizer attaching process.

(4) Operating condition with source PCB

(5) Storage temperature condition including glass

(6) Condition without packing. (Unpacking condition)

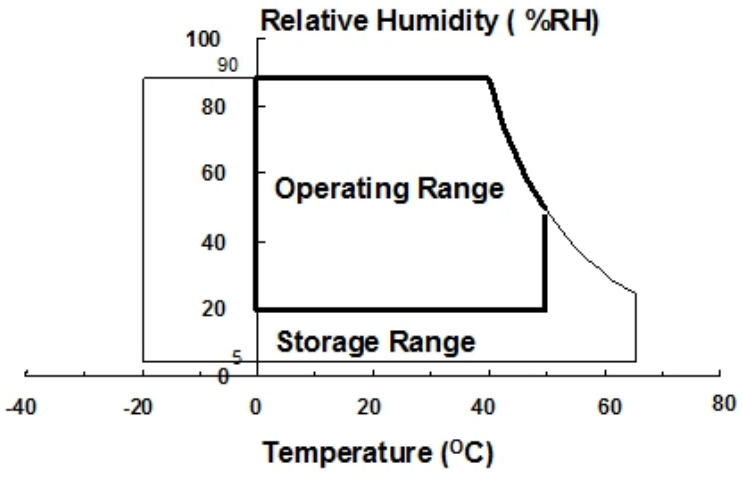


Fig. Range for temperature and relative humidity

2. Optical characteristics

The optical characteristics should be measured in the dark room or the space surrounded by the similar setting.
Measuring equipment : TOPCON RD-80S, TOPCON SR-3 ,ELDIM EZ-Contrast
(Ta = 25 ± 2°C, VDD=12.0V, fv=60Hz, f_{DCLK}=78MHz, Light source: D65 Standard light)

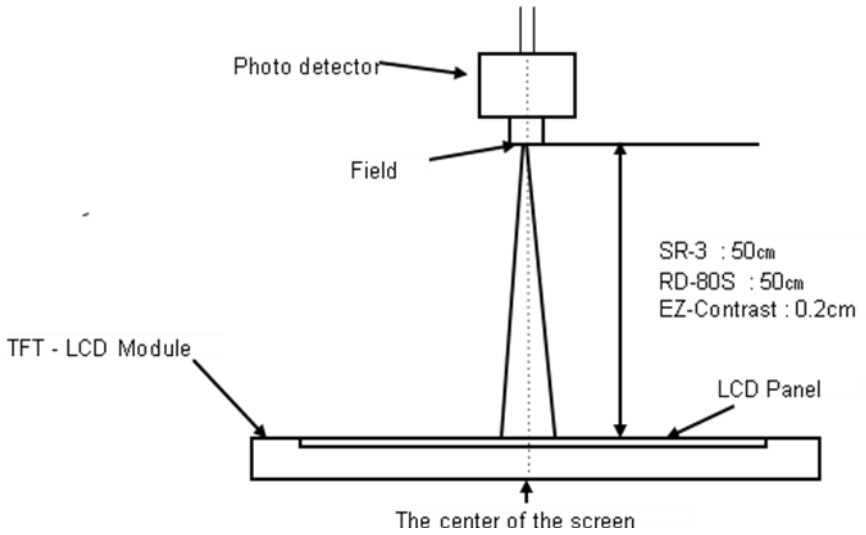
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast ratio (At the center of screen)		C/R		3000	4000	-		(1) SR-3
Luminance of white (At the center of screen)		Y_L	Normal qL,R=0 qU,D=0 Viewing Angle	410	450	-	cd/m^2	(4) SR-3
Chromaticity (CIE 1931)	Red	Rx		TYP. -0.03	0.660	TYP. +0.03		(5),(6) SR-3
		Ry			0.327			
	Green	Gx			0.280			
		Gy			0.580			
	Blue	Bx			0.132			
		By			0.129			
	White	Wx			0292			
		Wy			0.363			
Color gamut		-		62	65	-	%	(5) SR-3
Color		-		5000	7000	9000	K	
Viewing Angle	Hor.	q_L	C/R≥10	75	89	-	Degree	(6) SR-3 EZ-Contrast
		q_R		75	89	-		
	Ver.	q_U		75	89	-		
		q_D		75	89	-		
Brightness uniformity (9 Points)		B_{uni}				25	%	(2) SR-3
Gamma				1.9	2.2	2.5		(8) SR3
transmissivity		T		5.8	6.3		%	(7) D65/SR3

Notice

(a) Setup for test equipment
The measurement should be executed in a stable, windless, and dark room for 40min and 60min after operating the panel at the given temperature for stabilization of the standard light. (SDC uses the standard luminance of the D65 media).
This measurement should be measured at the center of screen.
The environment condition: Ta = 25 ± 2 °C

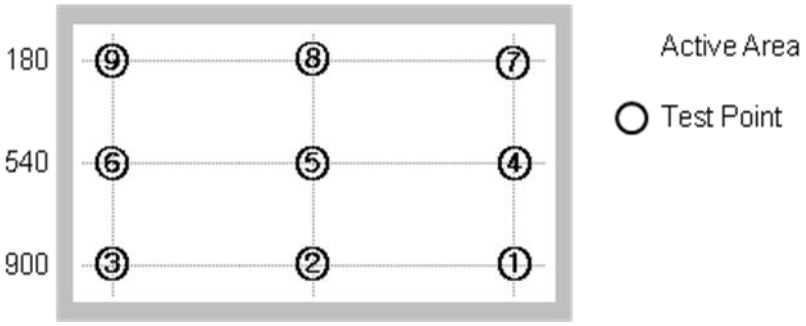
(b) D65 media has the general light source.
The temperature of color is 6487K. The coordinate of color is Wx 0.313, Wy 0.329
The luminance of this product is 7217cd/㎡.

Photo detector	Field
SR-3	2°/1°
RD-80S	1°



(c) The CIE positions D65 as the standard daylight illuminant:
[D65] is intended to represent average daylight and has a correlated color temperature of approximately 6487 K. CIE standard illuminant D65 should be used in all colorimetric calculations requiring representative daylight, unless there are specific reasons for using a different illuminant.

- Definition of the test point



Note (1) Definition of contrast ratio (C/R)
: The ratio of gray max (Gmax) & gray min (Gmin) at the center point ⑤ of the panel
The measurement goes in D65 Standard light source

$$C/R = \frac{G\max}{G\min}$$

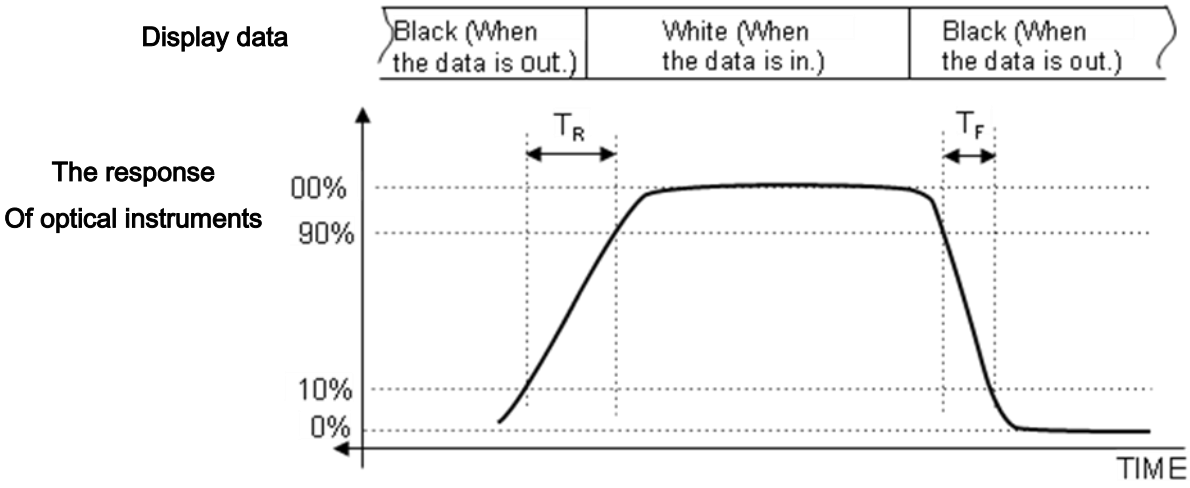
Gmax : The luminance with all white pixels
Gmin : The luminance with all black pixels

Note (2) Definition of the brightness uniformity of 9 points (Test pattern : The full white)
The measurement shall be executed with the standard light source of D65 .

$$Buni = 100 * \frac{(B\max - B\min)}{B\max}$$

Bmax : The maximum brightness
Bmin : The minimum brightness

Note (3) Definition of the response time : Sum of Tr, Tf

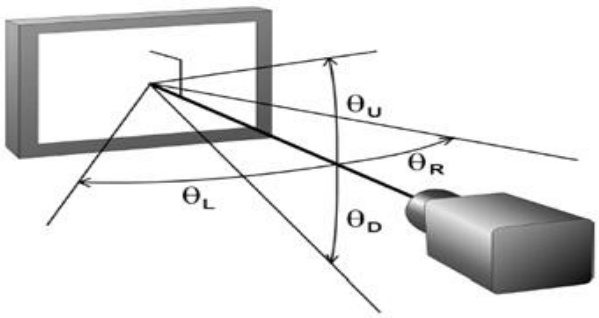


※ G-to-G : Average response time between whole gray scale to whole gray scale.
The response time is the value that was measured after it was operated in Samsung's standard BLU for one hour.(at room temperature)

Note (4) The definition of luminance of white: The luminance of white at the center point ⑤
The measurement shall be executed with the standard light source of D65.

Note (5) The definition of chromaticity (CIE 1931)
The color coordinate of red, green, blue and white at the center point ⑤
The measurement shall be executed with the standard light source of D65.

Note (6) Definition of viewing angle
: The range of viewing angle (C/R ≥10)
The measurement shall be executed with the standard light source of D65.



Note (7) Definition of transmissivity
The measurement shall be executed with the standard light source of D65.

Note (8) Definition of Gamma

$$Gamma = \log(X_{lum}/100)/\log(Y/100)$$

$$X_{lum} = (Z - B_{\min})/(B_{\max} - B_{\min}) \times 100$$

Y: Measurement Level / Z: Measurement Brightness

B_{max}: Maximum Brightness / B_{min}: Minimum Brightness

3. Electrical characteristics

3.1 TFT LCD Module

The connector for the display data & timing signal should be connected.

Ta = 25°C ± 2 °C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of power supply		V_{DD}	10.8	12.0	13.2	V	(1)
Current of power supply	(a) Black	I_{DD}	-	650	800	mA	(2),(3)
	(b) White		-	750	950	mA	
	(c) Sub V-Stripe		-	1300	1700	mA	
Vsync frequency		f_V	48	60	62.5	Hz	
Hsync frequency		f_H	60	67.5	70	kHz	
Main frequency		Fdclk	130	148.5	152.5	MHz	
Rush current		I_{RUSH}	-	-	4	A	(4)

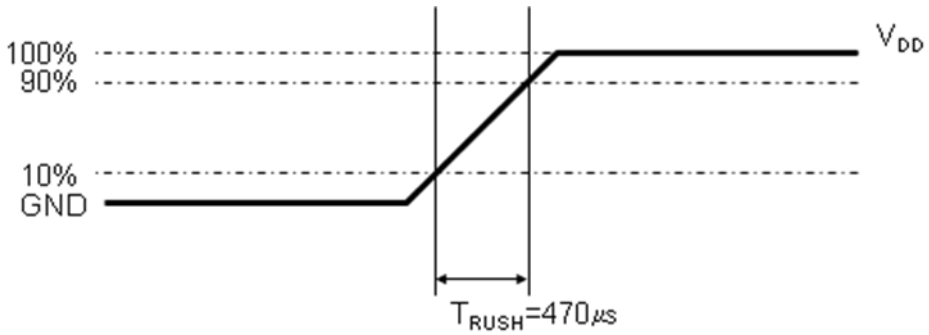
Note (1) The ripple voltage should be controlled fewer than 10% of V_{DD} (Typ.) voltage.

(2) fV=60Hz, fDCLK =148.5MHz, V_{DD} = 12.0V, DC Current.

(3) Power dissipation check pattern (LCD Module only)

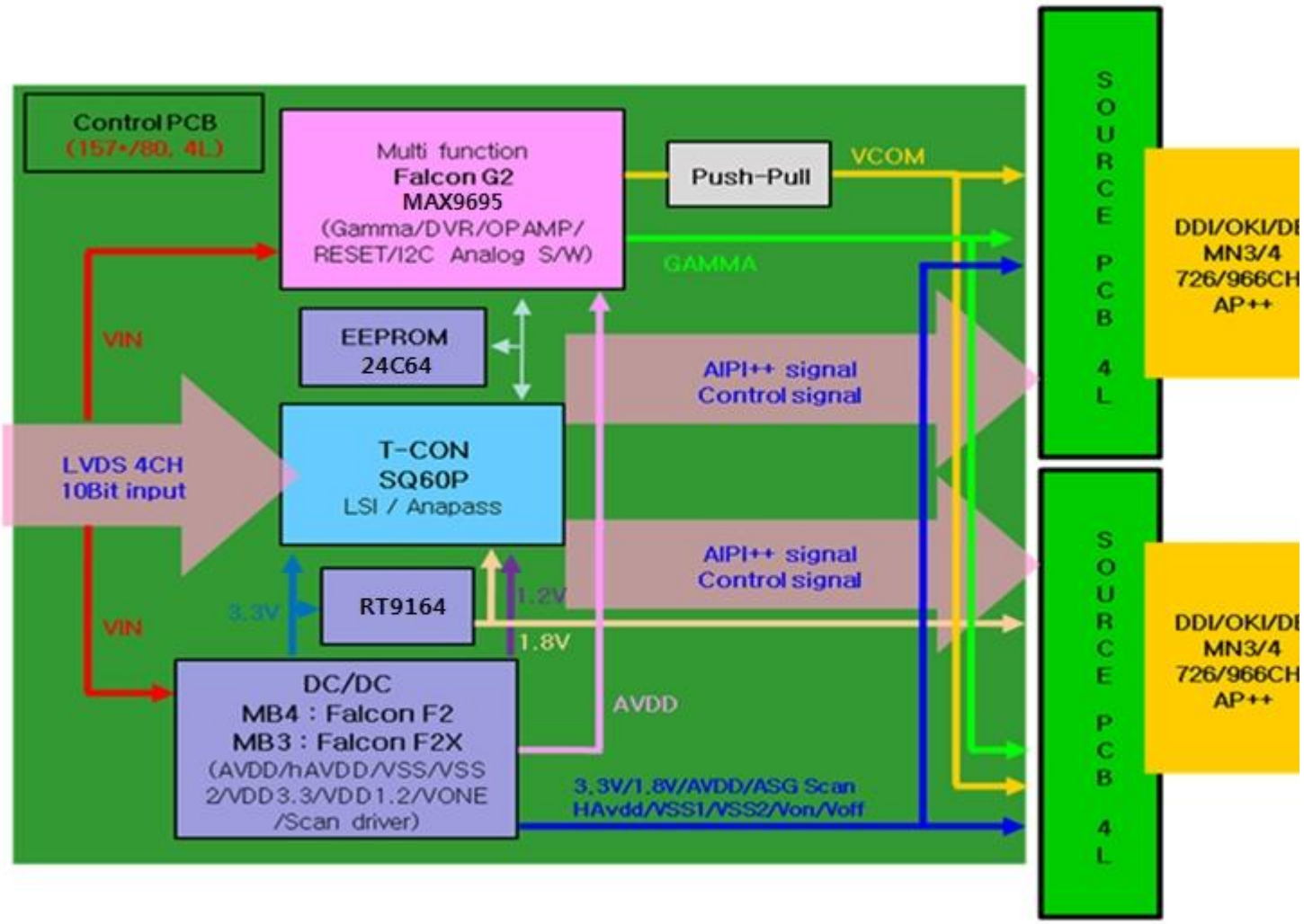
a) Black pattern b) White pattern c) V-stripe

(4) Conditions for measurement



The rush current, I_{RUSH} can be measured during T_{RUSH} is 470us

4. Block diagram



5. The Pin assignment in the input terminal

5.1. Input signal & power

Pin	Symbol	Description	Pin	Symbol	Description
1	TCON_WP	Bus release	19	Rx1CLK-	1st, 5thLVDS Clock -
2	SCL_I	I2C SCL	20	Rx1CLK+	1st, 5thLVDS Clock +
3	SDA_I	I2C SDA	21	GND	Ground
4	3D Format 0	Not Connect (2)	22	Rx1[D]N	1st, 5thLVDS Signal -
5	3D_SYNC_O	ShutterGlass sync output signal	23	Rx1[D]P	1st, 5thLVDS Signal +
6	3D Format 1	Not Connect (2)	24	Rx1[E]N	1st, 5thLVDS Signal - (1)
7	N.C	Not Connect	25	Rx1[E]P	1st, 5thLVDS Signal + (1)
8	N.C	Not Connect (3)	26	3D_EN	3D_EN signal
9	N.C	Not Connect (3)	27	N.C	Not Connect (3)
10	N.C	Not Connect (3)	28	Rx2[A]N	2nd, 6thLVDS Signal -
11	GND	Ground	29	Rx2[A]P	2nd, 6thLVDS Signal +
12	Rx1[A]N	1st, 5thLVDS Signal -	30	Rx2[B]N	2nd, 6thLVDS Signal -
13	Rx1[A]P	1st, 5thLVDS Signal +	31	Rx2[B]P	2nd, 6thLVDS Signal +
14	Rx1[B]N	1st, 5thLVDS Signal -	32	Rx2[C]N	2nd, 6thLVDS Signal -
15	Rx1[B]P	1st, 5thLVDS Signal +	33	Rx2[C]P	2nd, 6thLVDS Signal +
16	Rx1[C]N	1st, 5thLVDS Signal -	34	GND	Ground
17	Rx1[C]P	1st, 5thLVDS Signal +	35	Rx2CLK-	2nd, 6thLVDS Clock -
18	GND	Ground	36	Rx2CLK+	2nd, 6thLVDS Clock +

Pin	Symbol	Description	Pin	Symbol	Description
37	GND	Ground	44	GND	Ground
38	Rx2[D]N	2nd, 6thLVDS Signal -	45	GND	Ground
39	Rx2[D]P	2nd, 6thLVDS Signal +	46	GND	Ground
40	Rx2[E]N	2nd, 6thLVDS Signal - (1)	47	N.C	Not Connect
41	Rx2[E]P	2nd, 6thLVDS Signal + (1)	48	12V	DC power supply
			49	12V	DC power supply
42	N.C	Not Connect (3)	50	12V	DC power supply
43	N.C	Not Connect (3)	51	12V	DC power supply

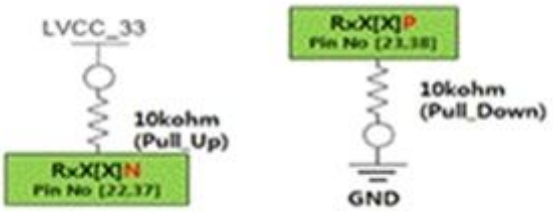
Note(1) :
- Input Mode 8Bit Setting & 8bit input 시, ==> E_Chanel : Floating
- Input Mode 10bit Setting & 8bit input 시, ==> E_Chanel : Keep Level '0'
  (41 PIN, 51 PIN) No.22 / No.37 : Pull Up
  (41 PIN, 51 PIN) No.23 / No.38 : Pull Down

* Level of LVDS signals are base on LVDS CHARACTERISTICS(9.4)

NOTE(2) : 3D input format selection

- FORMAT[1:0] : 2'b0x = Line interleave , 2'b10 = side/side , 2'b11 = top/bottom

Note(3) No connection: These PINS are used only for the product of SAMSUNG. (DO NOT CONNECT the input device to these pins.

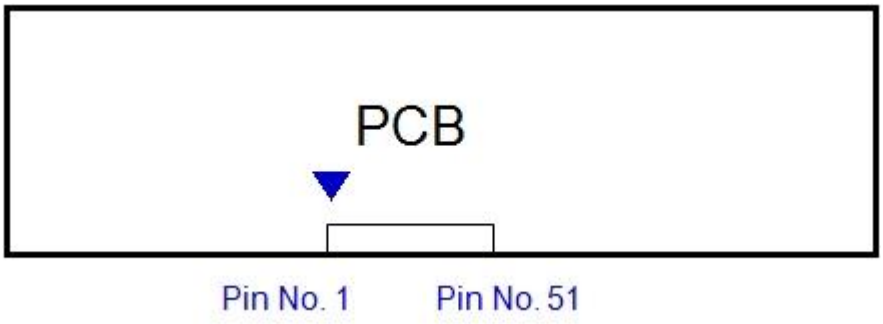


Note (1) NOT CONNECTED, THESE PINS ARE ONLY USED FOR SEC INTERNAL OPERATIONS.
(DO NOT CONNECT the input device to these pins)

Note(2) LVDS OPTION: IF THIS PIN : LOW (GND V)/ NC → JEIDA LVDS FORMAT
OTHERWISE : HIGH (3.3V) → NORMAL NS LVDS FORMAT

[Sequence Condition]
ON: V_{IN}(T1) → LVDS Option → Interface Signal(T2)
OFF: Interface Signal(T3) → LVDS Option → V_{IN}

Note (3) Pin number which starts from the left side.



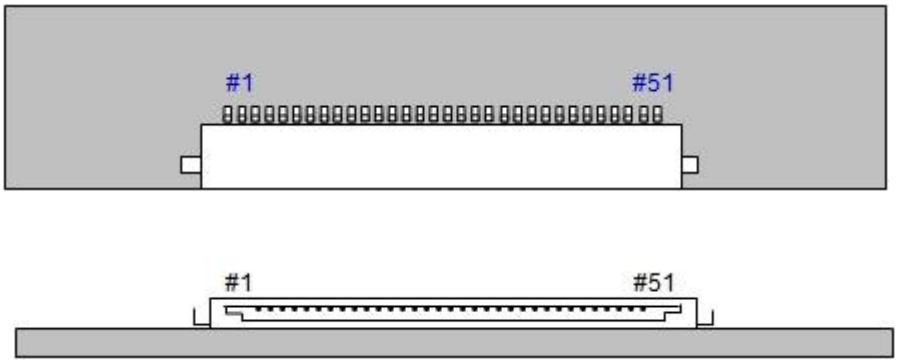


Fig . The diagram of connector

a. Power GND pins should be connected to the LCD's metal chassis.
b. All power input pins should be connected together.
c. All NC pins should be separated from other signal or power.

5-2. LVDS Interface

- LVDS Receiver :
- JEIDA

差動信號	LVDS pin	JEIDA
TxOUT/RxIN0	TxIN/RxOUT0	R4
	TxIN/RxOUT1	R5
	TxIN/RxOUT2	R6
	TxIN/RxOUT3	R7
	TxIN/RxOUT4	R8
	TxIN/RxOUT6	R9
	TxIN/RxOUT7	G4
TxOUT/RxIN1	TxIN/RxOUT8	G5
	TxIN/RxOUT9	G6
	TxIN/RxOUT12	G7
	TxIN/RxOUT13	G8
	TxIN/RxOUT14	G9
	TxIN/RxOUT15	B4
	TxIN/RxOUT18	B5
TxOUT/RxIN2	TxIN/RxOUT19	B6
	TxIN/RxOUT20	B7
	TxIN/RxOUT21	B8
	TxIN/RxOUT22	B9
	TxIN/RxOUT24	HSYNC
	TxIN/RxOUT25	VSYNC
	TxIN/RxOUT26	DEN
TxOUT/RxIN3	TxIN/RxOUT27	R2
	TxIN/RxOUT5	R3
	TxIN/RxOUT10	G2
	TxIN/RxOUT11	G3
	TxIN/RxOUT16	B2

	TxIN/RxOUT17	B3
	TxIN/RxOUT23	RESERVED
TxOUT/RxIN4	TxIN/RxOUT28	R0
	TxIN/RxOUT29	R1
	TxIN/RxOUT30	G0
	TxIN/RxOUT31	G1
	TxIN/RxOUT32	B0
	TxIN/RxOUT33	B1
	TxIN/RxOUT34	RESERVED

5.3 Input signals, basic display colors and the gray scale of each color.

COLOR	DISPLAY	DATA SIGNAL																												GRAY SCALE LEVEL
		RED										GREEN										BLUE									
		R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~ R1020
	↓ LIGHT	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1021
		0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1022
	RED	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1023
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~ G1020
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1021
		0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1022
	GREEN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1023
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~ B1020
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	B1021
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	B1022
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	B1023

Note) The definition of gray :
Rn : Red gray, Gn : Green gray, Bn : Blue gray (n = Gray level)
Input signal : 0 = Low level voltage, 1 = High level voltage

6. Interface timing

6.1 The parameters of timing (Only DE mode)

SIGNAL	ITEM	SMBOL	MIN.	TYP.	MAX.	Unit	NOTE
Clock	Frequency	$1/T_C$	130	148.5	152.5	MHz	-
Hsync		F_H	53	67.5	70	KHz	-
Vsync		F_V	48	60	62.5	Hz	-
Term for the vertical display	Active display period	T_{VD}	-	1080	-	Lines	-
	Total vertical	T_V	1100	1125	1400	Lines	-
Term for the horizontal display	Active display period	T_{HD}	-	1920	-	Clocks	-
	Total Horizontal	T_H	2092	2200	2348	clocks	-

Note) These products don't have to receive the signal of Hsync & Vsync from the input device.

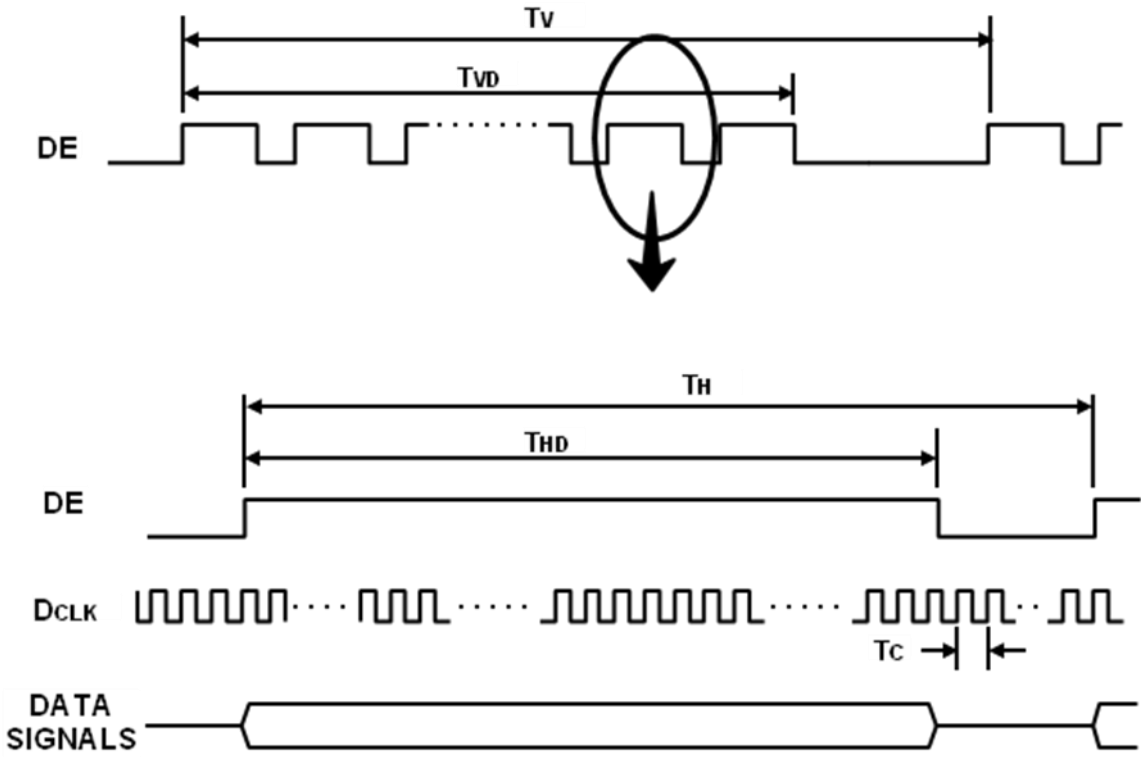
(1) Key points when testing: TTL controls the signal and the CLK at the input terminal of LVDS Tx of the system.

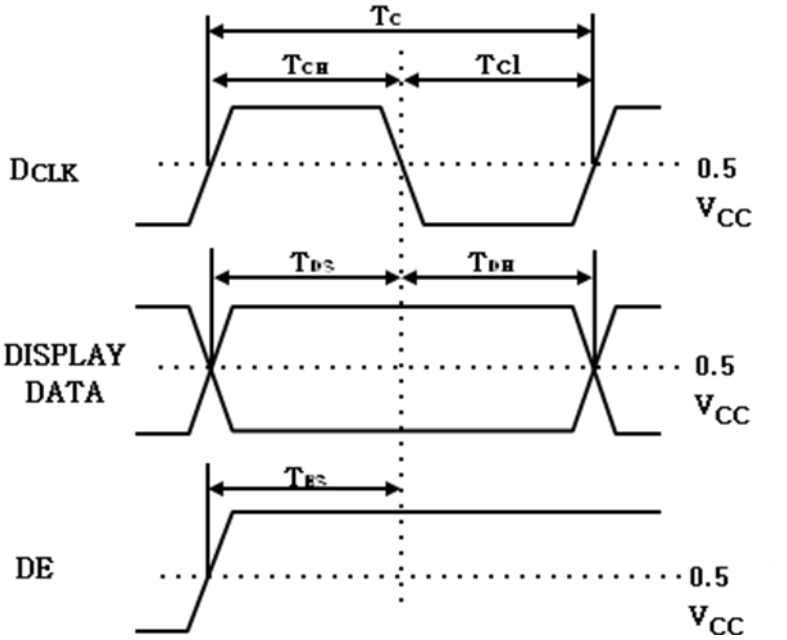
(2) Internal VDD = 3.3V

(3) Spread spectrum

- The limit of spread spectrum's range of SET in which the LCD module is assembled should be within ± 3 %.

6.2 Timing diagrams of interface signal (Only DE mode)



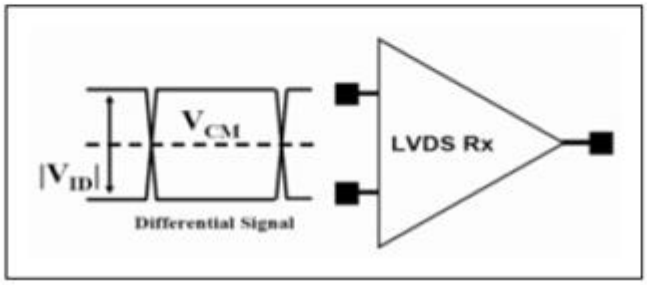


6.3 LVDS CHARACTERISTICS (SQ60PB)

-. DC Specification.

Definition of LVDS receiver DC characteristics

Characteristics	Symbol	Condition	Min.	Typ.	Max.	Unit
IO Supply Voltage	VDD33_LVDS		3.0	3.3	3.6	V
Core Supply Voltage	VDD12_LVDS		1.1	1.2	1.3	V
Color Depth				8/10		bit
Input Common Mode Voltage	V_{CM}		0.3		1.8	V
Differential Input Voltage	$\|V_{ID}\|$		100	350	600	mV



-. AC Specification.

LVDS receiver AC characteristics

Symbol	Characteristics	Min.	Typ.	Max.	Unit
F_{IN}	Input Clock Frequency (= 1/T)	25		90	MHz
t_{RCP}	Output Clock period	11.11		40	ns
t_{RSRM}	Input Data position			+400	ps
t_{RSLM}	Input Data position	-400			ps
t_{RPLL}	Lock Time			100	μsec
t_{duty}	Rx Output Clock Duty Ratio	45	50	55	%

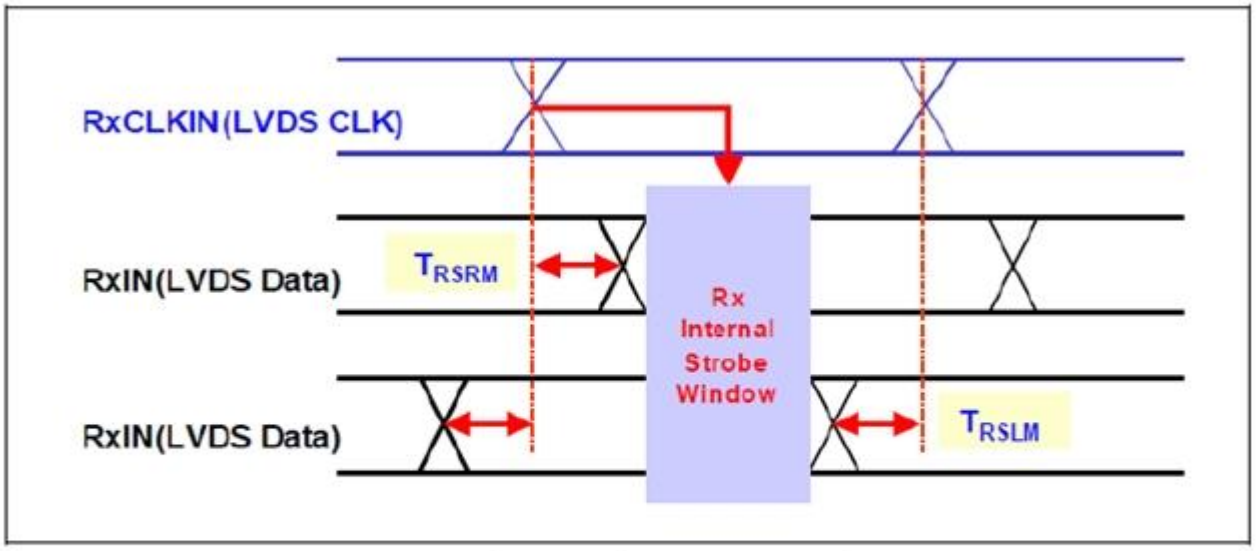


Figure 4. Timing diagram of LVDS receiver skew margin

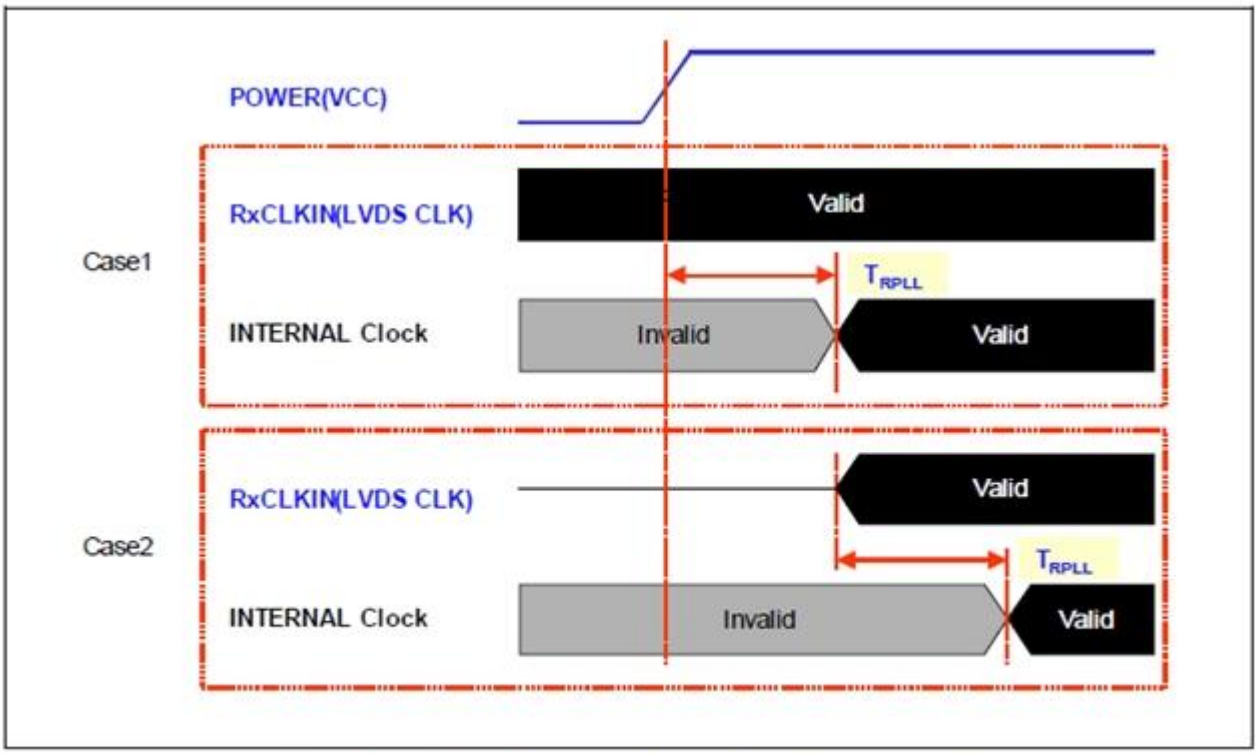
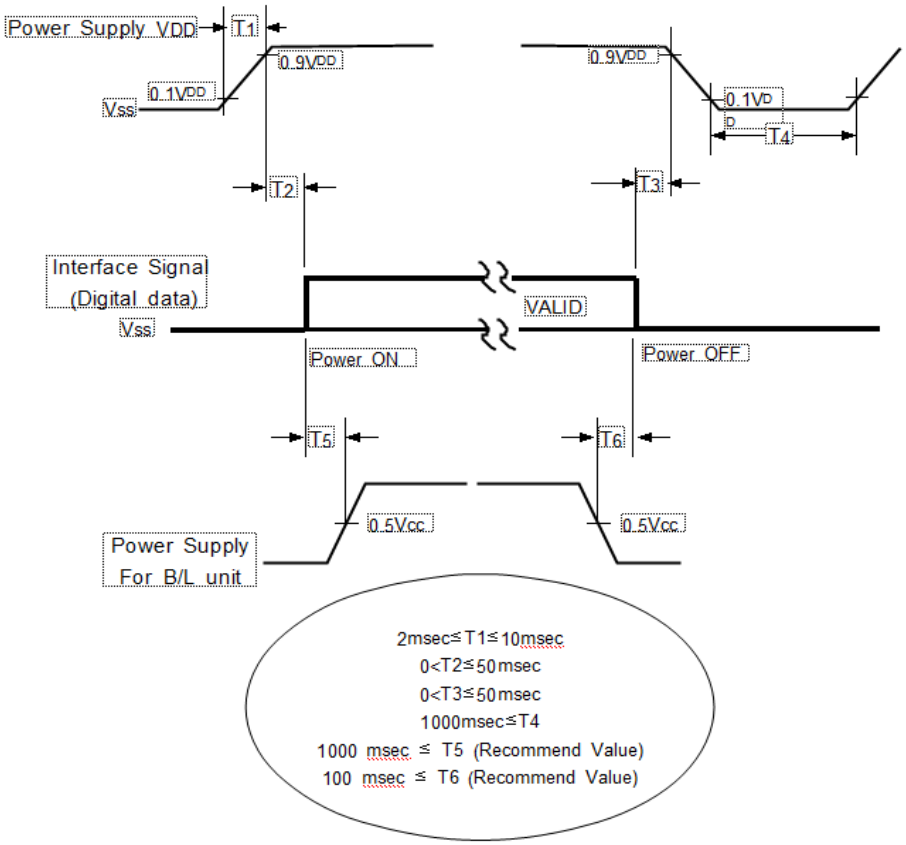


Figure 5. Timing diagram of LVDS receiver operation

6.4 The sequence of power on and off – Sony Model attached Reference file

To prevent a latch-up phenomena or the DC operation of the LCD Module, the power on/off sequence should be accorded with the settings described in the diagram below.



T1 : The V_{DD} rising time from 10% to 90%

T2 : The time from the point which V_{DD} reach to 90% of voltage to the point which the valid data is out when the power is on.

T3: The time from the point which the valid data is out to the point which V_{DD} reach to the 90% of voltage when the power is off.

T4: the time from the point which the Vdd decrease to the point which the Vdd increase again for windows to restart.

※ The recommended operating condition of the back light system

T5: The time which takes for B/L to be turned on after the signal is entered when the time is on.

T6 : The time which takes until the signal is out after BL is turned off

- The condition of supply voltage to enter in the module from the external system should have the same condition as the definition of V_{DD}.

- Apply the voltage for the lamp within the range which the LCD operates. when the back light is turned on before the LCD is operated or when the LCD is turned off before the back light is turned off, the display may show the abnormal screen momentarily.
- While the V_{DD} is off level, please keep the level of input signals low or keep a high impedance condition.
- The figure of T4 should be measured after the module has been fully discharged between the periods when the power is on and off.
- The interface signal must not keep the high impedance condition when the power is on.

7. Outline dimension

8. Reliability test

8.1 Panel

<table>
<tr><th>Item</th><th>Test Condition</th><th>Quantity</th><th>Note</th></tr>
<tr><td>HTOL</td><td>60 ℃ (Panel change 500hr / circuit change 250hr)</td><td>8</td><td></td></tr>
<tr><td>LTOL</td><td>-5 ℃ (Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>THB</td><td>50 ℃ / 90 %RH(Panel change 500hr / circuit change 250hr)</td><td>10</td><td></td></tr>
<tr><td>ASG
Low
temperature</td><td>Max. frequency 25℃~-40℃</td><td>Each
Cell</td><td>ASG Product Only</td></tr>
<tr><td>ASG
High
Temperature</td><td>Min. frequency 60℃Coperation 96hr</td><td>Each
Cell</td><td>ASG Product Only</td></tr>
<tr><td rowspan="2">Image sticking</td><td>25 ℃ / Mosaic pattern(9*10) 12hrs</td><td rowspan="2">8</td><td rowspan="2"></td></tr>
<tr><td>Rolling pattern 12hrs / 3cycles</td></tr>
<tr><td>Decompressio
n</td><td>-40~50℃, 0m(0ft) ~ 13,700m(45,000ft), 72.5Hr</td><td>4</td><td></td></tr>
<tr><td>HTS</td><td>70 ℃, Storage (Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>LTS</td><td>-25 ℃, Storage(Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>Transportation
condition</td><td>drop(20cm) → temperature/humidity(-30~60℃ / 40℃ 90%RH)
→ pressure → vibration(5~200Hz 1.05Grms, 2hr) → drop(20cm)</td><td>1pallet</td><td></td></tr>
<tr><td>WHTS</td><td>60 ℃ / 75 %RH , Storage</td><td>4</td><td></td></tr>
<tr><td>Noise</td><td>Electromagnetic noise: Overall 23dB 이하</td><td>2</td><td></td></tr>
<tr><td>Complex
stress</td><td>-20℃~60℃, 0~90%RH, 2cycle</td><td>4</td><td></td></tr>
<tr><td>ESD</td><td>S-IC Input ±7KV, Output ±4KV
Output 은 data TP 에 직접 인가 후 진행
Input 은 CKV,VCOM 등에 FFC CNT 를 통하여 TEST 를 진행</td><td>3</td><td></td></tr>
<tr><td>EOS (optional)</td><td><table><tr><th>Item</th><th>Test condition</th></tr><tr><td>Vin Input
step</td><td>Surge combination (High impedance)
Pass Condition: 5kV under</td></tr><tr><td>Signal Input
step</td><td>Surge combination (High impedance)
Pass Condition: 120V under</td></tr></table></td><td>2</td><td></td></tr>
</table>

[Criteria on evaluation]

There should be no change of the product, which may affect to the practical display functions, when the display quality test is executed under the normal operation setting.

* HTOL/ LTOL : The operating cycle on the high and low temperature
* THB : Temperature humidity slant
* HTS/LTS : The storage at the high and low temperature
* WHTS : The storage in the high temperature with the high humidity

9. General precautions

9.1 Handling

(a) When the panel kit and BLU kit are assembled, the panel kit and BLU kit should be attached to the set system firmly by combining each mounted holes. Be careful not to give the mechanical stress.

(b) Be careful not to give any extra mechanical stress to the panel when designing the set, and BLU kit.

(c) Be cautious not to give any strong mechanical shock and / or any forces to the panel kit.
Applying the any forces to the panel may cause the abnormal operation or the damage to the panel kit and the back light unit kit.

(d) Refrain from applying any forces to the source PBA and the drive IC in the process of the handling or installing to the set. If any forces are applied to the products, it may cause damage or a malfunction in the panel kit.

(e) Refrain from applying any forces which cause a constant shock to the back side of panel kit, the set design and BLU kit. If any forces are applied to the products, it may cause an abnormal display, a functional failure and etc.

(f) Note that polarizer could be damaged easily.
Do not press or scratch the bare surface with the material which is harder than a HB pencil lead.

(g) Wipe off water droplets or oil immediately. If you leave the droplets for a long time on the product, a staining or the discoloration may occur.

(h) If the surface of the polarizer is dirty, clean it using the absorbent cotton or the soft cloth.

(i) Desirable cleaners are water or IPA (Isopropyl Alcohol).
Do not use Kenton type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. These might cause the permanent damage to the polarizer due to chemical reaction.

(j) If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.

(k) Protect the panel kit and BLU Kit out of the static electricity. Otherwise the circuit IC could be damaged.

- Reference : Process control standard of SDC

No.	Item	Control standard
1	Ionizer	All Equipment should be controlled under 150V.(Typ. 100V)
2	Carrying Roller	Carrying Roller should be controlled under 200V.
3	Equipment Ground Resistance	All Equipment Ground Should be less than 1ohm.

(l) Remove the stains with finger-stalls wearing soft gloves in order to keep the display clean in the process of the incoming inspection and the assembly process.

(m) Do not pull or fold the source drive IC which connects to the source PBA and the panel or the gate drive IC.

(n) Do not pull, fold or bend the source drive IC and the gate drive IC in any processes.
If not, the source drive IC could be bent one time in the process of assembling the panel Kit and the BLU Kit.

(o) Do not adjust the variable resistor located on the panel kit and BLU kit except when adjusting the flicker.

(p) Do not touch the pins of the interface connector directly with bare hands.

(q) Be cautious not to be peeled off the protection film.

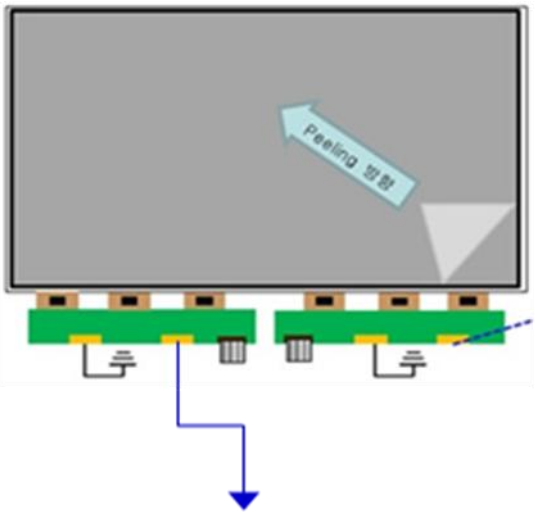


Fig. GND SR-Open Pattern – Be sure to be contacted to the ground while peeling of the protection film

- Make sure to peel off slowly
(It is recommended to peel it off at the speed of more than 8sec. constantly.)
- The peeling direction is shown at the Fig
- Instruct the ground worker to work with the adequate methods such as the antistatic wrist band.
- Maker sure to be grounded the source PBA while peeling of the protection film.
- Ionized air should be blown over during the peeling
- The protection film should not t be contacted to the source drive IC.
- If the adhesive stains remain on the polarizer after the protection film is peeled off, please move stains with isopropyl-alcohol liquid.

(r) The protection film for the polarizer on the panel kit should be slowly peeled off just before using so that the electrostatic charge can be minimized.

(s) The panel kit and BLU kit have high frequency circuits. The sufficient suppression to the EMI should be done by the set manufacturers.

(t) The set of which the panel is assembled shall not be twisted. If the product is twisted, it may cause the damage on the product.

(u) Surface Temp. of IC should be controlled less than 100℃, operating over the Temp. can cause the damage or decrease of lifetime.

9.2 Storage

The storage condition for packing

<table>
<tr><th>ITEM</th><th colspan="2">Unit</th><th colspan="2">Min.</th><th colspan="2">Max.</th></tr>
<tr><td>Storage Temperature</td><td colspan="2">(℃)</td><td colspan="2">5</td><td colspan="2">40</td></tr>
<tr><td>Storage Humidity</td><td colspan="2">(%rH)</td><td colspan="2">35</td><td colspan="2">75</td></tr>
<tr><td>Storage life</td><td colspan="6">6 months</td></tr>
<tr><td rowspan="3">Storage Condition</td><td colspan="6">(1) The storage room should provide good ventilation and temperature control.
(2) Products should not be placed on the floor, but on the Pallet away from a wall.
(3) Prevent products from direct sunlight, moisture nor water; Be cautious of a buildup of condensation.
(4) Avoid other hazardous environment while storing goods.
(5) If products delivered or kept in conditions of the recommended temperature or humidity, we recommend you leave them at a circumstance which is shown in the following table.</td></tr>
<tr><td>period</td><td>1 month</td><td>2 months</td><td>3 months</td><td>4 months</td><td>5 months</td><td>6 months</td></tr>
<tr><td>Baking Condition</td><td colspan="2">No Baking</td><td>50℃, 10% 24Hr</td><td colspan="3">50℃, 10%, 48Hr</td></tr>
</table>

9.3 Operation

(a) Do not connect or disconnect the FFC cable during the "Power On" condition.

(b) Power supply should be always turned on and off by the "Power on/off sequence"

(c) The module has high frequency circuits. The sufficient suppression to the electromagnetic interference should be done by the system manufacturers. The grounding and shielding methods is important to minimize the interference.

(d) The cables between TV SET connector and Control PBA interface cable should be connected directly to have a minimized length. A longer cable between TV SET connector and Control PBA interface cable maybe operate abnormal display

(e) Recommend to age for over 1 hour at least in the state, which the product is driving initially to stabilize the characteristic of the initial TFT.

(f) Response time depends on the temperature.(In Lower temperature, it becomes longer)

9.4 Operation condition guide

(a) The LCD product shall be operated under normal conditions.
The normal condition is defined as below;
- Temperature : 20±15℃
- Humidity : 55±20%
- Display pattern : continually changing pattern (Not stationary)

(b) If the product will be used under extreme conditions such as under the high temperature, humidity, display patterns or the operation time etc.., it is strongly recommended to contact SDC for the advice about the application of engineering . Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.

9.5 Others

(a) The ultra-violet ray filter is necessary for the outdoor operation.

(b) Avoid the condensation of water which may result in the improper operation of product or the disconnection of electrode.

(c) Do not exceed the limit on the absolute maximum rating. (For example, the supply voltage variation, the input voltage variation, the variation in content of parts and environmental temperature, and so on) If not, panel may be damaged.

(d) If the module keeps displaying the same pattern for a long period of time, the image may be remained to the screen. To avoid the image sticking, it is recommended to use a screen saver.

(e) This Panel has its circuitry of PCB's on the rear side, so it should be handled carefully in order for a force not to be applied.

(f) Please contact the SDC in advance when the same pattern is displayed for a long time

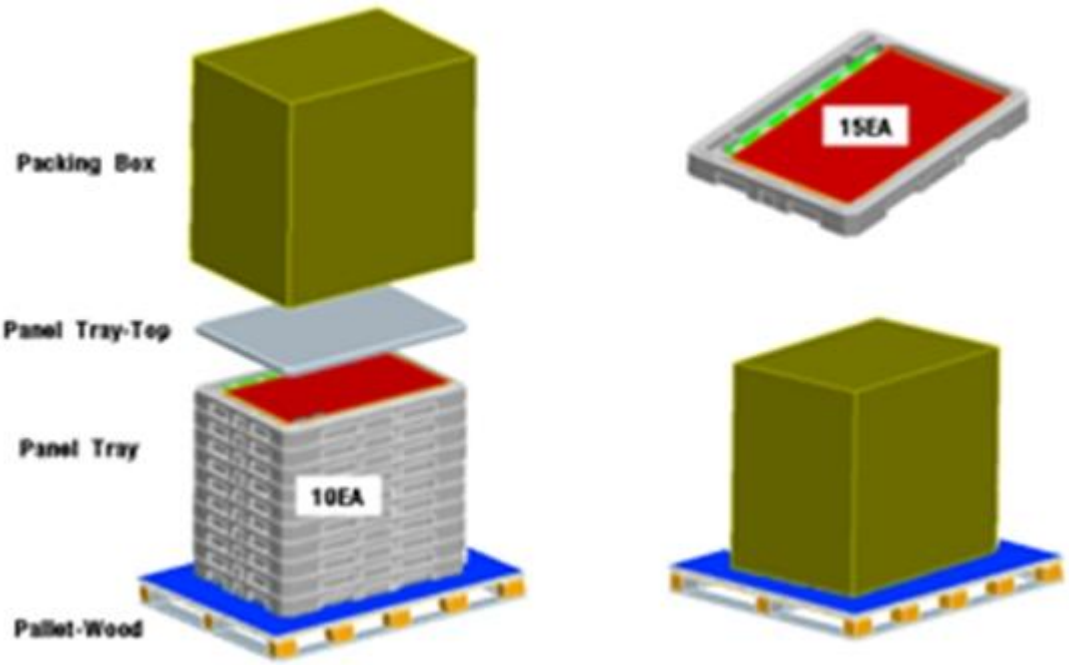
10. Special precautions

10.1 Lists to be cautious when executing the design process

No.	Component	Expected cause
1	Upholding part for panel	Prevent the panel from breaking by assigning gaps between the panel and the upholding part for panel on the drawing for the upholding part for panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
2	The shape of the upholding part for panel	Design the upholding part for panel to fit to the panel appropriately when designing the BLU since the shape of the upholding part for panel may damage the panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
3	The edge of upholding part for panel	Design the edge of panel to have a sufficient space with the upholding part for panel when designing the BLU since the edge of the upholding part for panel may damage the panel when assembling the panel and BLU. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
4	Upholding part for panel	Place the upholding part for the panel in order for the shape of mold, which contacts with the panel not to interfere with the area of panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
5	Drive IC	Design the BLU in order for the COF not to contain the lead crack resulted from the tensioned COF created when the product is twisted if the space between the D-IC COF and the middle mold isn't sufficient. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
6	Drive IC	Design the BLU in order for the product not to contain the lead crack resulted from the tensioned COF caused under the condition, which the product is twisted by fixing the source PCB. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
7	IC component	1) The temperature of each part of product suggested by our company and the second vendor shall meet the standard of temperature, which is recommended not to be exceeded by our company when the product is affected under the various temperature ranges. Apply over 1mm long separation distance stated in the safety standard between the electric part and each conductor. (Apply the rated separation distance when insulating.)
8	Thermal pad	Apply the thermal pad in a designated size to the product as a measure to lower the temperature of heat in order for each part to use the rated temperature.
9	POL	The surrounding area of the POL shall be treated with an electrification treatment since the external ESD may cause a phenomenon, which the POL is coming off. In addition, the GND portion of source PBA shall be grounded.
10	PBA	The GND portion of each PBA shall be contacted with the GND portion of BLU. Refer to the (a) and (b) of 3-3 for the design of BLU.
11	Circuit	The standardized approval from the client is required since the EMI is executed by a client. Our company can only measure the reference since the client measures the BLU.
12	The height of component	Design the BLU with considering the maximum height of parts, which our company suggests.
13	Between the FFC and the C-PBA	Design the instrument with considering the length between the FFC and the control PBA. (The marginal minimum length of 5mm or 8mm is required.)
14	Panel	The surface temperature of panel shall be maintained within 0℃ and 45℃ when the external ambient temperature is at 25℃. (Design the BLU with considering the increase of the temperature in the panel by the LED, CCFL, and etc.)
15	Aging	Recommend to age for over 1 hour at least in the state, which the product is driving initially to stabilize the characteristic of the initial TFT.
16	The attachment of gasket	The additional confirmation by our company is required If the attachment of gasket to the S-PBA of our company is required.(To fix the S-PBA or the EMI)
17	Drive IC	Design the top chassis and the driver IC to be contacted by placing the shape of emboss inside the top chassis as a measure to prevent the driver IC from heating. The size of emboss shall be designed in larger size than the size of IC inside the film of the driver IC. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
18	The prohibited bandwidth	Design the BLU in order for the BLU not to interfere with the area, where the control PBA and the source PBA are located densely according to the drawing for the BLU from our company.
19	S-PBA	The material, which contacts with the bottom side of S-PBA which has a pattern shall be non-conducting material or shall be insulated.

11. PACKING

11.1 Pallet



11.2 Packing Specification

ITEM	Specification	Remark
Total Pallet Size	W×V×Height [mm]	-. 1475 X 1150 X 1100
Tray	15 [Panel/Tray]	-. Panel : 51.0 kg (3.4 kg/Panel, 15ea/Tray)) -. Middle Sheet : 1.62kg (0.09 kg/ea, 18ea/Tray) -. Panel Tray : 3.2kg (EPS)
Pallet	11[Tray/Pallet]	-. Pallet 24.5 kg (Wood Pallet) -. 10ea + 1ea(Top tray)
Total Weight	556.8 [kg]	-. Packing Box : 3kg (Paper)