4-BIT BI-DIRECTIONAL LEVEL TRANSLATOR OPEN-DRAIN AND PUSH-PULL APPLICATIONS

Description

The LSF0204 is a 4-channel bi-directional multi-voltage level translator for open-drain and push-pull applications. This device is a universal level translator with A port operating from 0.8V to 4.5V (Vref_A) and B port from 1.8V to 5.5V (Vref_B). This range allows for bi-directional voltage translations between 0.8V and 5.0V. Be aware that Vref_B is recommended to be at 1.0V higher than Vref_A for the best signal integrity.

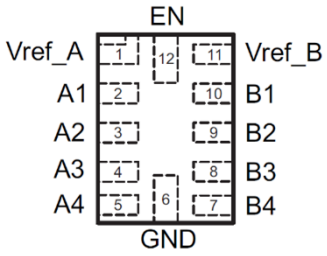
The EN pin is used to activate the device. When EN is HIGH, the translator switch is on. Otherwise, if EN is LOW, the translator switch is off, and a high-impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_A. EN must be LOW to ensure the high-impedance state during power-up or power-down to avoid misoperation.

Please note that an external Rpu (pullup resistor) is required on port A and B for push-pull and open-drain application because a pull-high state can avoid misoperation during the power sequence. About the Rpu, the smaller value can result in the larger driving current. Overall, the LSF0204 is designed for easy-to-use with auto direction. So, there is no need for a direction pin to minimize system effort. This device supports 5V tolerant I/O pins for compatibility with TTL levels in a variety of applications which require a proper voltage translation.

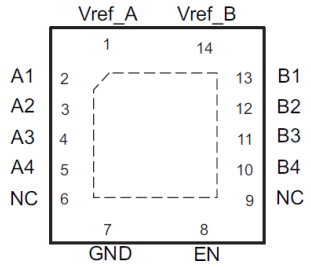
Features

- External Rpu (Pullup Resistor) to Set Driving Current in Both Push-Pull and Open-Drain Applications
- Up & Down Translation
  - ≤ 100MHz; C_L = 15pF, 30pF
  - ≤ 50MHz; C_L = 50pF
- Bi-Directional Voltage Level Translation Between:
  - 0.8V and 1.8V, 2.5V, 3.3V and 5.0V
  - 1.2V and 1.8V, 2.5V, 3.3V and 5.0V
  - 1.8V and 2.5V, 3.3V and 5.0V
  - 2.5V and 3.3V and 5.0V
  - 3.3V and 5.0V
- ESD Protection Exceeds JESD 22
  - 2000V HBM (A114)
  - 1000V CDM (C101)
- Latchup Exceeds 100mA per JESD 17
- Specified from -40°C to +125°C
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **An automotive-compliant part is available under separate datasheet (LSF0204Q)**

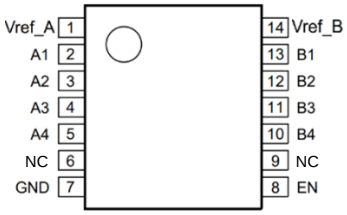
Pin Assignments



U-QFN1720-12 (Type CJ)



V-QFN3535-14 (Type CJ)



TSSOP-14

Applications

- GPIO, MDIO, SDIO, SVID, UART
- PMBus™, SMBus™, I2C, and other interfaces
- Telecom infrastructures
- Industrial
- High-performance computing
- Wide array of products such as:
  - PCs, networking, notebooks
  - Smart phones
  - Tablets

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Pin Descriptions

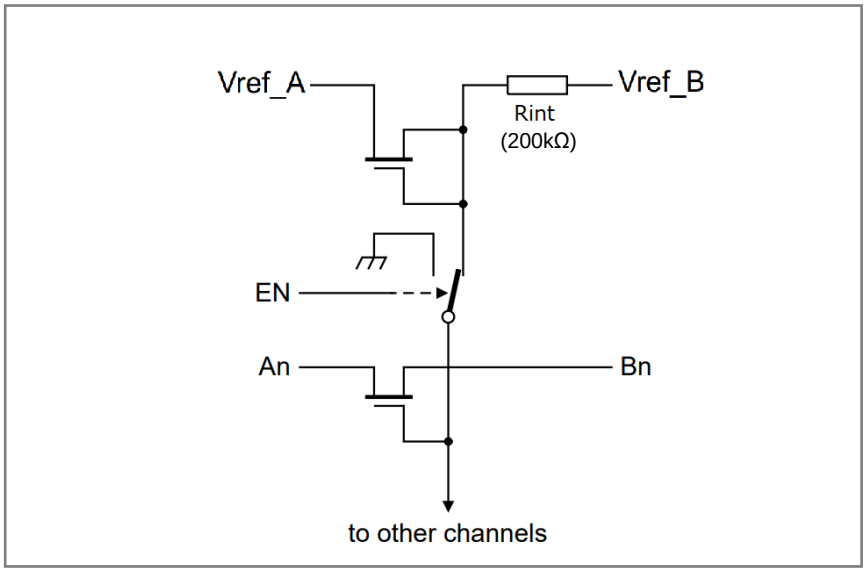
Pin Name	TSSOP-14	U-QFN1720-12 (Type CJ)	V-QFN3535-14 (Type CJ)	Function
V_{ref_A}	1	1	1	Reference supply voltage; A port
A1	2	2	2	Input/output 1
A2	3	3	3	Input/output 2
A3	4	4	4	Input/output 3
A4	5	5	5	Input/output 4
NC	6	—	6	No connection. Not internally connected.
GND	7	6	7	Ground
EN	8	12	8	Switch enable input; EN is high-active.
NC	9	—	9	No connection. Not internally connected.
B4	10	7	10	Input/output 4
B3	11	8	11	Input/output 3
B2	12	9	12	Input/output 2
B1	13	10	13	Input/output 1
V_{ref_B}	14	11	14	Reference supply voltage; B port

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	±2	kV
ESD CDM	Charged Device Model ESD Protection	±1	kV
V_{REF}	Supply Reference Voltage Range	-0.5 to +6.0	V
V_I	Input Voltage Range	-0.5 to +6.0	V
V_O	Voltage Range Applied to Any Output in the High-Z or Power-Off State	-0.5 to +6.0	V
I_{CH}	Continuous Channel Current	128	mA
I_{IK}	Input Clamp Current, $V_I < 0$	-50	mA
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Storage Temperature	-65 to +150	°C

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Functional Diagram



Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
V_{REF}	Reference Voltage, A & B Ports	0.8	5.5	V
$V_{I/O}$	Input/Output Voltage	0.8	5.5	V
V_{EN}	Enable Voltage	0	5.5	V
I_{PASS}	Pass Transistor Current	—	64	mA
T_A	Operating Free-Air Temperature	-40	+125	°C

Electrical Characteristics (Note 5) (@T_A = +40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{ref_A}	A Port Supply Voltage	—		0.8	—	4.5	V
V_{ref_B}	B Port Supply Voltage	—		1.8	—	5.5	V
V_{IK}	—	I_I = -18mA, V_{EN} = 0		-1.2	—	—	V
I_{IH}	—	V_I = 5V, V_{EN} = 0		—	—	5.0	µA
I_{CCBA}	Leakage from Vref B to Vref_A	V_{ref_B} = 3.3V, V_{ref_A} = 1.8V, V_{EN} = V_{ref_A}, I_O = 0 V_I = 3.3V or GND		—	—	3.5	µA
I_{CCA} + I_{CCB}	Total Current Through GND	V_{ref_B} = 3.3V, V_{ref_A} = 1.8V, V_{EN} = V_{ref_A}, I_O = 0 V_I = 3.3V or GND		—	0.2	—	µA
I_{IN}	Control Pin Current	V_{ref_B} = 5.5V, V_{ref_A} = 4.5V, V_{EN} = 0 to V_{ref_A}, I_O = 0		—	—	±1	µA
I_{off}	Power Off Leakage Current	V_{ref_B} = V_{ref_A} = 0, V_{EN} = GND, I_O = 0, V_I = 5V or GND		—	—	±1	µA
C_I (ref_A/B/EN)	—	V_I = 3V or 0		—	7	—	pF
C_{io} (off)	—	V_O = 3V or 0, V_{EN} = 0		—	5.0	6.0	pF
C_{io} (on)	—	V_O = 3V or 0, V_{EN} = V_{ref_A}		—	10.5	13	pF
V_{IH} (EN)	High-Level Input Voltage	V_{ref_A} = 1.5V to 4.5V		0.7×V_{ref_A}	—	—	V
V_{IL} (EN)	Low-Level Input Voltage	V_{ref_A} = 1.5V to 4.5V		—	—	0.3×V_{ref_A}	V
V_{IH} (EN)	High-Level Input Voltage	V_{ref_A} = 1.0V to 1.5V		0.8×V_{ref_A}	—	—	V
V_{IL} (EN)	Low-Level Input Voltage	V_{ref_A} = 1.0V to 1.5V		—	—	0.3×V_{ref_A}	V
Δt/Δv (EN)	Input Transition Rise or Fall Rate for EN Pin	—		—	10	—	ns/V
R_{on}	—	V_I = 0, I_O = 64mA	V_{ref_A} = V_{EN} = 3.3V; V_{ref_B} = 5V	—	3	—	Ω
			V_{ref_A} = V_{EN} = 1.8V; V_{ref_B} = 5V	—	4	—	
		V_I = 0, I_O = 32mA	V_{ref_A} = V_{EN} = 1.0V; V_{ref_B} = 5V	—	5	—	Ω
			V_{ref_A} = V_{EN} = 1.8V; V_{ref_B} = 5V	—	4	—	
		V_I = 0, I_O = 32mA, V_{ref_A} = V_{EN} = 2.5V; V_{ref_B} = 5V		—	3	—	Ω
		V_I = 1.8V, I_O = 15mA, V_{ref_A} = V_{EN} = 3.3V; V_{ref_B} = 5V		—	5	—	Ω
		V_I = 1.0V, I_O = 10mA, V_{ref_A} = V_{EN} = 1.8V V_{ref_B} = 3.3V		—	8	—	Ω
		V_I = 0, I_O = 10mA, V_{ref_A} = V_{EN} = 1.0V; V_{ref_B} = 3.3V		—	6	—	Ω
		V_I = 0, I_O = 10mA, V_{ref_A} = V_{EN} = 1.0V; V_{ref_B} = 1.8V		—	6	—	Ω

Note: 5. All typical values are at T_A = +25°C. Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals. The actual supply current for LSF0204 is I_{CCA} + I_{CCB}; the leakage from Vref_B to Vref_A can be measured on Vref_A and Vref_B pins.

EN Pin Characteristics (Note 6) (@T_A = +40°C to +125°C, unless otherwise specified.)

Translating Down, 3.3V to 1.8V

Parameter	From EN Pin	To Port A or B	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLZ} (LOW to OFF)			13	20	12	20	11	20	ns
t_{PZL} (OFF to LOW)			35	50	30	40	25	40	ns
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 3.3V, V_M = 0.9V, V_{EN} = 1.8V, V_{EXT} = V_{ref_A}, Rpu = NA, V_{IH} = 3.3V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Up, 1.8V to 3.3V

Parameter	From EN Pin	To Port A or B	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLZ} (LOW to OFF)			13	20	12	20	11	20	ns
t_{PZL} (OFF to LOW)			35	50	30	40	25	40	ns
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 3.3V, V_M = 0.9V, V_{EN} = 1.8V, V_{EXT} = V_{ref_A}, Rpu = NA, V_{IH} = 3.3V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Down Characteristics (Note 6) (@T_A = +40°C to +125°C, unless otherwise specified.)

Translating Down, 5.0V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	B	A	0.6	5.1	0.5	5.1	0.3	5.0	ns
t_{PHL}			1.1	4.8	0.9	4.5	0.5	4.4	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 5.0V, V_M = 2.15V, V_{EN} = 1.8V, Switch = S2, V_{IH} = 5.0V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Down, 3.3V to 1.8V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	B	A	0.7	5.5	0.5	5.3	0.3	5.2	ns
t_{PHL}			0.9	4.9	0.7	4.7	0.5	4.5	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 3.3V, V_M = 1.15V, V_{EN} = 1.8V, Switch = S2, V_{IH} = 3.3V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Down, 3.3V to 1.2V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	B	A	0.8	4.1	0.5	3.9	0.3	3.8	ns
t_{PHL}			0.9	4.7	0.7	4.5	0.6	4.3	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.2V, V_{ref_B} = 3.3V, V_M = 0.85V, V_{EN} = 1.2V, Switch = S2, V_{IH} = 3.3V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Note: 6. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; Rpu = pullup resistor as load resistance; S1/S2 = Test selection switch.

Translating Down Characteristics (continued) (Note 6) (@T_A = +40°C to +125°C, unless otherwise specified.)

Translating Down, 1.8V to 1.2V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	B	A	1.3	4.6	1.1	4.4	1.0	4.1	ns
t_{PHL}			1.4	5.3	1.3	5.1	1.2	4.7	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.2V, V_{ref_B} = 1.8V, V_M = 0.65V, V_{EN} = 1.2V, Switch = S2, V_{IH} = 1.8V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Down, 1.8V to 0.8V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	B	A	1.5	4.7	1.2	4.5	1.1	4.3	ns
t_{PHL}			1.7	5.6	1.6	5.3	1.3	5.0	ns
f_{MAX}			50		80		100		MHz
Test Conditions: V_{ref_A} = 0.8V, V_{ref_B} = 1.8V, V_M = 0.55V, V_{EN} = 0.8V, Switch = S2, V_{IH} = 1.8V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Up Characteristics (Note 6) (@T_A = +40°C to +125°C, unless otherwise specified.)

Translating Up, 1.8V to 5.0V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A	B	0.6	5.7	0.4	5.3	0.2	5.2	ns
t_{PHL}			1.3	6.7	1.0	6.4	0.7	5.3	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 5.0V, V_M = 2.05V, V_{EN} = 1.8V, Switch = S1, Rpu = 500Ω, V_{EXT} = 5.0V, V_{IH} = 1.8V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Up, 1.8V to 3.3V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A	B	0.6	5.7	0.4	5.3	0.2	5.2	ns
t_{PHL}			1.3	6.7	1.0	6.4	0.7	5.3	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.8V, V_{ref_B} = 3.3V, V_M = 2.05V, V_{EN} = 1.8V, Switch = S1, Rpu = 500Ω, V_{EXT} = 5.0V, V_{IH} = 1.8V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Up, 1.2V to 3.3V

Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A	B	0.7	7.3	0.4	7.1	0.2	6.9	ns
t_{PHL}			1.6	7.1	1.3	6.5	1.0	5.4	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.2V, V_{ref_B} = 3.3V, V_M = 0.75V, V_{EN} = 1.2V, Switch = S1, Rpu = 500Ω, V_{EXT} = 3.3V, V_{IH} = 1.2V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Note: 6. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; Rpu = pullup resistor as load resistance; S1/S2 = Test selection switch.

Translating Up Characteristics (continued) (Note 6) (@T_A = +40°C to +125°C, unless otherwise specified.)

Translating Up, 1.2V to 1.8V

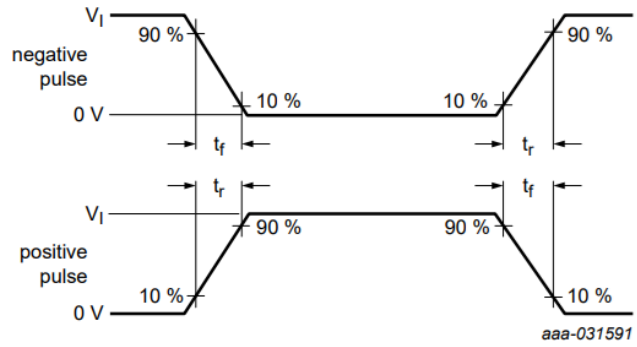
Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A	B	0.7	7.3	0.4	7.1	0.2	6.9	ns
t_{PHL}			1.6	7.1	1.3	6.5	1.0	5.4	ns
f_{MAX}			50		100		100		MHz
Test Conditions: V_{ref_A} = 1.2V, V_{ref_B} = 1.8V, V_M = 0.75V, V_{EN} = 1.2V, Switch = S1, Rpu = 500Ω, V_{EXT} = 3.3V, V_{IH} = 1.2V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Translating Up, 0.8V to 1.8V

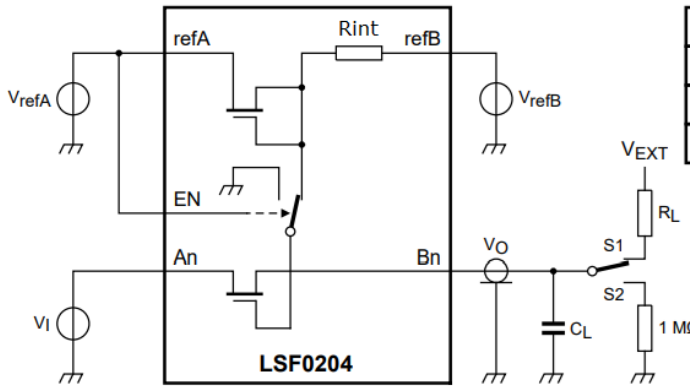
Parameter	From (Input)	To (Output)	C_L = 50pF		C_L = 30pF		C_L = 15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A	B	0.7	7.3	0.5	7.2	0.3	6.9	ns
t_{PHL}			1.6	7.1	1.4	6.6	1.0	5.4	ns
f_{MAX}			40		80		100		MHz
Test Conditions: V_{ref_A} = 0.8V, V_{ref_B} = 1.8V, V_M = 0.55V, V_{EN} = 0.8V, Switch = S1, Rpu = 500Ω, V_{EXT} = 1.8V, V_{IH} = 0.8V, V_{IL} = 0, PRR = 10MHz (unless otherwise noted, see Figure 1)									

Note: 6. All typical values are measured at T_A = +25°C. Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz; Z_O = 50Ω. Definitions test circuit: C_L = Load capacitance including jig and probe capacitance; Rpu = pullup resistor as load resistance; S1/S2 = Test selection switch.

Parameter Measurement Information



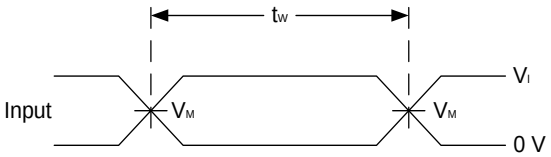
V_I source waveform



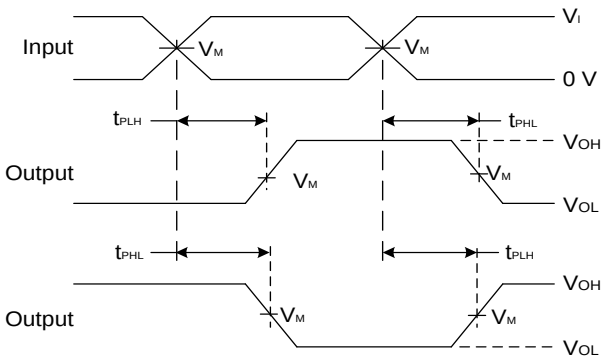
Measurement		switch
t_{PHL}/t_{PLH}, f_{max}	Translating up	S1
t_{PHL}/t_{PLH}, f_{max}	Translating down	S2
t_{PZL}/t_{PLZ}	Translating up/down	S1

Test circuit

Parameter Measurement Information (continued)



Voltage Waveform Pulse Duration



Voltage Waveform Propagation Delay Times Inverting and Non-Inverting Outputs

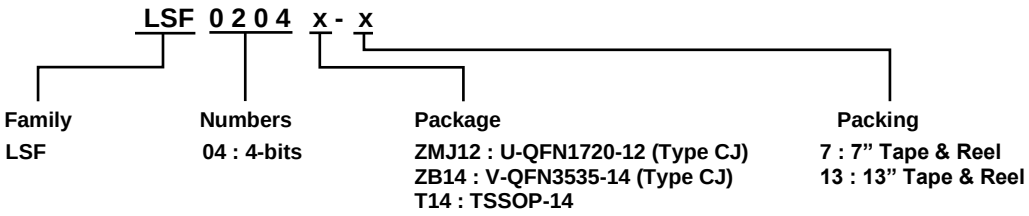
Figure 1. Load Circuit and Voltage Waveforms, R_L = 500Ω, C_L = 15pF, 30pF, 50pF

Package Characteristics

Symbol	Parameter	Package	Test Conditions	Min	Typ	Max	Unit
θ_{JA}	Thermal Resistance Junction-to-Ambient	U-QFN1720-12 (Type CJ)	(Note 7)	—	185	—	°C/W
		TSSOP-14		—	125	—	
		V-QFN3535-14 (Type CJ)		—	89	—	
θ_{JC}	Thermal Resistance Junction-to-Case	U-QFN1720-12 (Type CJ)	(Note 7)	—	65	—	
		TSSOP-14		—	72	—	
		V-QFN3535-14 (Type CJ)		—	34	—	

Note: 7. Test condition for the package type(s): device mounted on JEDEC standard PCB per JESD51, with minimum recommended pad layout.

Ordering Information (Notes 8 & 9)



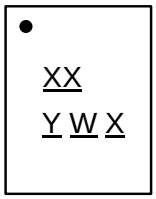
Part Number	Part Number Suffix	Package Code	Package	Packing (Note 10)	
				Qty.	Carrier
LSF0204ZMJ12-7	-7	ZMJ12	U-QFN1720-12 (Type CJ)	3,000	7" Tape and Reel
LSF0204ZB14-13	-13	ZB14	V-QFN3535-14 (Type CJ)	5,000	13" Tape and Reel
LSF0204T14-13	-13	T14	TSSOP-14	2,500	13" Tape and Reel

Notes:
8. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.
9. Pad layout as shown in Diodes Incorporated's package outline PDFs, which can be found on our website at http://www.diodes.com/package-outlines.html.
10. The taping orientation is located on our website at https://www.diodes.com/assets/Packaging-Support-Docs/ap02007.pdf.

Marking Information

(1) U-QFN1720-12 (Type CJ)

(Top View)

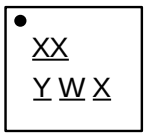


XX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Part Number	Package	Identification Code
LSF0204ZMJ12-7	U-QFN1720-12 (Type CJ)	J2

(2) V-QFN3535-14 (Type CJ)

(Top View)

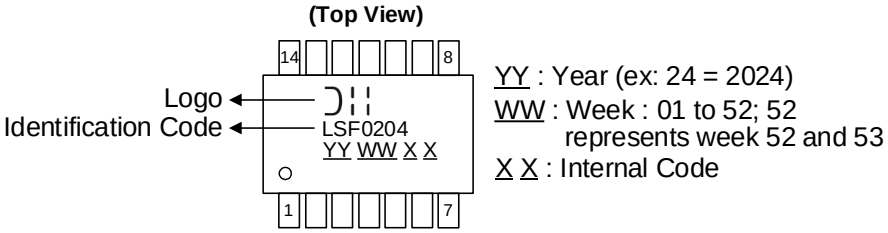


XX : Identification Code
Y : Year : 0 to 9 (ex: 4 = 2024)
W : Week : A to Z : week 1 to 26;
a to z : week 27 to 52; z represents week 52 and 53
X : Internal Code

Part Number	Package	Identification Code
LSF0204ZB14-13	V-QFN3535-14 (Type CJ)	JE

Marking Information (continued)

(3) TSSOP-14

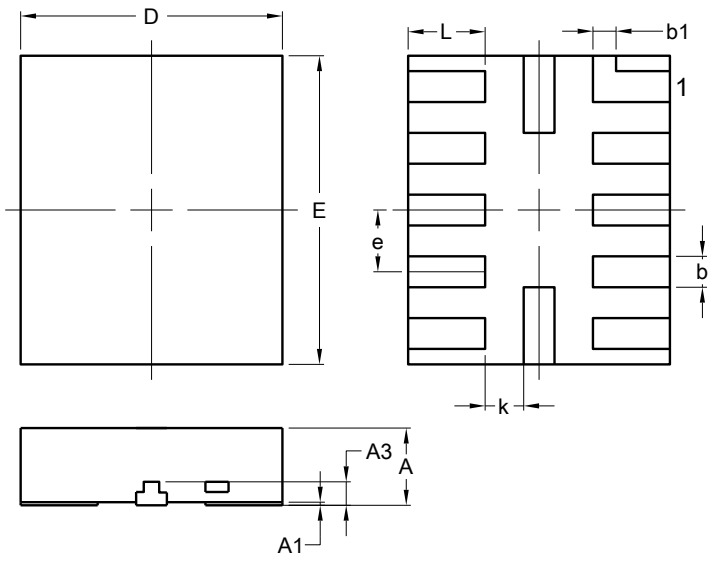


Part Number	Package	Identification Code
LSF0204T14-13	TSSOP-14	LSF0204

Package Outline Dimensions

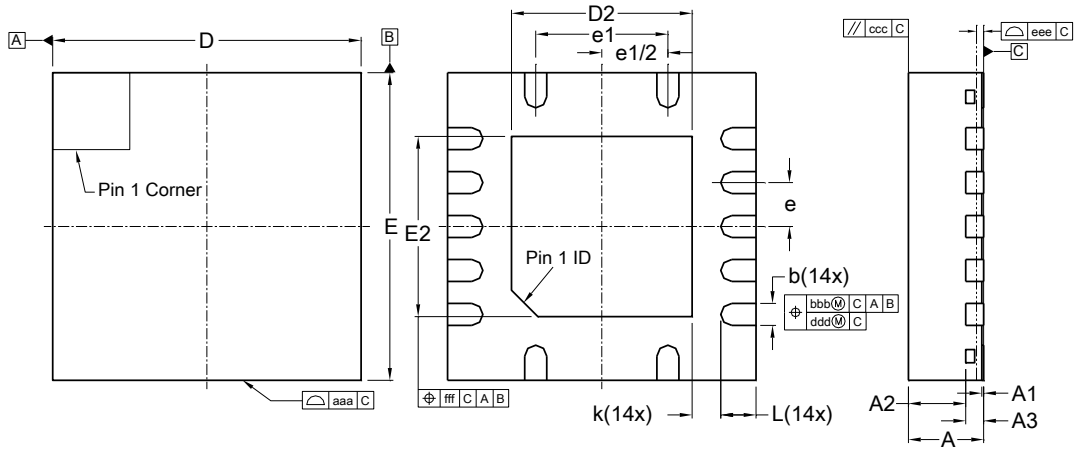
Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) U-QFN1720-12 (Type CJ)



U-QFN1720-12 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	0.450	0.550	--
A1	0.00	0.050	--
A3	0.152 REF		
b	0.150	0.250	--
b1	0.150 REF		
D	1.600	1.800	--
E	1.900	2.100	--
e	0.400 BSC		
k	0.250 REF		
L	0.400	0.600	--
All Dimensions in mm			

(2) V-QFN3535-14 (Type CJ)

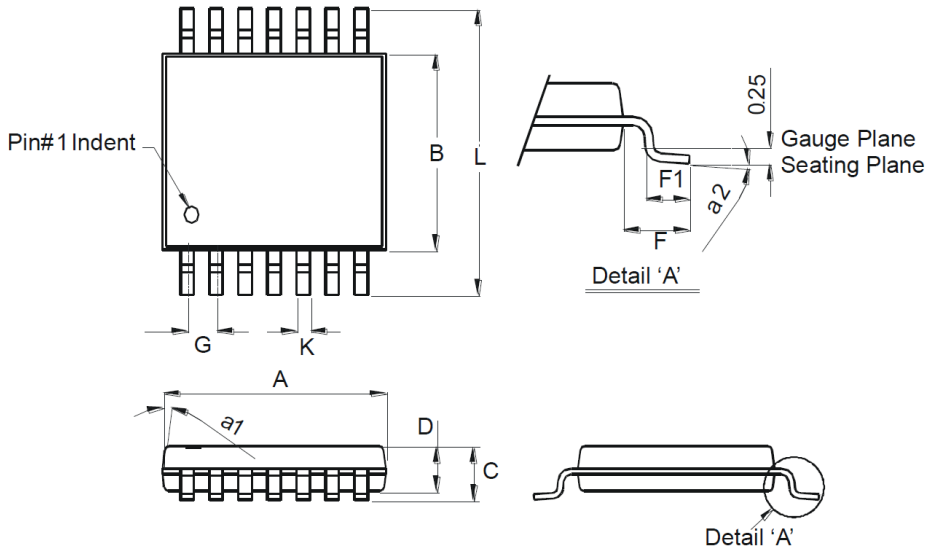


V-QFN3535-14 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	0.80	0.90	0.85
A1	0.00	0.05	0.02
A2	--	--	0.65
A3	0.203 REF		
b	0.20	0.30	0.25
D	3.50 BSC		
D2	1.95	2.15	2.05
E	3.50 BSC		
E2	1.95	2.15	2.05
e	0.50 BSC		
e1	1.50 BSC		
L	0.30	0.50	0.40
k	0.325 REF		
aaa	0.1		
bbb	0.1		
ccc	0.1		
ddd	0.05		
eee	0.08		
fff	0.1		
All Dimensions in mm			

Package Outline Dimensions (continued)

Please see http://www.diodes.com/package-outlines.html for the latest version.

(3) TSSOP-14

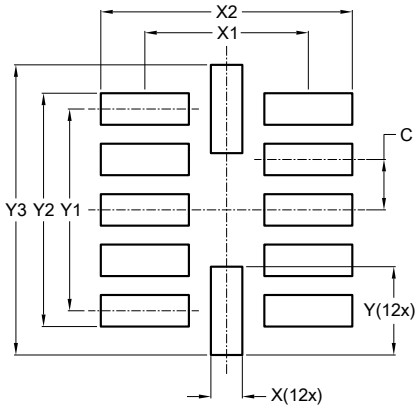


TSSOP-14		
Dim	**Min**	**Max**
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	-	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
All Dimensions in mm		

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

(1) U-QFN1720-12 (Type CJ)

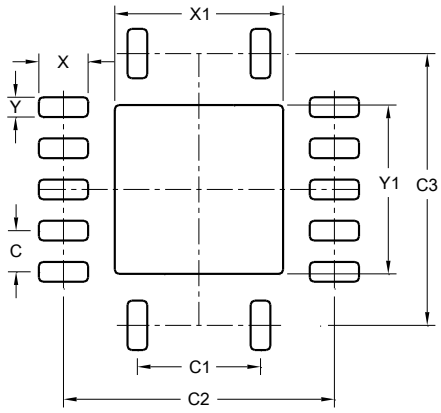


Dimensions	Value (in mm)
C	0.400
X	0.250
X1	1.300
X2	2.000
Y	0.700
Y1	1.600
Y2	1.850
Y3	2.300

Suggested Pad Layout (continued)

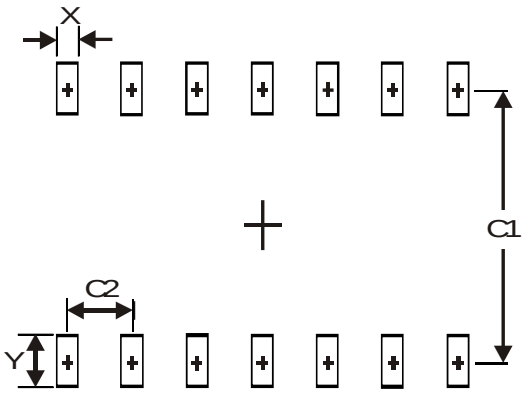
Please see http://www.diodes.com/package-outlines.html for the latest version.

(2) V-QFN3535-14 (Type CJ)



Dimensions	Value (in mm)
C	0.500
C1	1.500
C2	3.300
C3	3.300
X	0.600
X1	2.050
Y	0.240
Y1	2.050

(3) TSSOP-14



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 e3
- Max Soldering Temperature +260°C for 30 secs as per JEDEC J-STD-020
- Weight:
  - U-QFN1720-12 (Type CJ): 21.5mg (Approximate)
  - V-QFN3535-14 (Type CJ): 32.5mg (Approximate)
  - TSSOP-14: 83.5mg (Approximate)

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