Customer: VD

DATE: 11.Dec.2012

SAMSUNG TFT-LCD

MODEL: LSF320HN02-A

(LCD Panel + Driver Ass'y Kit)

The Information described in this specification is for the first draft and can be changed without prior notice

Samsung Display Co., LTD

Contents

The revision history- VD Only

Date	Rev. No	Page	Summary
11. Dec. 2012	00	all	First Issue (First Draft)

General Description

Description

This model uses a liquid crystal display (LCD) of amorphous silicon TFT as switching components. This model is composed of a TFT LCD panel, a driver circuit, and an ass'y KIT of source PBA. This 46.0" model has a resolution of a 1366 x 768 and can display up to 16.7 million colors with the wide viewing angle of 89° or a higher degree in all directions. This panel is designed to support applications by providing a excellent performance function of the flat panel display such as home-alone multimedia TFT-LCD TV and a high definition TV.

General Information

Features

- RoHS compliance (Pb-free)
- High contrast ratio & aperture ratio with the wide color gamut
- SVA mode
- Wide viewing angle (±178°)
- High speed response
- FHD resolution (16:9)
- Low power consumption
- DE (Data enable) mode
- The interface (2pixel/clock) of 2ch LVDS (Low voltage differential signaling)

Items	Specification	Unit	Note
Active Display Area	698.4(H) x 392.85(V)	㎜	
Switching Components	a-Si TFT Active matrix		
Glass Size	TFT : 715.4 (H) x 409.5 (V) CF : 715.4 (H) x 406.9 (V)	mm	±0.4mm
Panel Size	715.4 (H) x 409.5 (V)	mm	±0.4mm
	1.80(D)	mm	±0.1mm
Weight	1200 (max 1320)	g	± 10%
Display Colors	16.7M (True Display) 1.07B (Dithered 10bit)	color	
Number of Pixels	1,920 × 1,080	pixel	16 : 9
Pixel Arrangement	RGB Vertical Stripe		
Display Mode	Normally Black		
Surface Treatment	AG-POL(Anti-Glare),		
Haze	Haze 2.3%		± 2.1%
Hardness	Hard coating 2H		

1. Absolute Maximum Ratings

If the figures on measuring instruments exceed maximum ratings, it can cause the malfunction or the unrecoverable damage on the device.

Item	Symbol	Min.	Max.	Unit	Note
Power supply voltage	V_{DD}	10.8	13.2	V	(1)
Temperature for storage	T_{STG}	-20	65	℃	(2),(4)
Temperature of glass surface	T_{OPR2}	0	65	℃	(2)
Operating temperature	T_{OPR}	0	50	℃	(2),(5)
Humidity for storage	H_{STG}	5	95	%RH	(2),(4)
Operating humidity	H_{OPR}	20	95	%RG	(2),(5)
Endurance on static electricity			150	V	(3)

Note (1) The power supply voltage at Ta= 25 ± 2 °C

(2) Temperature and the range of relative humidity are shown in the figure below.

- a. 95 % RH Max. (Ta ≤ 39 °C)
- b. The relative humidity is 95% or less. (Ta > 39 °C)
- c. No condensation
- d. Operating condition with SET

(3) Keep the static electricity under 150V in Polarizer attaching process.

(4) Operating condition with source PCB

(5) Storage temperature condition including glass

(6) Condition without packing. (Unpacking condition)

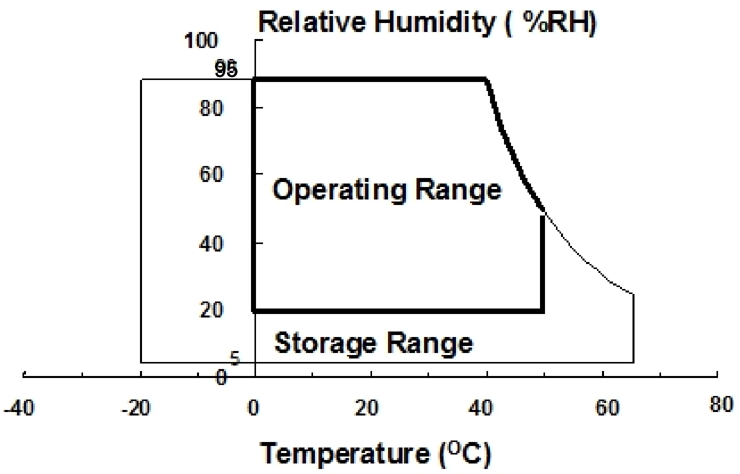


Fig. Range for temperature and relative humidity

2. Optical characteristics

The optical characteristics should be measured in the dark room or the space surrounded by the similar setting.

Measuring equipment : TOPCON RD-80S, TOPCON SR-3 ,ELDIM EZ-Contrast

(Ta = 25 ± 2°C, VDD=12.0V, fv=60Hz, f_{DCLK}=148.5MHz, Light source: D65 Standard light)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Light Source	Note
Contrast ratio (At the center of screen)		C/R		4000	5000	-		Standard	(1) SR-3
Response time	G-to-G	Tg	$T_{PAN,SUR}$ =29.9℃	-	8	16	msec	Standard or VD BLU	(3) RD-80S
Luminance of white (At the center of screen)		Y_L	Normal qL,R=0 qU,D=0 Viewing Angle	250	300	-	cd/m^2	VD BLU	(4) SR-3
Chromaticity (CIE 1931)	Red	Rx		TYP. -0.03	0.640	TYP. +0.03		VD BLU	(5),(6) SR-3
		Ry			0.330				
	Green	Gx			0.300				
		Gy			0.600				
	Blue	Bx			0.150				
		By			0.060				
	White	Wx			0.280				
		Wy			0.290				
sRGB Concordance		-			99		%	VD BLU	(5) SR-3
Color gamut		-		-	72	-	%		
Color		-		-	10,000	-	K		
Viewing Angle	Hor.	q_L	C/R≥10	75	89	-	Degree	Standard or VD BLU	(6) SR-3 EZ-Contrast
		q_R		75	89	-			
	Ver.	q_U		75	89	-			
		q_D		75	89	-			
Brightness uniformity (9 Points)		B_{uni}		-	-	25	%	Standard	(2) SR-3
Transmissivity		T		4.37	4.7	-	%	Standard	(7) D65/SR3
Transmissivity Uniformity		T_{uni}		-	-	10	%	Standard	(8) D65/SR3
Gamma Value		GMA	(@20G~128G)	2.0	2.2	2.4		Standard or VD BLU	(9) SR-3
Gamma variation		Gdiff	(@20G~128G)	-0.14	-	0.14			(11) SR-3
ACC Linearity		ACC_lin		-0.015	-	0.015		Standard or VD BLU	(12) SR-3
5nit Uniformity		Buni_5nit		-30	-	30	%	Standard (38G/255G)	(10) SR-3
White Color Coordinate Uniformity		Wx uni		-	-	0.005		Standard	(13) SR-3
		Wy uni				0.008			

Notice

(a) Setup for test equipment

The measurement should be executed in a stable, windless, and dark room for 40min and 60min after operating the panel at the given temperature for stabilization of the standard light. (SDC uses the standard luminance of the D65 media).

This measurement should be measured at the center of screen.

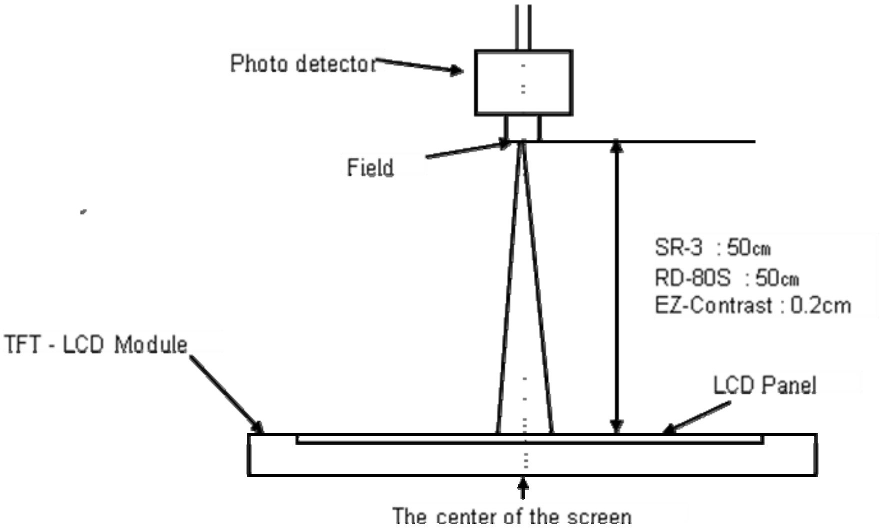
The environment condition: Ta = 25 ± 2 °C

(b) D65 media has the general light source.

The temperature of color is 6847K. The coordinate of color is Wx 0.313, Wy 0.329

The luminance of this product is 7217cd/㎡.

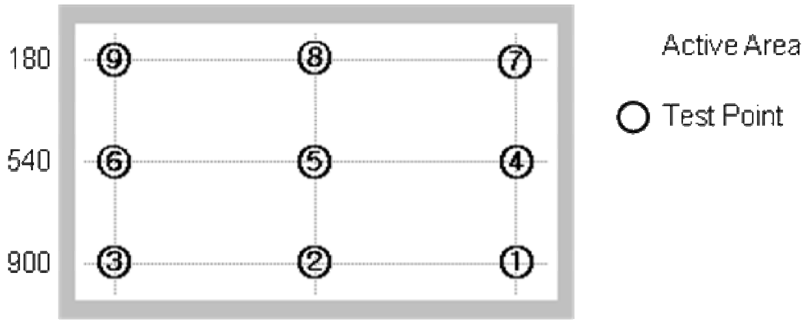
Photo detector	Field
SR-3	2°/1°
RD-80S	1°



(c) The CIE positions D65 as the standard daylight illuminant:

[D65] is intended to represent average daylight and has a correlated color temperature of approximately 6500 K. CIE standard illuminant D65 should be used in all colorimetric calculations requiring representative daylight, unless there are specific reasons for using a different illuminant.

- Definition of the test point



Note (1) Definition of contrast ratio (C/R)

: The ratio of gray max (Gmax) & gray min (Gmin) at the center point ⑤ of the panel

The measurement goes in D65 Standard light source

$$C/R = \frac{G\max}{G\min}$$

Gmax : The luminance with all white pixels

Gmin : The luminance with all black pixels

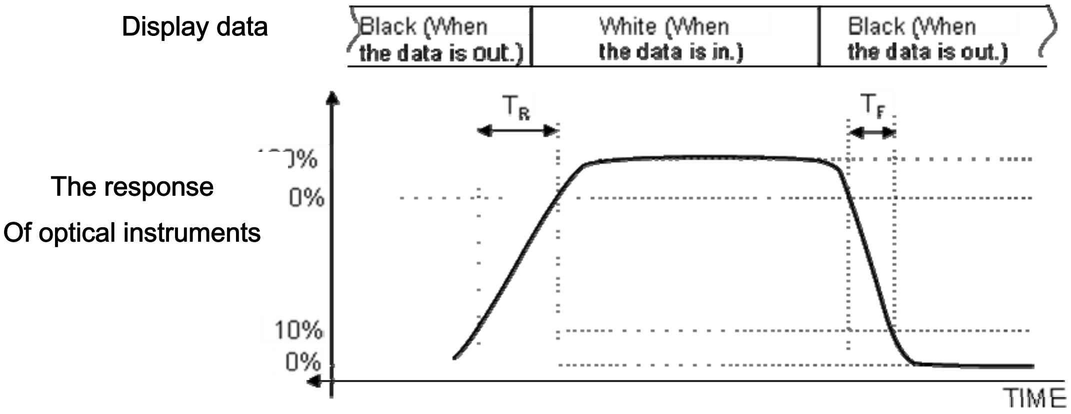
Note (2) Definition of the brightness uniformity of 9 points (Test pattern : The full white)

The measurement shall be executed with the standard light source of D65 .

$$Buni = 100 * \frac{(B\max - B\min)}{B\max}$$

Bmax : The maximum brightness
Bmin : The minimum brightness

Note (3) Definition of the response time : Sum of Tr, Tf



※ G-to-G : Average response time between whole gray scale to whole gray scale.

The response time is the value that was measured after it was operated in Samsung's standard BLU for one hour.(at room temperature)

Note (4) The definition of luminance of white: The luminance of white at the center point ⑤

The measurement shall be executed with the standard light source of D65.

Note (5) The definition of chromaticity (CIE 1931)

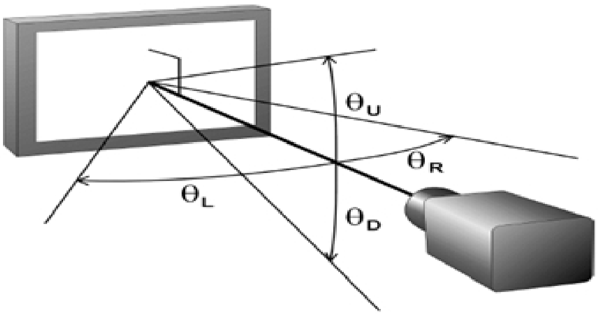
The color coordinate of red, green, blue and white at the center point ⑤

The measurement shall be executed with the standard light source of D65.

Note (6) Definition of viewing angle

: The range of viewing angle (C/R ≥10)

The measurement shall be executed with the standard light source of D65.



Note (7) Definition of transmissivity

The measurement shall be executed with the standard light source of D65.

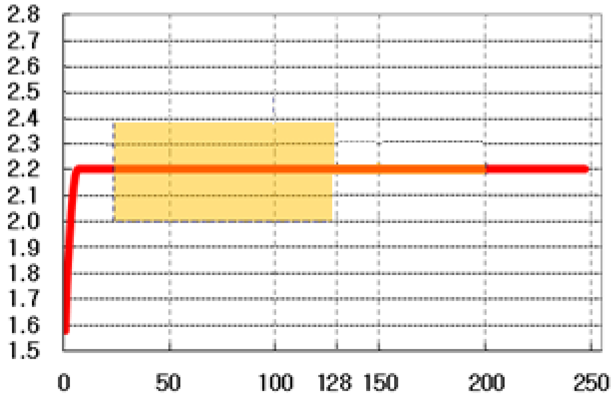
Note (8) Definition of the Transmissivity uniformity of 9 points (Test pattern: The full white)

The measurement shall be executed with the standard light source of D65.

$$Tuni = 100^* \frac{(Tmax - Tmin)}{Tmax}$$

Tmax : The maximum Transmissivity
Tmin : The minimum Transmissivity

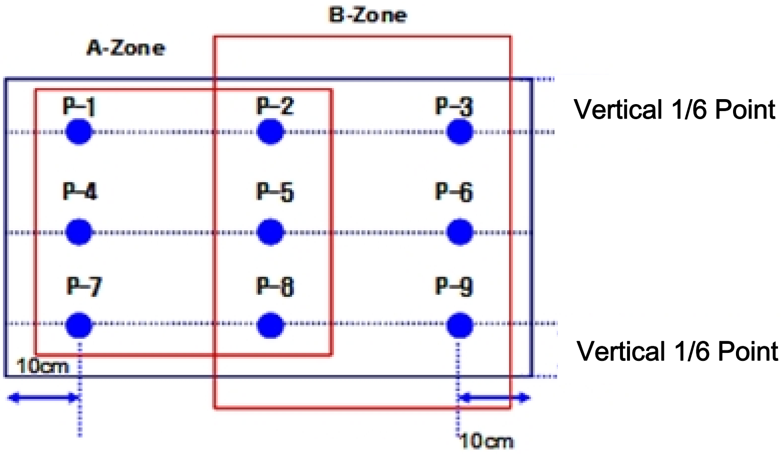
Note (9) Management Criteria of Gamma Value



Gamma Value

- 20 ~ 128Gray : 2.0 ~ 2.4 (Typ. 2.2)

Note (10) 5nit Low Gray Uniformity



[Panel Measure Point]

$$Buni\_5nit = 100^* \frac{(Bmax\_5nit - Bmin\_5nit)}{Bmax\_5nit}$$

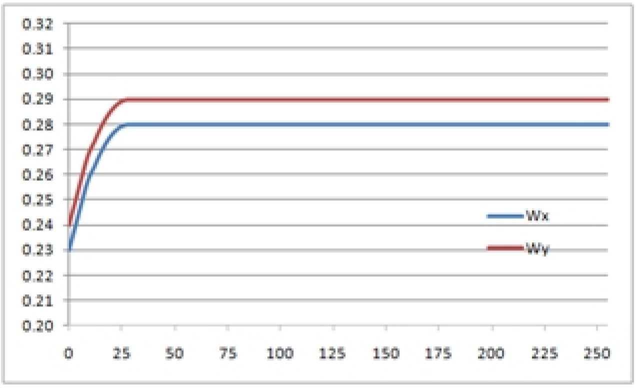
Bmax_5nit : The maximum brightness at 5nit Gray
Bmin_5nit : The minimum brightness at 5nit Gray

Note (11) Gamma Variation between Center and Left (or Right)

Gamma measured at 10cm point from the left & right side is more less than 0.1 than Gamma measured at Center

(Gamma measured at 10cm of the P-4 & P-6 is more less than 0.1 than Gamma measured at P-5)

Note (12) Management Criteria of ACC Linearity



255Gray Wx/Wy value basis (a module unit basis)

a. Color coordinate differences are less than 15/1,000 at Any Point above 30Gray and 255Gray

b. When Wx/Wy coordinates reverse at 0Gray, it permits an once intersection under, 30Gray

Note (13) White Color Coordinate Uniformity of 9 points (Test pattern: The full white)

$$W_{x,\ uni} = W_{x\,max} - W_{x\,min}$$

Wx max : The maximum Wx

Wx min : The minimum Wx

$$W_{y,\ uni} = W_{y\,max} - W_{y\,min}$$

Wy max: The maximum Wy

Wy min: The minimum Wy

3. Electrical characteristics – Sony Model Attached Reference file

3.1 TFT LCD Module

The connector for the display data & timing signal should be connected.

Ta = 25°C ± 2 °C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		Module V_{DD}	10.8	12.0	13.2	V	(1)
Current of Power Supply	(a) Black	I_{DD}	-	**420**	**700**	mA	(2),(3) (Without Inverter) Column Driving
	(b) White		-	**360**	**700**	mA	
	(d) Sub_V_Stripe		-	**650**	**1000**	mA	
Vsync Frequency		f_V	47	60	63	Hz	
Hsync Frequency		f_H	50	67.5	75	kHz	
Main Frequency		f_{DCLK}	130	148.5	160	MHz	
Rush Current		I_{RUSH}	-	-	4	A	(4)

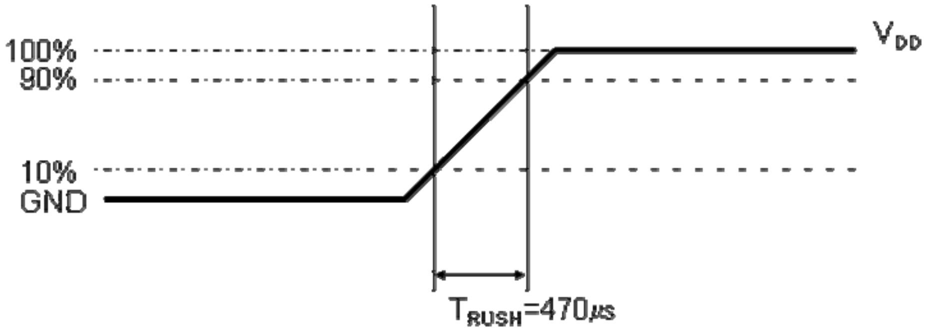
Note (1) The ripple voltage should be controlled fewer than 10% of V_{DD} (Typ.) voltage.

(2) fV=60Hz, fDCLK =148.5MHz, V_{DD} = 12.0V, DC Current.

(3) Power dissipation check pattern (LCD Module only)

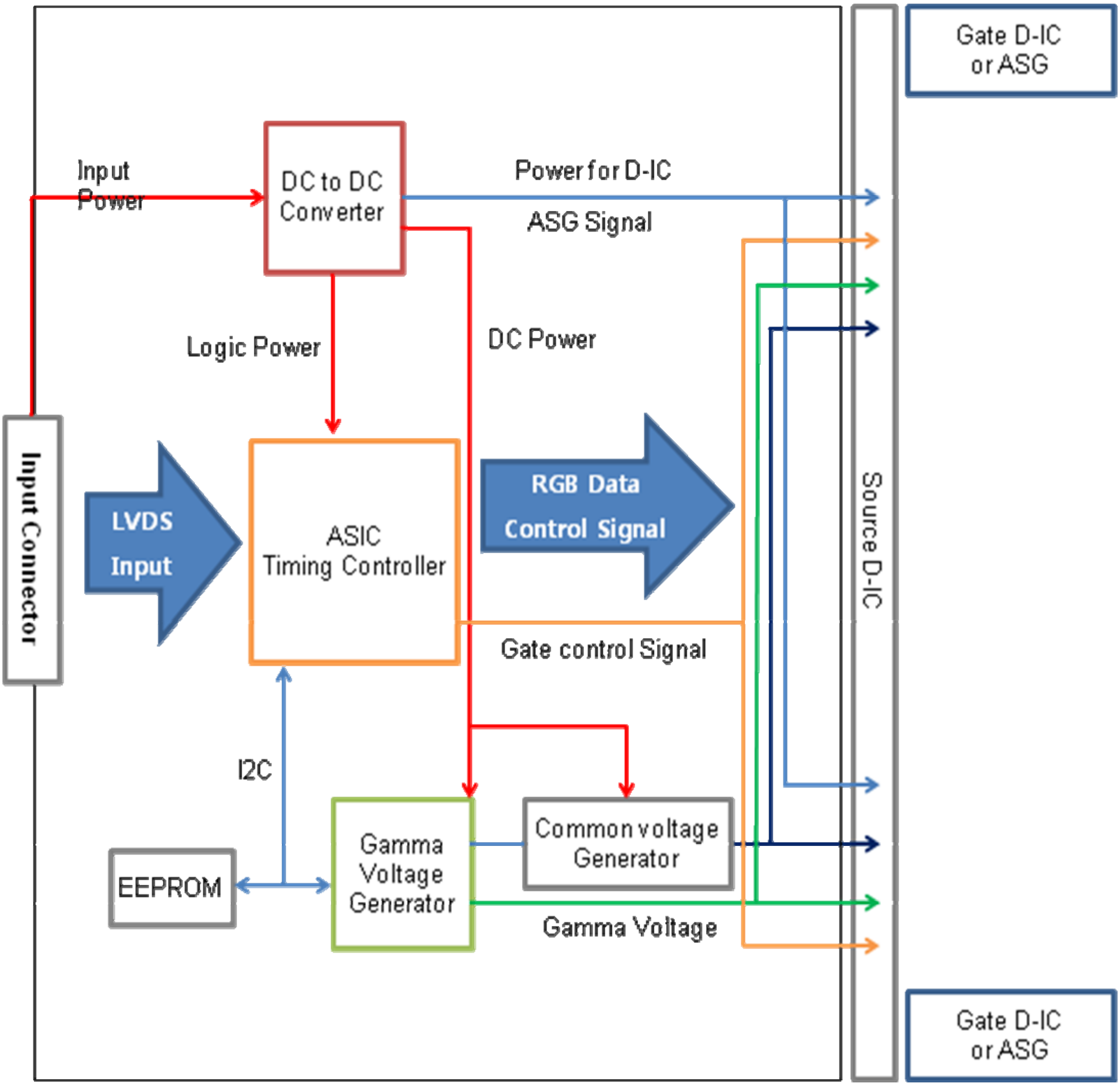
a) Black pattern b) White pattern c) Sub V-stripe

(4) Conditions for measurement



The rush current, I_{RUSH} can be measured during T_{RUSH} is 470us

4. Block diagram



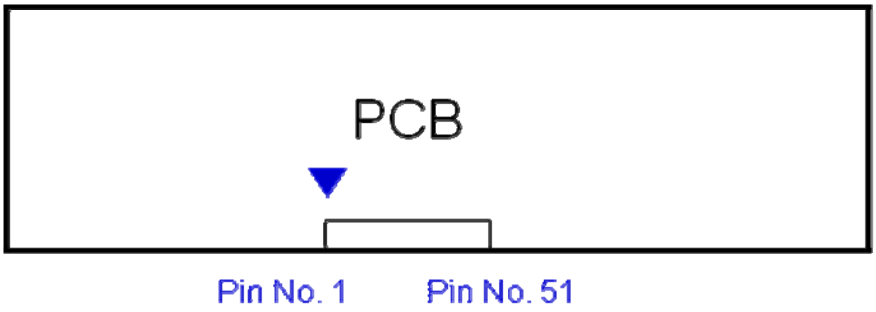
5. The Pin assignment in the input terminal

5.1. Input signal & power

Connector : **FI-RE51S-HF (JAE)**

No		No	
1	DC power supply V_{DD}(+12[V])	26	Even LVDS Signal +
2	DC power supply V_{DD}(+12[V])	27	Even LVDS Signal −
3	DC power supply V_{DD}(+12[V])	28	Even LVDS Signal +
4	DC power supply V_{DD}(+12[V])	29	Even LVDS Signal −
5	DC power supply V_{DD}(+12[V])	30	Even LVDS Signal +
6	Not Connected *	31	GND
7	GND	32	Even LVDS Clock −
8	GND	33	Even LVDS Clock +
9	GND	34	GND
10	Odd LVDS Signal −	35	Even LVDS Signal −
11	Odd LVDS Signal +	36	Even LVDS Signal +
12	Odd LVDS Signal −	37	Not Connected *
13	Odd LVDS Signal +	38	Not Connected *
14	Odd LVDS Signal −	39	GND
15	Odd LVDS Signal +	40	SCL_I
16	GND	41	SDA_I
17	Odd LVDS Clock −	42	Not Connected *
18	Odd LVDS Clock +	43	B_INT
19	GND	44	SDA_I
20	Odd LVDS Signal −	45	LVDS_SEL
21	Odd LVDS Signal +	46	Not Connected
22	Odd LVDS Signal −	47	Not Connected
23	Odd LVDS Signal +	48	Not Connected
24	GND	49	Not Connected
25	Even LVDS Signal −	50	Not Connected
		51	Not Connected

Note (1) Pin number which starts from the left side.



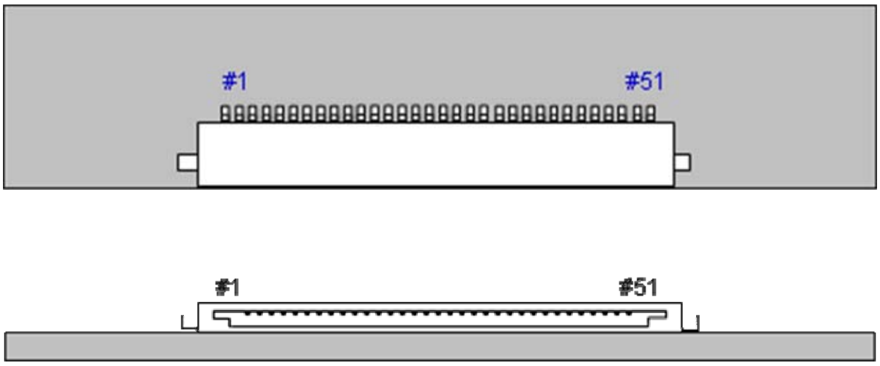


Fig . The diagram of connector

a. Power GND pins should be connected to the LCD’s metal chassis.

b. All power input pins should be connected together.

c. All NC pins should be separated from other signal or power.

Note(2) LVDS OPTION : IF THIS PIN : LOW (GND V)/ NC → JEIDA LVDS FORMAT
OTHERWISE : HIGH (3.3V) → NORMAL NS LVDS FORMAT

Note(3) AGING ENABLE PIN / IF THIS PIN GND → BIST MODE (ROLLING PATTERN IS OPERATED)

5.2 LVDS Interface

- LVDS receiver : T-con (merged) (8Bit)
- Data format

	LVDS pin	JEIDA -DATA	Normal-DATA
TxOUT/RxIN0	TxIN/RxOUT0	R2	R0
	TxIN/RxOUT1	R3	R1
	TxIN/RxOUT2	R4	R2
	TxIN/RxOUT3	R5	R3
	TxIN/RxOUT4	R6	R4
	TxIN/RxOUT6	R7	R5
	TxIN/RxOUT7	G2	G0
TxOUT/RxIN1	TxIN/RxOUT8	G3	G1
	TxIN/RxOUT9	G4	G2
	TxIN/RxOUT12	G5	G3
	TxIN/RxOUT13	G6	G4
	TxIN/RxOUT14	G7	G5
	TxIN/RxOUT15	B2	B0
	TxIN/RxOUT18	B3	B1
TxOUT/RxIN2	TxIN/RxOUT19	B4	B2
	TxIN/RxOUT20	B5	B3
	TxIN/RxOUT21	B6	B4
	TxIN/RxOUT22	B7	B5
	TxIN/RxOUT24	HSYNC	HSYNC
	TxIN/RxOUT25	VSYNC	VSYNC
	TxIN/RxOUT26	DEN	DE
TxOUT/RxIN3	TxIN/RxOUT27	R0	R6
	TxIN/RxOUT5	R1	R7
	TxIN/RxOUT10	G0	G6
	TxIN/RxOUT11	G1	G7
	TxIN/RxOUT16	B0	B6
	TxIN/RxOUT17	B1	B7
	TxIN/RxOUT23	RESERVED	RESERVED

5.3 Input signals, basic display colors and the gray scale of each color. (8bit))

COLOR	DISPLAY (8bit)	DATA SIGNAL																								GRAY SCALE LEVEL
		RED								GREEN								BLUE								
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑ ↓ LIGHT	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			R3~ R252
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R253
		0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R254
	RED	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R255
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑ ↓ LIGHT	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			G3~ G252
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G253
		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G254
	GREEN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	G255
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑ ↓ LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	B2
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			B3~ B252
		:	:	:	:	:	:			:	:	:	:	:	:			:	:	:	:	:	:			
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	B253
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	B254
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	B255

Note) The definition of gray :

Rn : Red gray, Gn : Green gray, Bn : Blue gray (n = Gray level)

Input signal : 0 = Low level voltage, 1 = High level voltage

5.4 LVDS receiver : T-con (merged) (8Bit)

- Data format

	LVDS pin	JEIDA -DATA	Normal -DATA
TxOUT/RxIN0	TxIN/RxOUT0	R2	R0
	TxIN/RxOUT1	R3	R1
	TxIN/RxOUT2	R4	R2
	TxIN/RxOUT3	R5	R3
	TxIN/RxOUT4	R6	R4
	TxIN/RxOUT6	R7	R5
	TxIN/RxOUT7	G2	G0
TxOUT/RxIN1	TxIN/RxOUT8	G3	G1
	TxIN/RxOUT9	G4	G2
	TxIN/RxOUT12	G5	G3
	TxIN/RxOUT13	G6	G4
	TxIN/RxOUT14	G7	G5
	TxIN/RxOUT15	B2	B0
	TxIN/RxOUT18	B3	B1
TxOUT/RxIN2	TxIN/RxOUT19	B4	B2
	TxIN/RxOUT20	B5	B3
	TxIN/RxOUT21	B6	B4
	TxIN/RxOUT22	B7	B5
	TxIN/RxOUT24	HSYNC	HSYNC
	TxIN/RxOUT25	VSYNC	VSYNC
	TxIN/RxOUT26	DEN	DE
TxOUT/RxIN3	TxIN/RxOUT27	R0	R6
	TxIN/RxOUT5	R1	R7
	TxIN/RxOUT10	G0	G6
	TxIN/RxOUT11	G1	G7
	TxIN/RxOUT16	B0	B6
	TxIN/RxOUT17	B1	B7
	TxIN/RxOUT23	RESERVED	RESERVED
TxOUT/RxIN4(dithered10bit)	TxIN/RxOUT28	R0	R8
	TxIN/RxOUT29	R1	R9
	TxIN/RxOUT30	G0	G8
	TxIN/RxOUT31	G1	G9
	TxIN/RxOUT32	B0	B8
	TxIN/RxOUT33	B1	B9
	TxIN/RxOUT34	RESERVED	RESERVED

5.5 Input signals, basic display colors and the gray scale of each color. (10bit)

COLOR	DISPLAY	DATA SIGNAL																														GRAY SCALE LEVEL
		RED										GREEN										BLUE										
		R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-
	GREEN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-
	CYAN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
	RED	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	MAGENTA	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	-
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	-
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
GRAY SCALE OF RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	DARK ↑	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~ R1020
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1021
		0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1022
	RED	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1023
GRAY SCALE OF GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G1
		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~ G1020
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1021
		0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1022
	GREEN	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	G1023
GRAY SCALE OF BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	DARK ↑	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	B1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	B2
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~ B1020
		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓ LIGHT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	B1021
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	B1022
	BLUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	B1023

Note) The definition of gray :

Rn : Red gray, Gn : Green gray, Bn : Blue gray (n = Gray level)

Input signal : 0 = Low level voltage, 1 = High level voltage

6. Interface timing

6.1 The parameters of timing (Only DE mode)

SIGNAL	ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Clock	Frequency Cycle	1/TC	130	148.5	160	MHz	
Vsync		Fh	50	67.5	75	KHz	
Hsync		Fv	47	60	63	Hz	
Vertical Active Disply Term	Display Period	TVD	--	1080	--	lines	
	Vertical Total	TVB	1092	1125	1158	lines	
Horizontal Active Display Term	Display Period	THD	-	1920	-	clocks	
	Horizontal Total	TH	2090	2200	2350	clocks	

Note) These products don’t have to receive the signal of Hsync & Vsync from the input device.

(1) Key points when testing: TTL controls the signal and the CLK at the input terminal of LVDS Tx of the system.

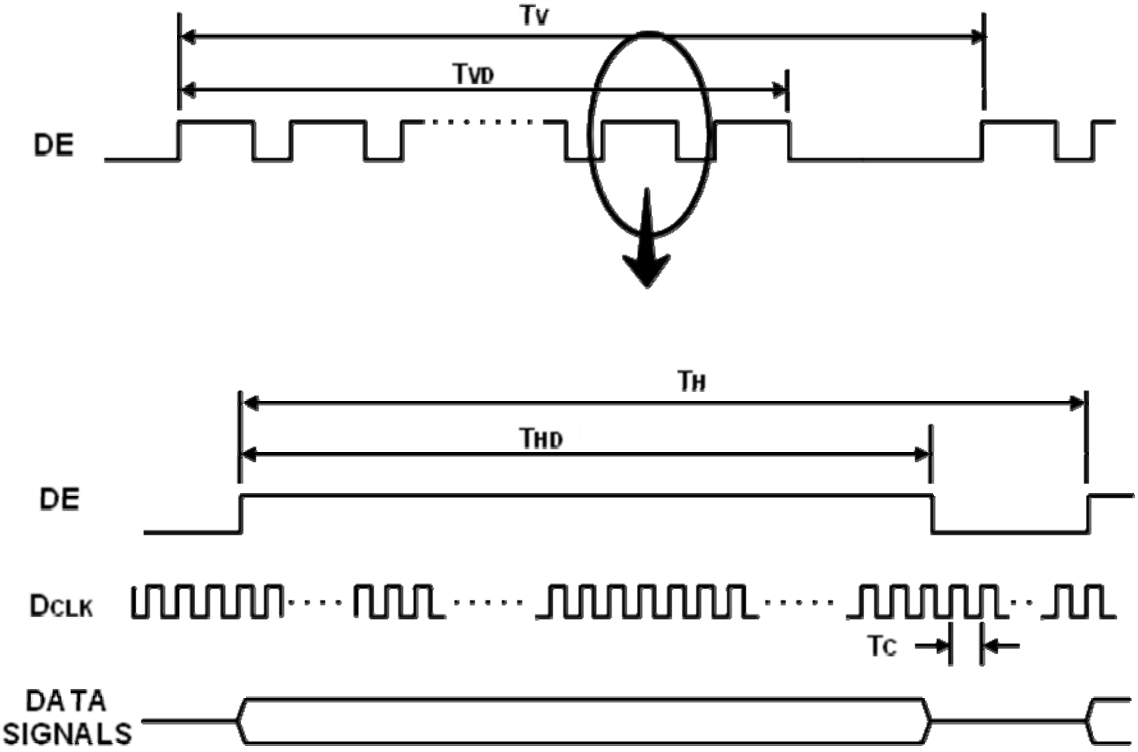
(2) Internal VDD = 3.3V

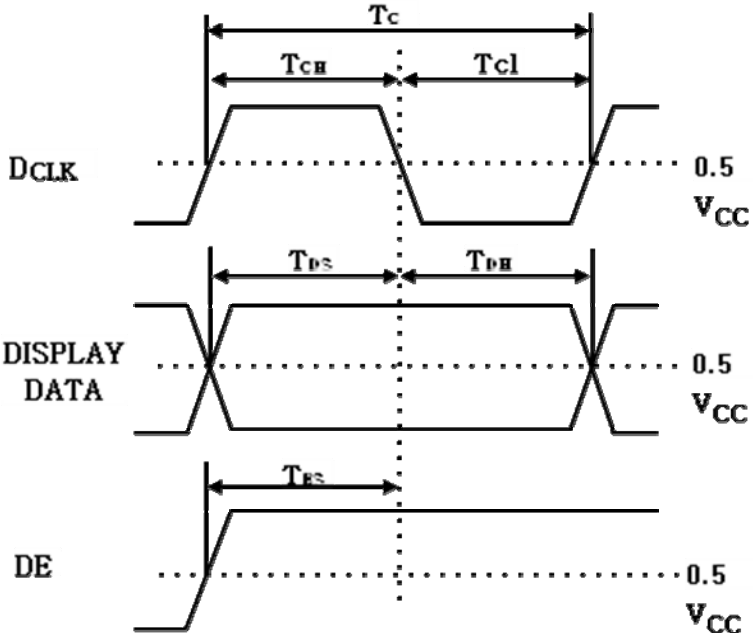
(3) Spread spectrum

- The limit of spread spectrum's range of SET in which the LCD module is assembled should be within ± 3 %.

TxOUT/RxIN4(dithered10bit)	TxIN/RxOUT28	R0	R8
	TxIN/RxOUT29	R1	R9
	TxIN/RxOUT30	G0	G8
	TxIN/RxOUT31	G1	G9
	TxIN/RxOUT32	B0	B8
	TxIN/RxOUT33	B1	B9
	TxIN/RxOUT34	RESERVED	RESERVED

6.2 Timing diagrams of interface signal (Only DE mode)



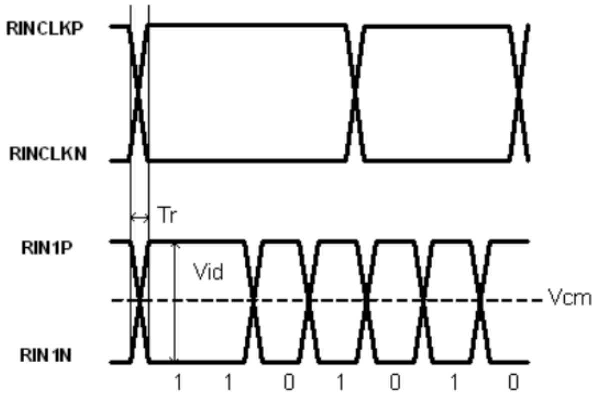


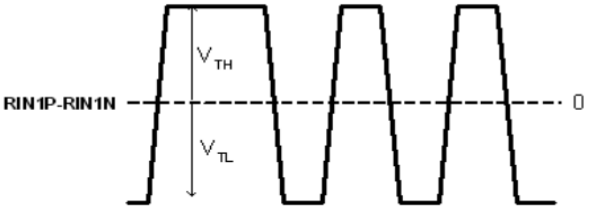
6.3 Characteristics of Input data of LVDS

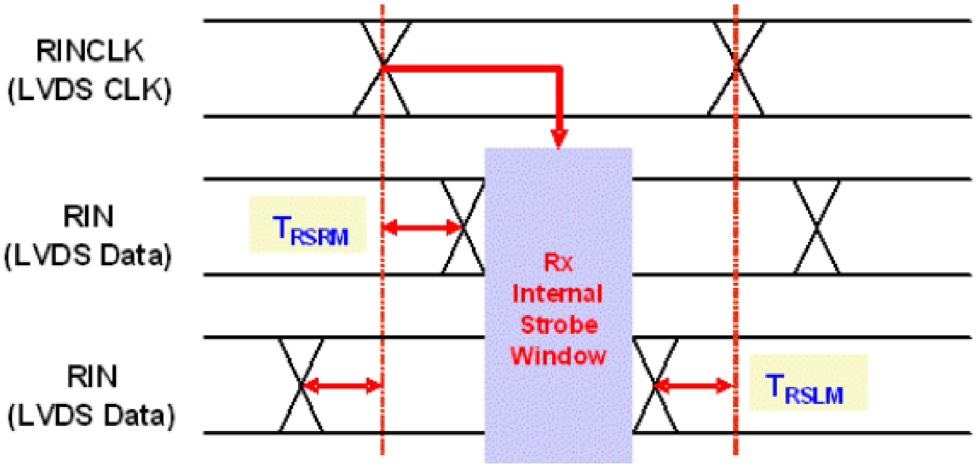
ITEM		SYMBOL	Min.	Typ.	Max.	UNIT	NOTE
Differential input high threshold voltage		VTH	-	-	+100	mV	V_{CM}= 1.2V
Differential input low threshold voltage		VTL	-100	-	-	mV	
Input common mode voltage		V_{CM}	0.2	1.2	2.0	V	-
Differential Input Voltage		$\lvert V_{ID}\rvert$	100	-	600	mV	$\lvert V_{ID}\rvert$=100mV
Input data position	F_{IN}=80MHz	t_{RSRM}	-	-	450	ps	
		t_{RSLM}	-450	-		ps	

Notice The spread spectrum should be 0% when the skew is measured.

Position of a measurement is T-CON LVDS input pin

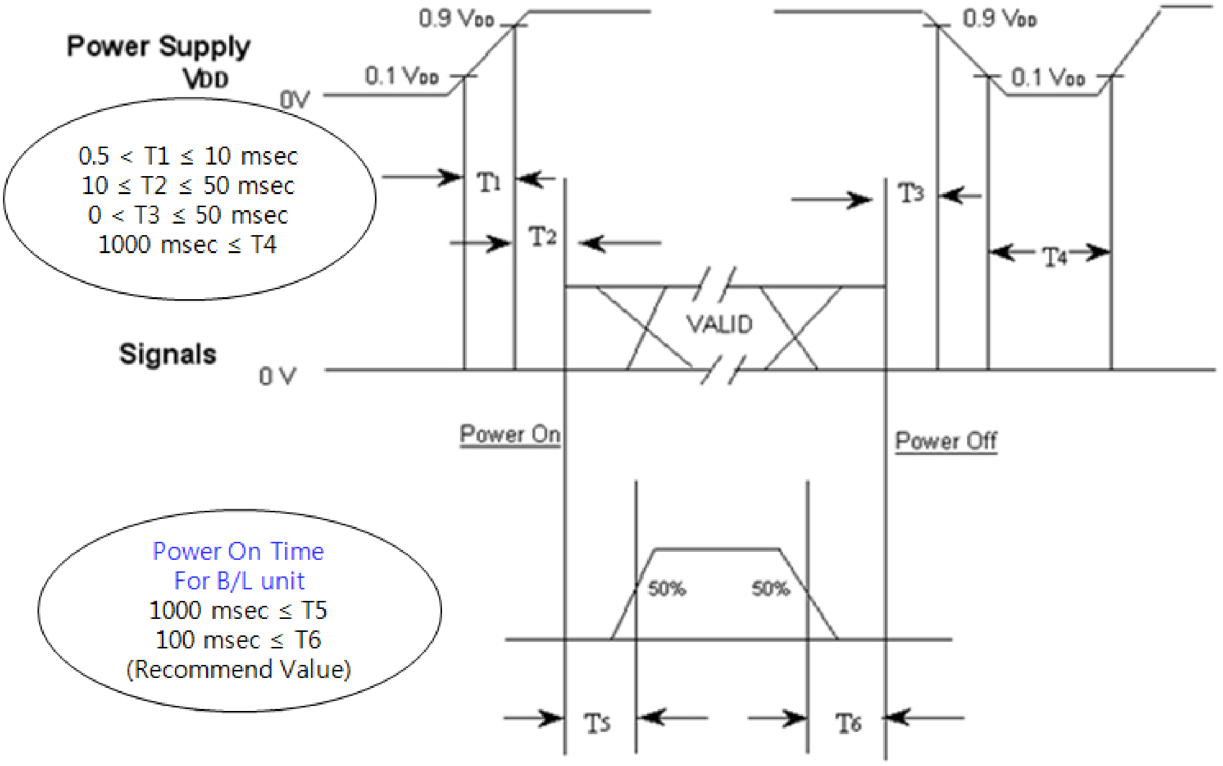






6.4 The sequence of power on and off – Sony Model attached Reference file

To prevent a latch-up phenomena or the DC operation of the LCD Module, the power on/off sequence should be accorded with the settings described in the diagram below.



T1 : The V_{DD} rising time from 10% to 90%

T2 : The time from the point which V_{DD} reach to 90% of voltage to the point which the valid data is out when the power is on.

T3: The time from the point which the valid data is out to the point which V_{DD} reach to the 90% of voltage when the power is off.

T4: the time from the point which the Vdd decrease to the point which the Vdd increase again for windows to restart.

※ The recommended operating condition of the back light system

T5: The time which takes for B/L to be turned on after the signal is entered when the time is on.

T6 : The time which takes until the signal is out after BL is turned off

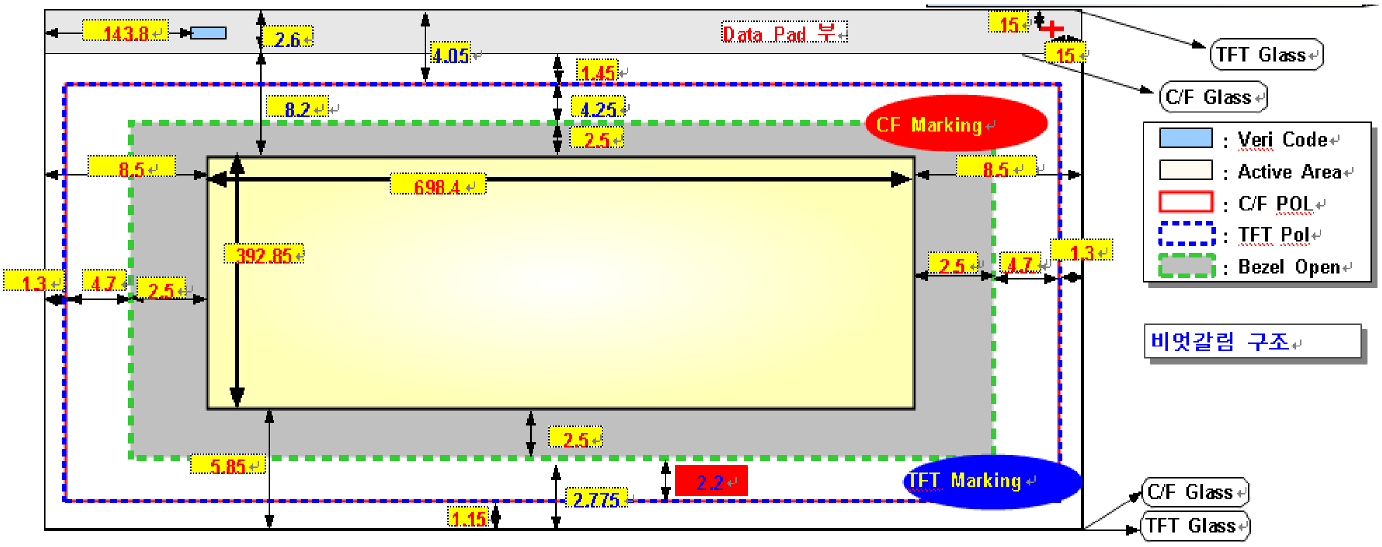
- The condition of supply voltage to enter in the module from the external system should have the same condition as the definition of V_{DD}.

- Apply the voltage for the lamp within the range which the LCD operates. when the back light is turned on before the LCD is operated or when the LCD is turned off before the back light is turned off, the display may show the abnormal screen momentarily.
- While the V_{DD} is off level, please keep the level of input signals low or keep a high impedance condition.
- The figure of T4 should be measured after the module has been fully discharged between the periods when the power is on and off.
- The interface signal must not keep the high impedance condition when the power is on.

7. Outline dimension

7.1 The adhesive size of POL

The next figure shows the size of POL on the drawing sheet attached to the panel for BLU design.



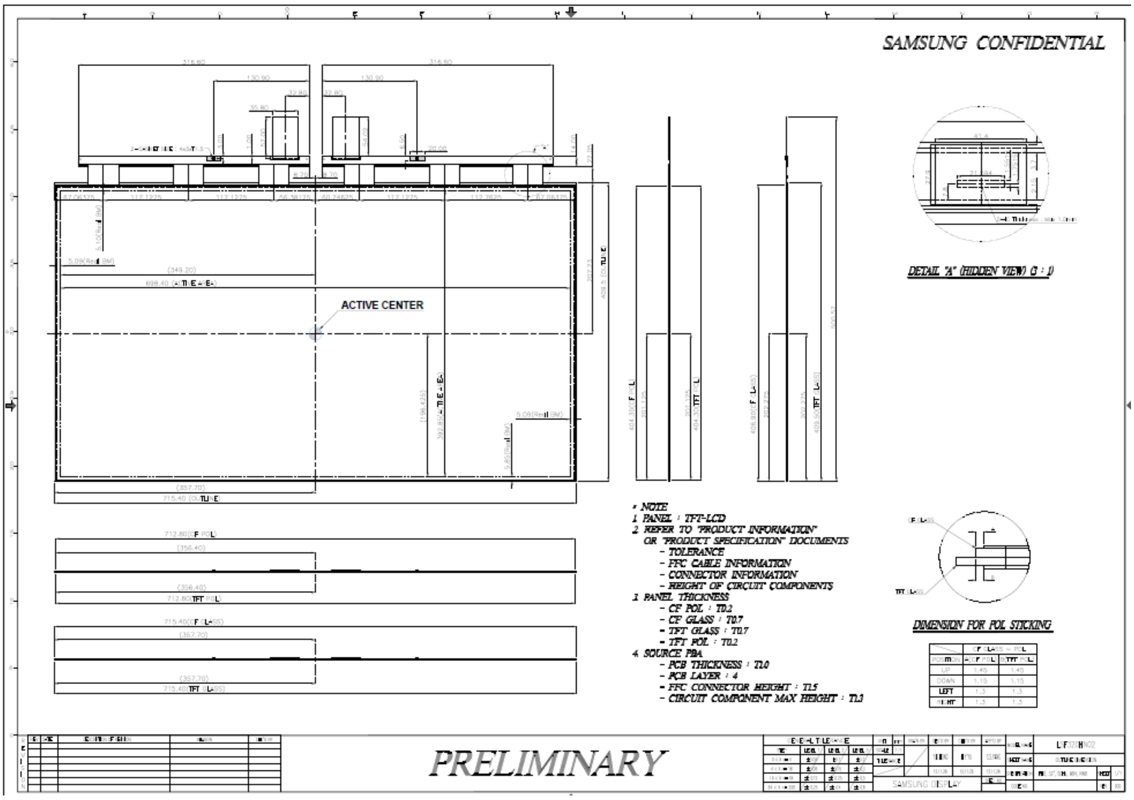
<Figure.>

The POL size of CF : 712.8 X 404.3 ± 0.5mm

The POL size of TFT: 712.8 X 404.3 ± 0.5mm

The total adhesion allowance of POL is ± 1.15㎜

7.2 The drawing sheet for the size of the OLB bonding



8. Reliability test

8.1 Panel

<table>
<tr><th>Item</th><th>Test Condition</th><th>Quantity</th><th>Note</th></tr>
<tr><td>HTOL</td><td>60 ℃ (Panel change 500hr / circuit change 250hr)</td><td>8</td><td></td></tr>
<tr><td>LTOL</td><td>-5 ℃ (Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>THB</td><td>50 ℃ / 90 %RH(Panel change 500hr / circuit change 250hr)</td><td>10</td><td></td></tr>
<tr><td>ASG Low temperature</td><td>Max. frequency 25℃~-40℃</td><td>Each Cell</td><td>ASG Product Only</td></tr>
<tr><td>ASG High Temperature</td><td>Min. frequency 60℃operation 96hr</td><td>Each Cell</td><td>ASG Product Only</td></tr>
<tr><td rowspan="2">Image sticking</td><td>25 ℃ / Mosaic pattern(9*10) 12hrs</td><td rowspan="2">8</td><td rowspan="2"></td></tr>
<tr><td>Rolling pattern 12hrs / 3cycles</td></tr>
<tr><td>Decompression</td><td>-40~50℃, 0m(0ft) ~ 13,700m(45,000ft), 72.5Hr</td><td>4</td><td></td></tr>
<tr><td>HTS</td><td>70 ℃, Storage (Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>LTS</td><td>-25 ℃, Storage(Panel change 500hr / circuit change 250hr)</td><td>4</td><td></td></tr>
<tr><td>Transportation condition</td><td>drop(20cm) → temperature/humidity(-30~60℃ / 40℃ 90%RH) → pressure → vibration(5~200Hz 1.05Grms, 2hr) → drop(20cm)</td><td>1pallet</td><td></td></tr>
<tr><td>WHTS</td><td>60 ℃ / 75 %RH , Storage</td><td>4</td><td></td></tr>
<tr><td>Noise</td><td>Electromagnetic noise: Overall 23dB 이하</td><td>2</td><td></td></tr>
<tr><td>Complex stress</td><td>-20℃~60℃, 0~90%RH, 2cycle</td><td>4</td><td></td></tr>
<tr><td>ESD</td><td>S-IC Input ±7KV, Output ±4KV
Output 은 data TP 에 직접 인가 후 진행
Input 은 CKV,VCOM 등에 FFC CNT 를 통하여 TEST 를 진행</td><td>3</td><td></td></tr>
<tr><td>EOS (optional)</td><td><table>
<tr><th>Item</th><th>Test condition</th></tr>
<tr><td>Vin Input step</td><td>Surge combination (High impedance)
Pass Condition: 5kV under</td></tr>
<tr><td>Signal Input step</td><td>Surge combination (High impedance)
Pass Condition: 120V under</td></tr>
</table></td><td>2</td><td></td></tr>
</table>

[Criteria on evaluation]

There should be no change of the product, which may affect to the practical display functions, when the display quality test is executed under the normal operation setting.

* HTOL/ LTOL : The operating cycle on the high and low temperature

* THB : Temperature humidity slant

* HTS/LTS : The storage at the high and low temperature

* WHTS : The storage in the high temperature with the high humidity

9. General precautions

9.1 Handling

(a) When the panel kit and BLU kit are assembled, the panel kit and BLU kit should be attached to the set system firmly by combining each mounted holes. Be careful not to give the mechanical stress.

(b) Be careful not to give any extra mechanical stress to the panel when designing the set, and BLU kit.

(c) Be cautious not to give any strong mechanical shock and / or any forces to the panel kit. Applying the any forces to the panel may cause the abnormal operation or the damage to the panel kit and the back light unit kit.

(d) Refrain from applying any forces to the source PBA and the drive IC in the process of the handling or installing to the set. If any forces are applied to the products, it may cause damage or a malfunction in the panel kit.

(e) Refrain from applying any forces which cause a constant shock to the back side of panel kit, the set design and BLU kit. If any forces are applied to the products, it may cause an abnormal display, a functional failure and etc.

(f) Note that polarizer could be damaged easily. Do not press or scratch the bare surface with the material which is harder than a HB pencil lead.

(g) Wipe off water droplets or oil immediately. If you leave the droplets for a long time on the product, a staining or the discoloration may occur.

(h) If the surface of the polarizer is dirty, clean it using the absorbent cotton or the soft cloth.

(i) Desirable cleaners are water or IPA (Isopropyl Alcohol). Do not use Kenton type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. These might cause the permanent damage to the polarizer due to chemical reaction.

(j) If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.

(k) Protect the panel kit and BLU Kit out of the static electricity. Otherwise the circuit IC could be damaged.

- Reference : Process control standard of SDC

No.	Item	Control standard
1	Ionizer	All Equipment should be controlled under 150V.(Typ. 100V)
2	Carrying Roller	Carrying Roller should be controlled under 200V.
3	Equipment Ground Resistance	All Equipment Ground Should be less than 1ohm.

(l) Remove the stains with finger-stalls wearing soft gloves in order to keep the display clean in the process of the incoming inspection and the assembly process.

(m) Do not pull or fold the source drive IC which connects to the source PBA and the panel or the gate drive IC.

(n) Do not pull, fold or bend the source drive IC and the gate drive IC in any processes. If not, the source drive IC could be bent one time in the process of assembling the panel Kit and the BLU Kit.

(o) Do not adjust the variable resistor located on the panel kit and BLU kit except when adjusting the flicker.

(p) Do not touch the pins of the interface connector directly with bare hands.

(q) Be cautious not to be peeled off the protection film.

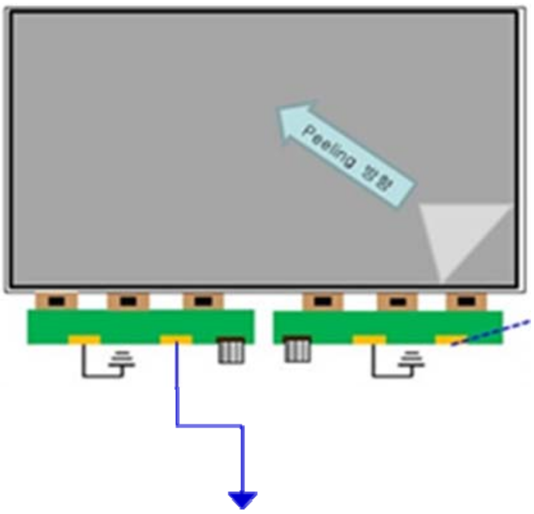


Fig. GND SR-Open Pattern – Be sure to be contacted to the ground while peeling of the protection film

- Make sure to peel off slowly

(It is recommended to peel it off at the speed of more than 8sec. constantly.)

- The peeling direction is shown at the Fig
- Instruct the ground worker to work with the adequate methods such as the antistatic wrist band.
- Maker sure to be grounded the source PBA while peeling of the protection film.
- Ionized air should be blown over during the peeling
- The protection film should not t be contacted to the source drive IC.
- If the adhesive stains remain on the polarizer after the protection film is peeled off, please move stains with isopropyl-alcohol liquid.

(r) The protection film for the polarizer on the panel kit should be slowly peeled off just before using so that the electrostatic charge can be minimized.

(s) The panel kit and BLU kit have high frequency circuits. The sufficient suppression to the EMI should be done by the set manufacturers.

(t) The set of which the panel is assembled shall not be twisted. If the product is twisted, it may cause the damage on the product.

(u) Surface Temp. of IC should be controlled less than 100℃, operating over the Temp. can cause the damage or decrease of lifetime.

9.2 Storage

The storage condition for packing

ITEM	Unit	Min.	Max.
Storage Temperature	(℃)	5	40
Storage Humidity	(%RH)	35	75
Storage life	12 months Based on shipping date at SDC site		
Storage Condition ITEM Storage Temperature	(1) Design the warehouse to be ventilated efficiently with equipping the roof, the ventilation system, and the temp. controller. (2) Don't load the product on the floor and store the product with loaded on the pallet placed far away from the wall. (3) Avoid exposing the product to the direct light, moisture, and water and prevent the product from being condensed. (4) Don't store the product at the container located outside where it rains and the direct light shines. (5) Prevent the product from being exposed to the noxious gas such as the acid gas or alkali gas which may damage the electric device. (6) Don't store the product at the location surrounded by dangerous factors, which can deteriorate the quality of product.		

9.3 Operation

(a) Do not connect or disconnect the FFC cable during the "Power On" condition.

(b) Power supply should be always turned on and off by the "Power on/off sequence"

(c) The module has high frequency circuits. The sufficient suppression to the electromagnetic interference should be done by the system manufacturers. The grounding and shielding methods is important to minimize the interference.

(d) The cables between TV SET connector and Control PBA interface cable should be connected directly to have a minimized length. A longer cable between TV SET connector and Control PBA interface cable maybe operate abnormal display

(e) Recommend to age for over 1 hour at least in the state, which the product is driving initially to stabilize the characteristic of the initial TFT.

(f) Response time depends on the temperature.(In Lower temperature, it becomes longer)

9.4 Operation condition guide

(a) The LCD product shall be operated under normal conditions.
The normal condition is defined as below;

- Temperature : 20±15℃
- Humidity : 55±20%
- Display pattern : continually changing pattern (Not stationary)

(b) If the product will be used under extreme conditions such as under the high temperature, humidity, display patterns or the operation time etc.., it is strongly recommended to contact SDC for the advice about the application of engineering . Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.

9.5 Others

(a) The ultra-violet ray filter is necessary for the outdoor operation.

(b) Avoid the condensation of water which may result in the improper operation of product or the disconnection of electrode.

(c) Do not exceed the limit on the absolute maximum rating. (For example, the supply voltage variation, the input voltage variation, the variation in content of parts and environmental temperature, and so on) If not, panel may be damaged.

(d) If the module keeps displaying the same pattern for a long period of time, the image may be remained to the screen. To avoid the image sticking, it is recommended to use a screen saver.

(e) This Panel has its circuitry of PCB's on the rear side, so it should be handled carefully in order for a force not to be applied.

(f) Please contact the SDC in advance when the same pattern is displayed for a long time

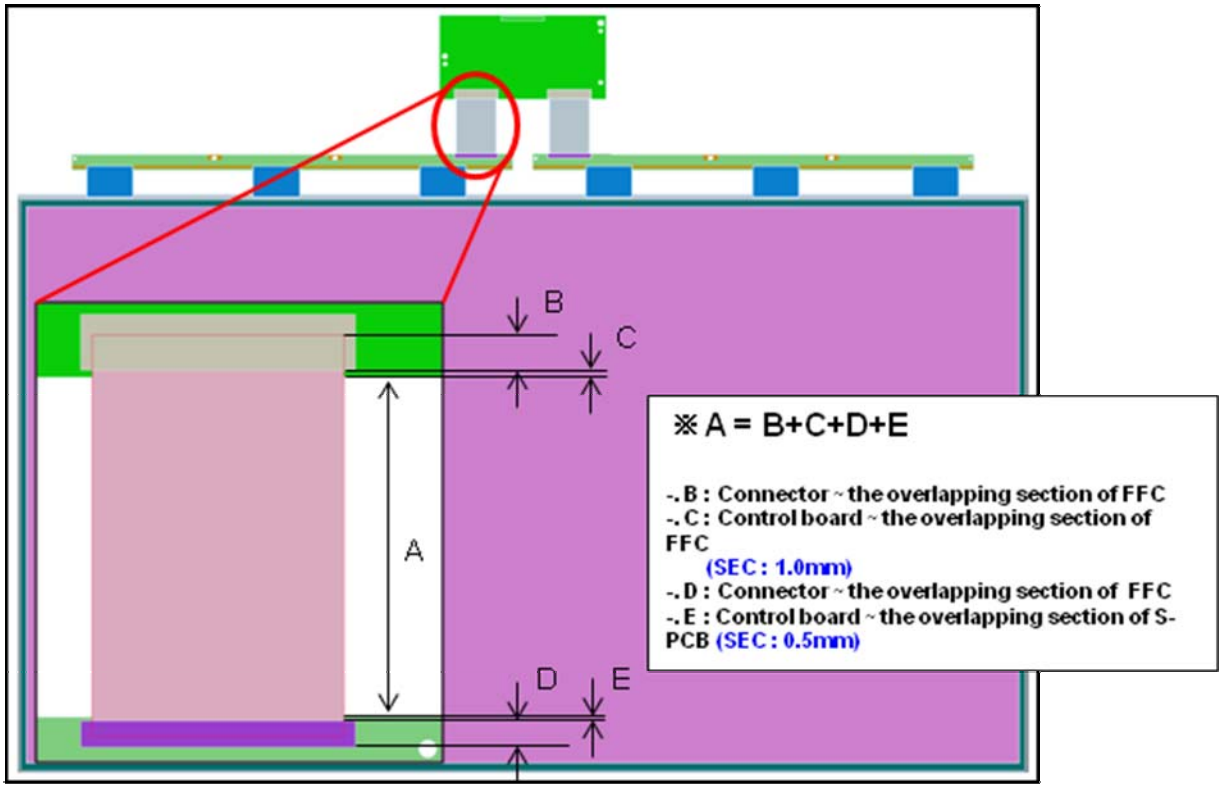
10. Special precautions

10.1 Lists to be cautious when executing the design process

No.	Component	Expected cause
1	Upholding part for panel	Prevent the panel from breaking by assigning gaps between the panel and the upholding part for panel on the drawing for the upholding part for panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
2	The shape of the upholding part for panel	Design the upholding part for panel to fit to the panel appropriately when designing the BLU since the shape of the upholding part for panel may damage the panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
3	The edge of upholding part for panel	Design the edge of panel to have a sufficient space with the upholding part for panel when designing the BLU since the edge of the upholding part for panel may damage the panel when assembling the panel and BLU. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
4	Upholding part for panel	Place the upholding part for the panel in order for the shape of mold, which contacts with the panel not to interfere with the area of panel. Refer to the (a), (b), (c) of 3-1 for the design of BLU.
5	Drive IC	Design the BLU in order for the COF not to contain the lead crack resulted from the tensioned COF created when the product is twisted if the space between the D-IC COF and the middle mold isn't sufficient. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
6	Drive IC	Design the BLU in order for the product not to contain the lead crack resulted from the tensioned COF caused under the condition, which the product is twisted by fixing the source PCB. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
7	IC component	1) The temperature of each part of product suggested by our company and the second vendor shall meet the standard of temperature, which is recommended not to be exceeded by our company when the product is affected under the various temperature ranges. Apply over 1mm long separation distance stated in the safety standard between the electric part and each conductor. (Apply the rated separation distance when insulating.)
8	Thermal pad	Apply the thermal pad in a designated size to the product as a measure to lower the temperature of heat in order for each part to use the rated temperature.
9	POL	The surrounding area of the POL shall be treated with an electrification treatment since the external ESD may cause a phenomenon, which the POL is coming off. In addition, the GND portion of source PBA shall be grounded.
10	PBA	The GND portion of each PBA shall be contacted with the GND portion of BLU. Refer to the (a) and (b) of 3-3 for the design of BLU.
11	Circuit	The standardized approval from the client is required since the EMI is executed by a client. Our company can only measure the reference since the client measures the BLU.
12	The height of component	Design the BLU with considering the maximum height of parts, which our company suggests.
13	Between the FFC and the C-PBA	Design the instrument with considering the length between the FFC and the control PBA. (The marginal minimum length of 5mm or 8mm is required.)
14	Panel	The surface temperature of panel shall be maintained within 0℃ and 45℃ when the external ambient temperature is at 25℃. (Design the BLU with considering the increase of the temperature in the panel by the LED, CCFL, and etc.)
15	Aging	Recommend to age for over 1 hour at least in the state, which the product is driving initially to stabilize the characteristic of the initial TFT.
16	The attachment of gasket	The additional confirmation by our company is required If the attachment of gasket to the S-PBA of our company is required.(To fix the S-PBA or the EMI)
17	Drive IC	Design the top chassis and the driver IC to be contacted by placing the shape of emboss inside the top chassis as a measure to prevent the driver IC from heating. The size of emboss shall be designed in larger size than the size of IC inside the film of the driver IC. Refer to the (a), (b), (c),(d),(e),(f), and (g)of 3-2 for the design of BLU.
18	The prohibited bandwidth	Design the BLU in order for the BLU not to interfere with the area, where the control PBA and the source PBA are located densely according to the drawing for the BLU from our company.
19	S-PBA	The material, which contacts with the bottom side of S-PBA which has a pattern shall be non-conducting material or shall be insulated.

11. Example

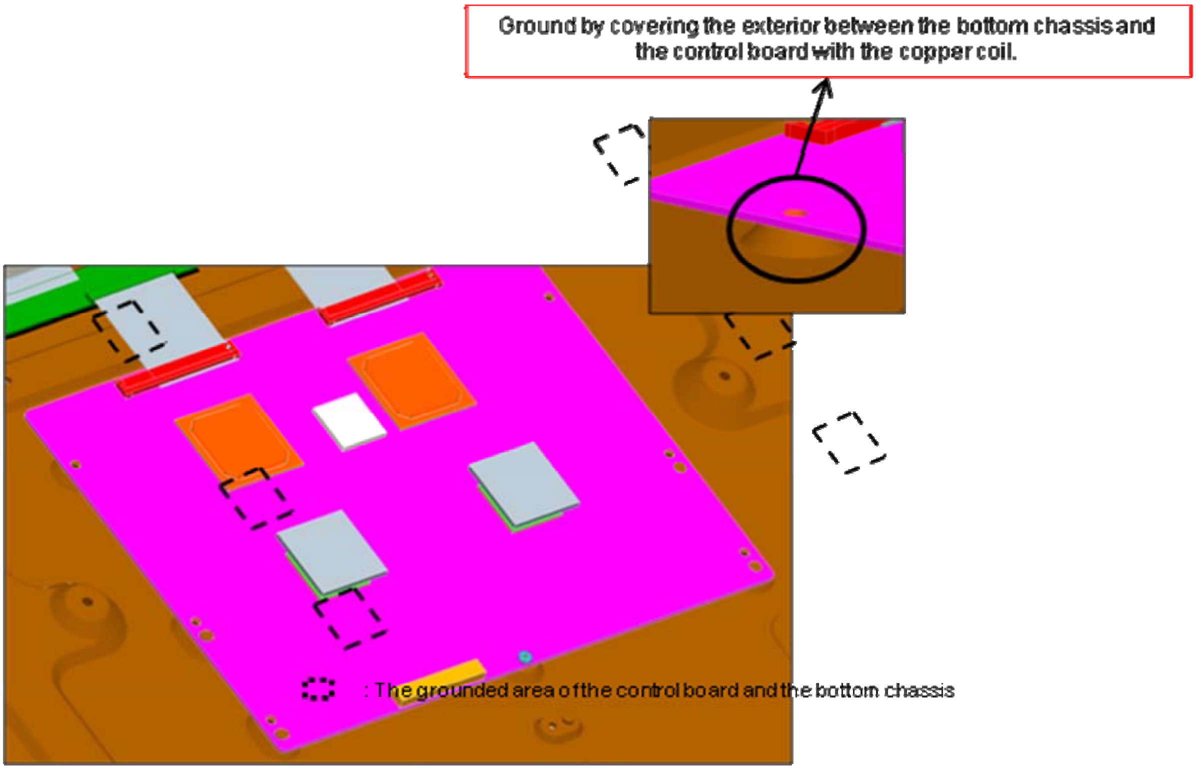
. The length between the FFC and the C-PBA



※ A = B+C+D+E

-. B : Connector ~ the overlapping section of FFC
-. C : Control board ~ the overlapping section of FFC
(SEC : 1.0mm)
-. D : Connector ~ the overlapping section of FFC
-. E : Control board ~ the overlapping section of S-PCB (SEC : 0.5mm)

. The grounding of PCB


Ground by covering the exterior between the bottom chassis and the control board with the copper coil.

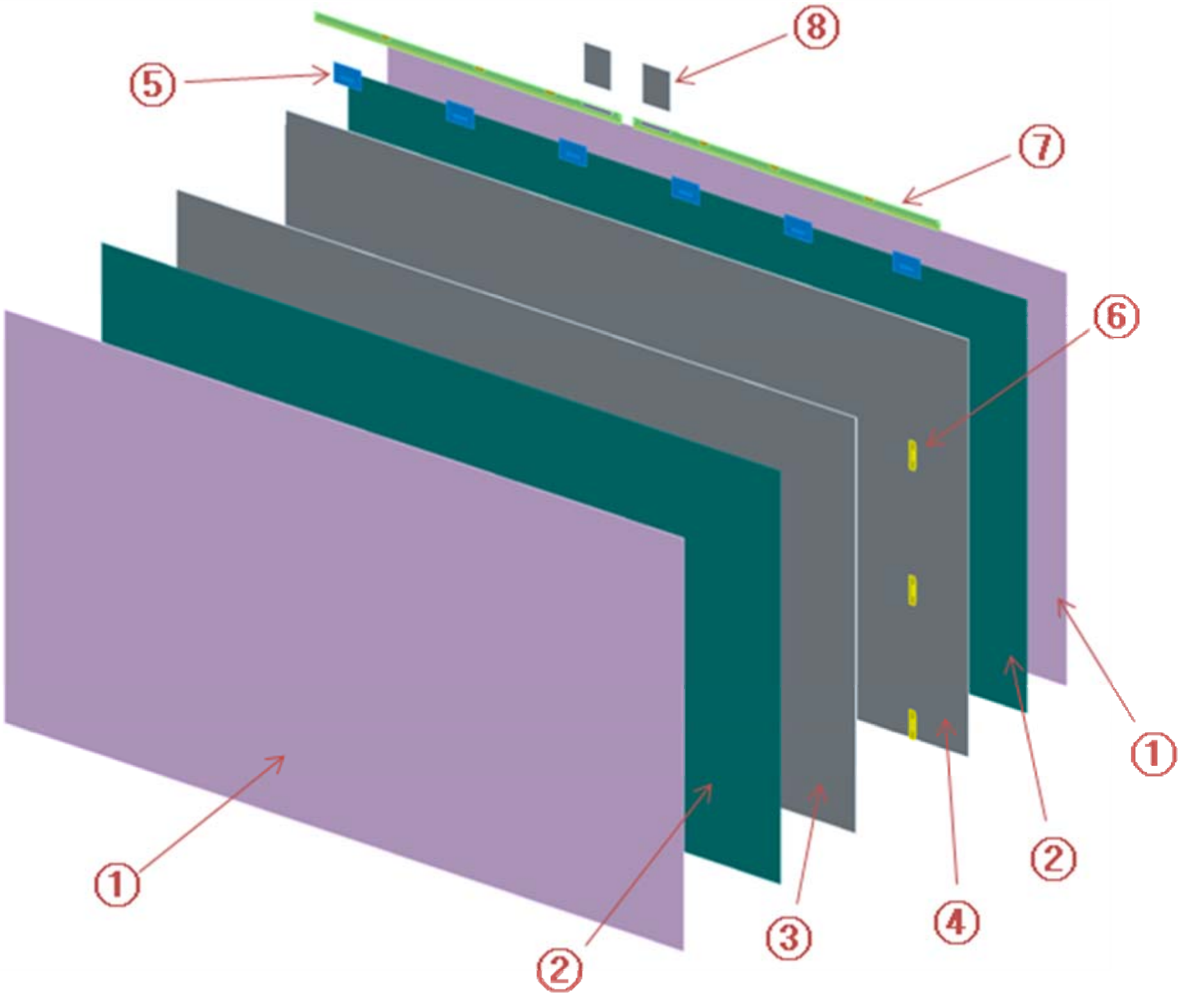
⬚ : The grounded area of the control board and the bottom chassis

Appendix2

Recommendation for the BLU Design

Samsung Display Co., LTD

1. The schematic of panel



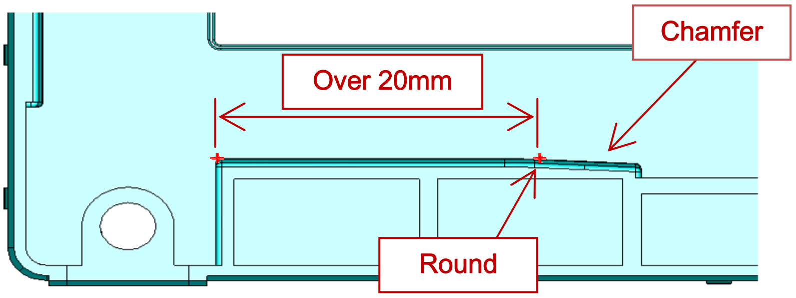
Item	Symbol	Remark
Protector Film	①	Removable
Polaroid Film	②	
Color Filter Glass	③	
TFT Glass	④	
Source IC	⑤	
Gate IC	⑥	
Source PBA	⑦	
FFC	⑧	

2. The guide for the mechanical design

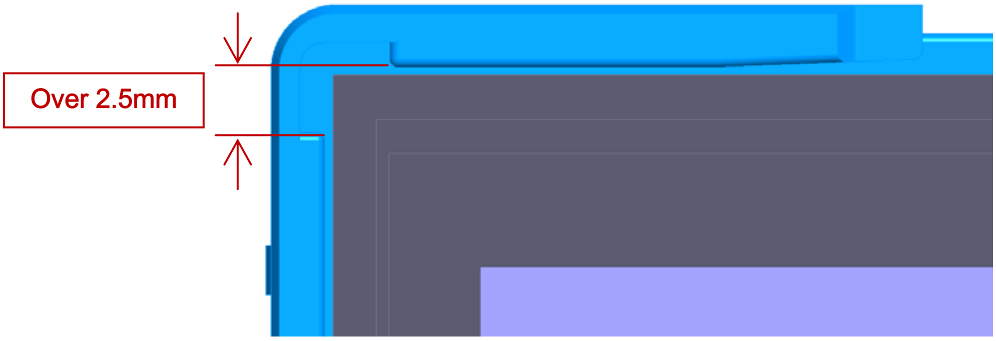
2.1 The panel guide

(a) When the panel guiding part is made of plastic resin, the gap between the panel and the guiding structure should be considered at the design process. The shrinkage of the plastic resin under the temperatures change can cause the light leakage. The gap should be determined to cover the temperature change from the guarantee condition and the BLU structure. SDC recommends the total gap between the panel and the guide structure as below, but the suggested dimension does not guarantee the quality of the products.

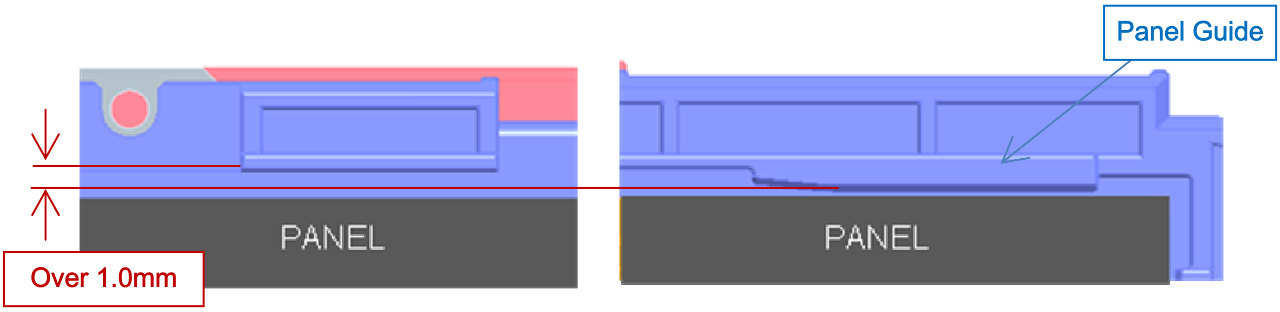
(b) It is recommended to follow the dimension and the shape of the guiding structure illustrated as below since the distortion of the panel can cause the light leakage.



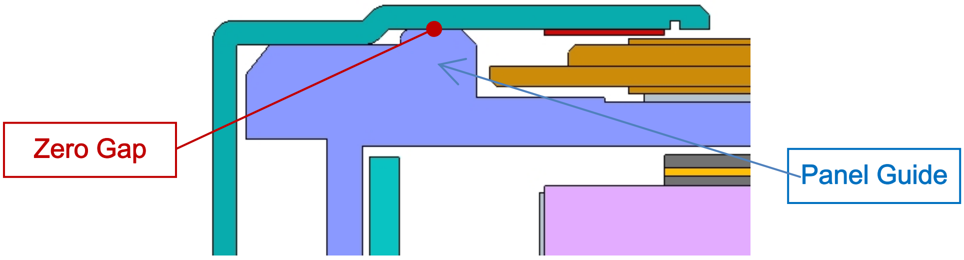
(c) When the panel guide is designed to be located at the corner of the BLU, the edge point of the panel shall not be in contact with the panel guide structures to prevent the crack of the panel caused by the burr at the edge of the glass. The distance larger than 2.5mm as shown in the picture is recommended.
(※ Suggested dimension does not guarantee the quality of the products.)



(d) It is recommended to keep the distance between the panel guides and other ribs over 1mm. If the ribs are placed at the same line with the panel guide, panel broken can be happen when the operator makes the mistake by placing the panel on the top of the ribs.
(※ Suggested dimension does not guarantee the quality of the products.)

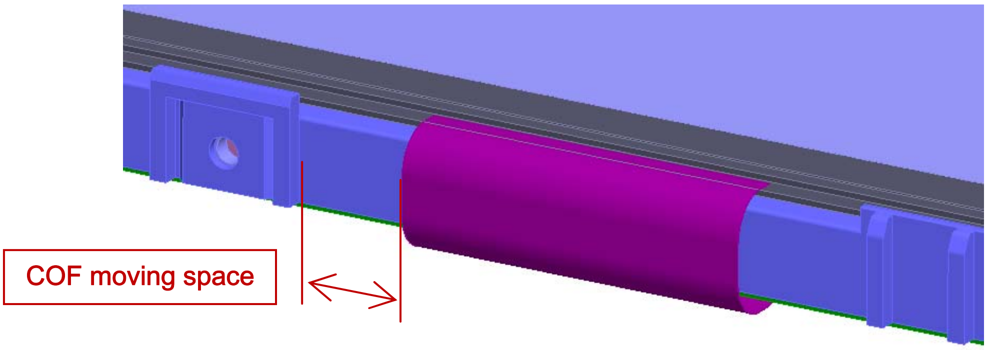


(e) The gap between the panel guide and the front cover (or front chassis) should be zero in z-direction. If there is gap, the panel is easily stuck into the gap and can be broken by external forces.



2.2 The COF and the Drive IC

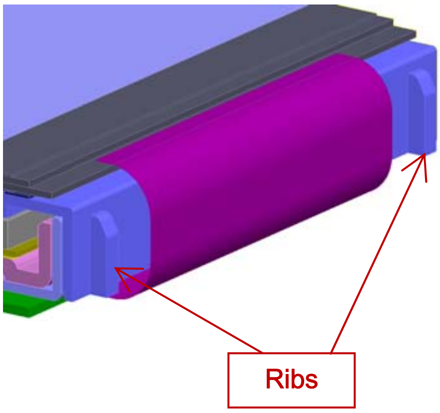
(a) It is recommended to secure sufficient gap between the COF and the other parts, since the lack of gap can cause the damage on the COF such as the lead crack, under the vibration and twist condition.
(※ Over 3.0mm for moving space is recommended, but the suggested dimension does not guarantee the quality of the products.)

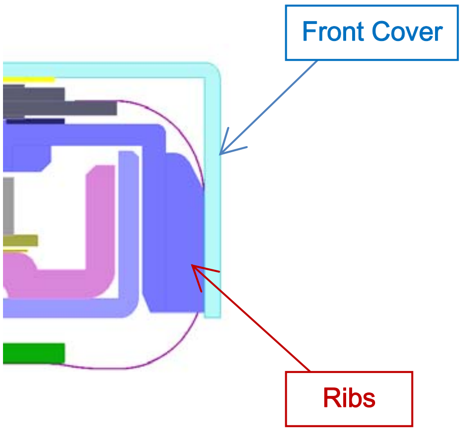


(b) The pattern of COF can be damaged at the sharp edge of the press part and the burr of mold part under the vibration condition. Therefore, it is recommended to avoid placing the gate position and parting line of the injection mold and sharp structure of metal parts around the COF.

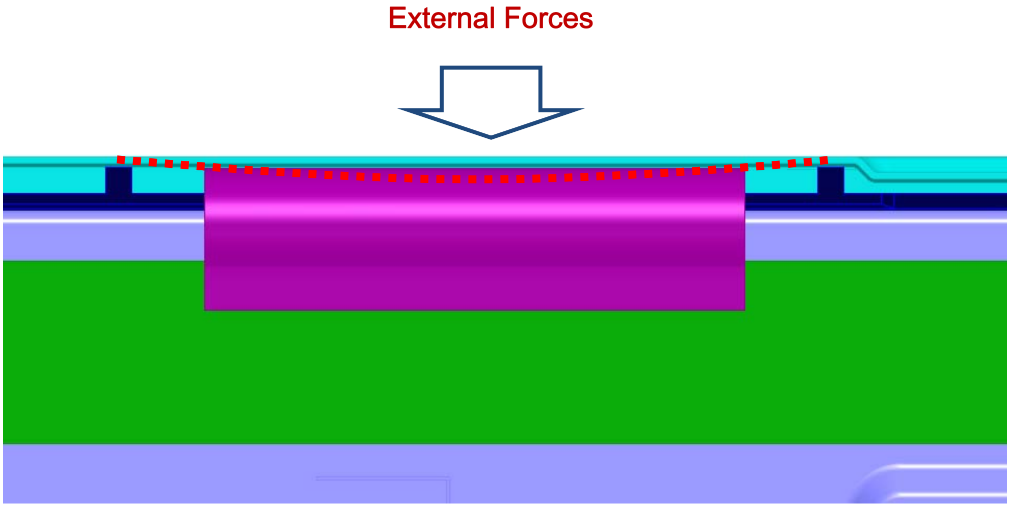
(c) The temperature of the surface of Drive-IC should be less than 125℃.

(d) Sufficient space for the COF and the Drive-IC should be secured to prevent the damage on the Drive-IC from external forces by adding the ribs around COF. And it is also important to reduce the gap between the ribs and the front cover as small as possible

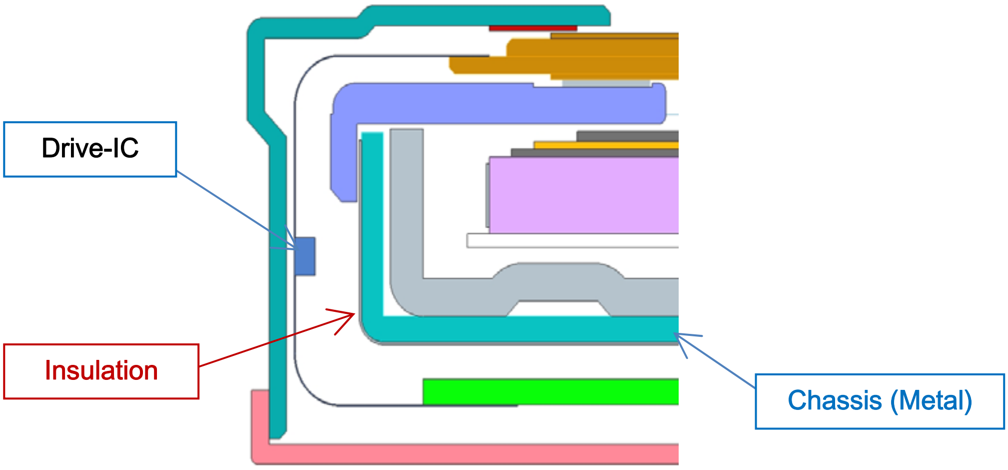




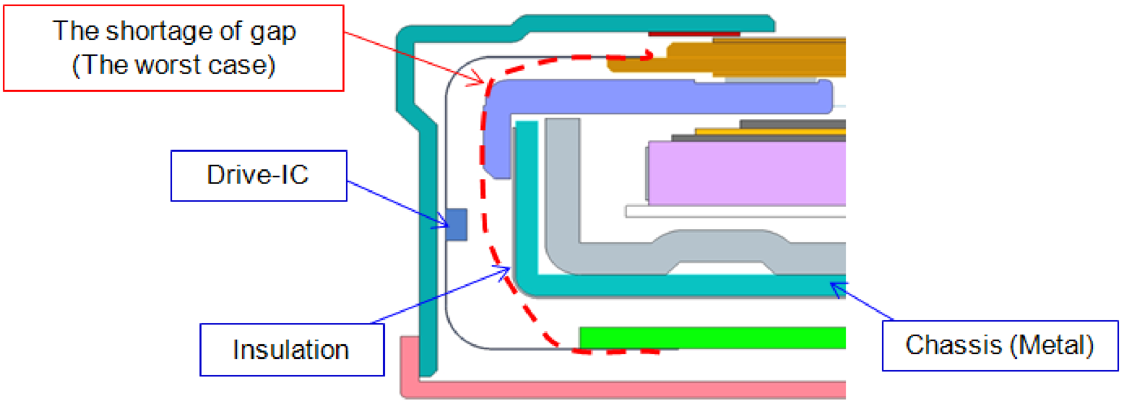
(e) It is recommended to make ribs for protecting Drive-IC as close as possible from the COF, otherwise forces from outside can deform the front cover and damage to the D-IC.



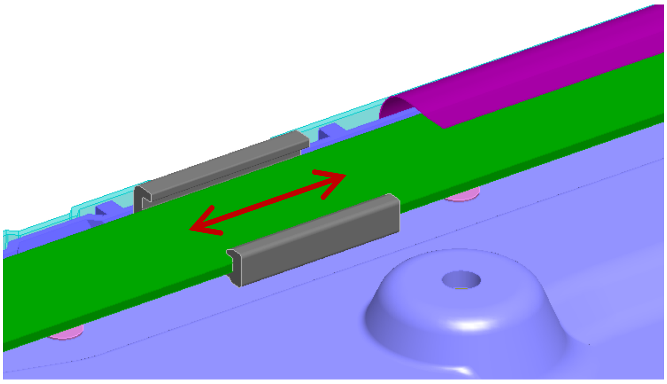
(f) When metal parts are assembled next to the Drive-IC, the metal part should be insulated to avoid the damage on Drive-IC from electrostatic discharge.



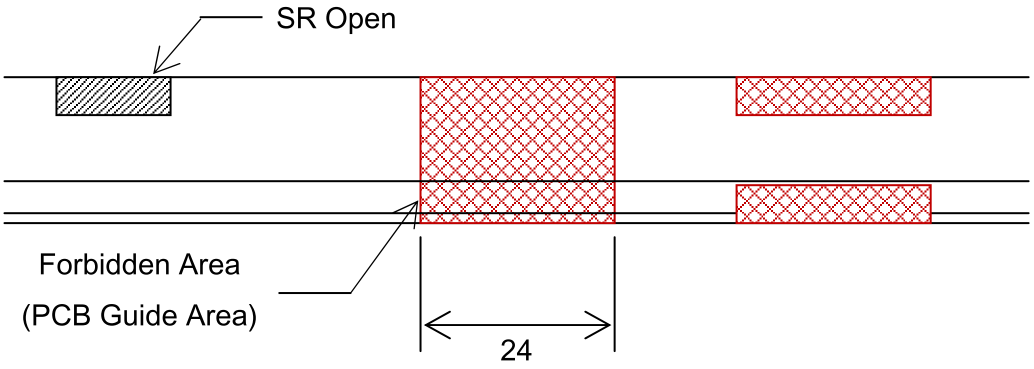
(g) If the length of COF is designed to be short, the lead crack can be occurred by applying the tension on the COF due to the drop, vibration and twist of the product.



(h) It is recommended that the source PCB should be easily moved in the direction which is parallel to the longer side of the panel, in order for the tension not to be applied to the COF under vibrating condition, such as transportation of the product.



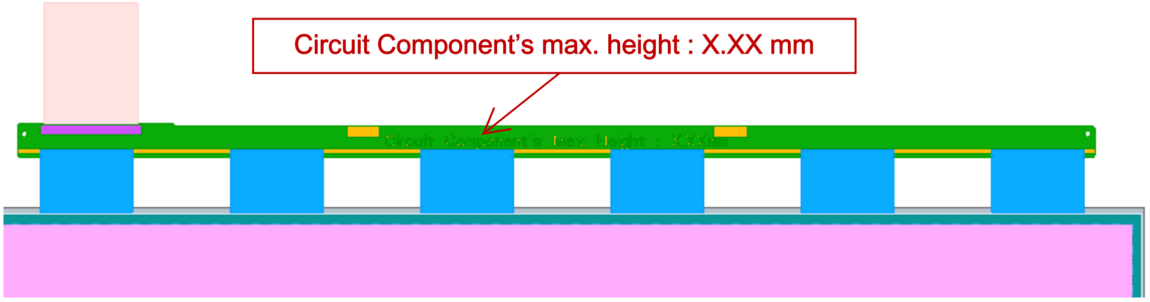
(I) It is suggested to make the holding structures of source PCB at the positions which is provided by SDC. They are marked at the 2D drawing and named as ‘PCB guide area’.



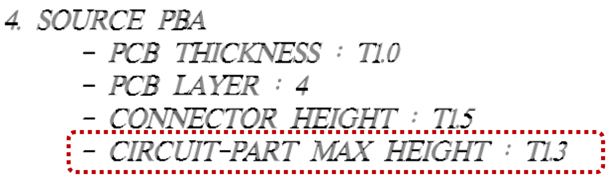
3.3 The control PBA and the Source PBA

(a) The gap between the circuit parts of the source PBA (or control PBA) and other parts should be considered to avoid damage on electrical parts by the static electrostatic discharge, short and external forces. If the shielding part is made of metal and if there is not enough distance from circuit parts, adding insulation is recommended. SDC will provide maximum height of circuit parts with 2D and 3D drawing, each customer can decide the distance under consideration of the material, thickness and other characteristics.

3D Drawing

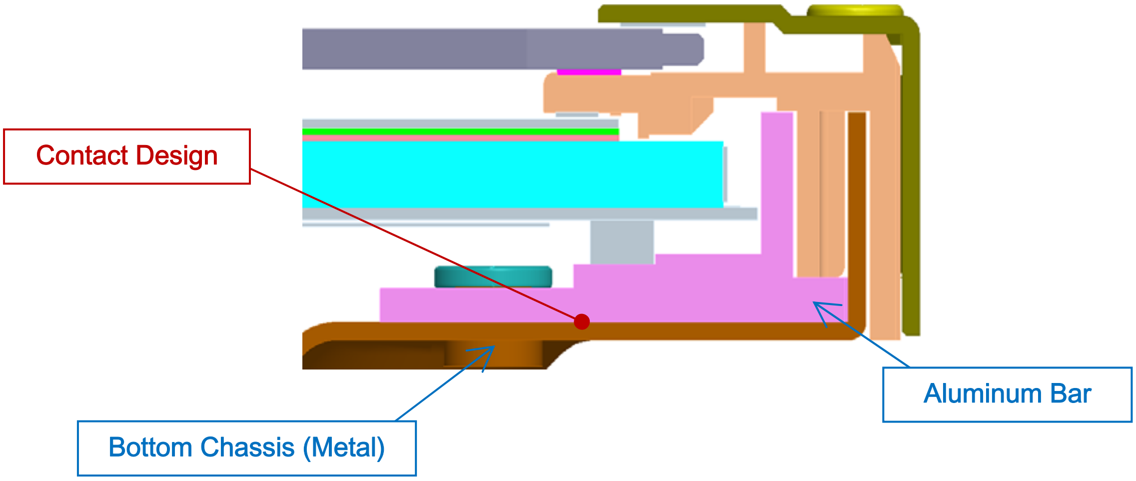


2D Drawing

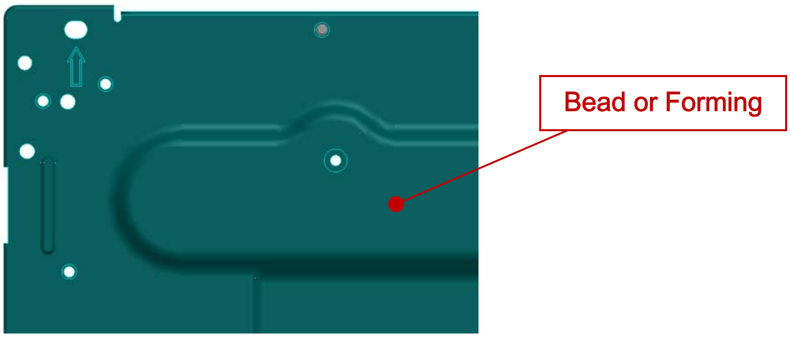

4. SOURCE PBA
- PCB THICKNESS : T1.0
- PCB LAYER : 4
- CONNECTOR HEIGHT : T1.5
- CIRCUIT-PART MAX HEIGHT : T1.3

3. 4 The 4-Corner and the cloudy light leakage

(a) SDC recommends to design in a way that the heat from light source should be dissipated effectively. For example, it is recommended to make the contact area between the heat sink and the bottom chassis to be maximized. The sharp change of temperature or the large temperature gradient in the surface of panel can cause the light leakage.

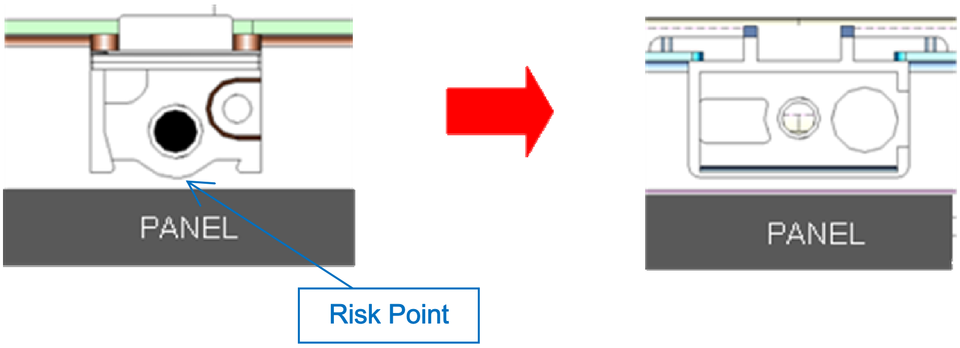


(b) The distortion of the panel by the lack of the stiffness of BLU can cause the light leakage and therefore it is recommended to design strong structure against distortion, such as place the strong beads at the corner of BLU to control the flatness of the panel.



3.5 Others

(d) Sharp or the round shape near the panel should be changed to flat shape, such as screw point, gate point of the injection mold etc. Since the panel can be damaged by the concentrated force of the convex point when there is external force.



(b) It is recommended to design the temperature of the active area below 50°C at room temperature for the protection from abnormalities in the screen due to the deterioration of the liquid crystal. In addition, each customer needs to consider all the guarantee conditions connected with temperature for this problem not to happen.