

# Multi line sensor heads for Wide format Scanner

## LSH1208-BD70A

Multi line Sensor heads(MLS) corresponding to high speed scan and to reading wrinkles and fold lines due to 6 output channels and dual light source. Newly developed shield-structure sensor IC improved anti-noise characteristic.

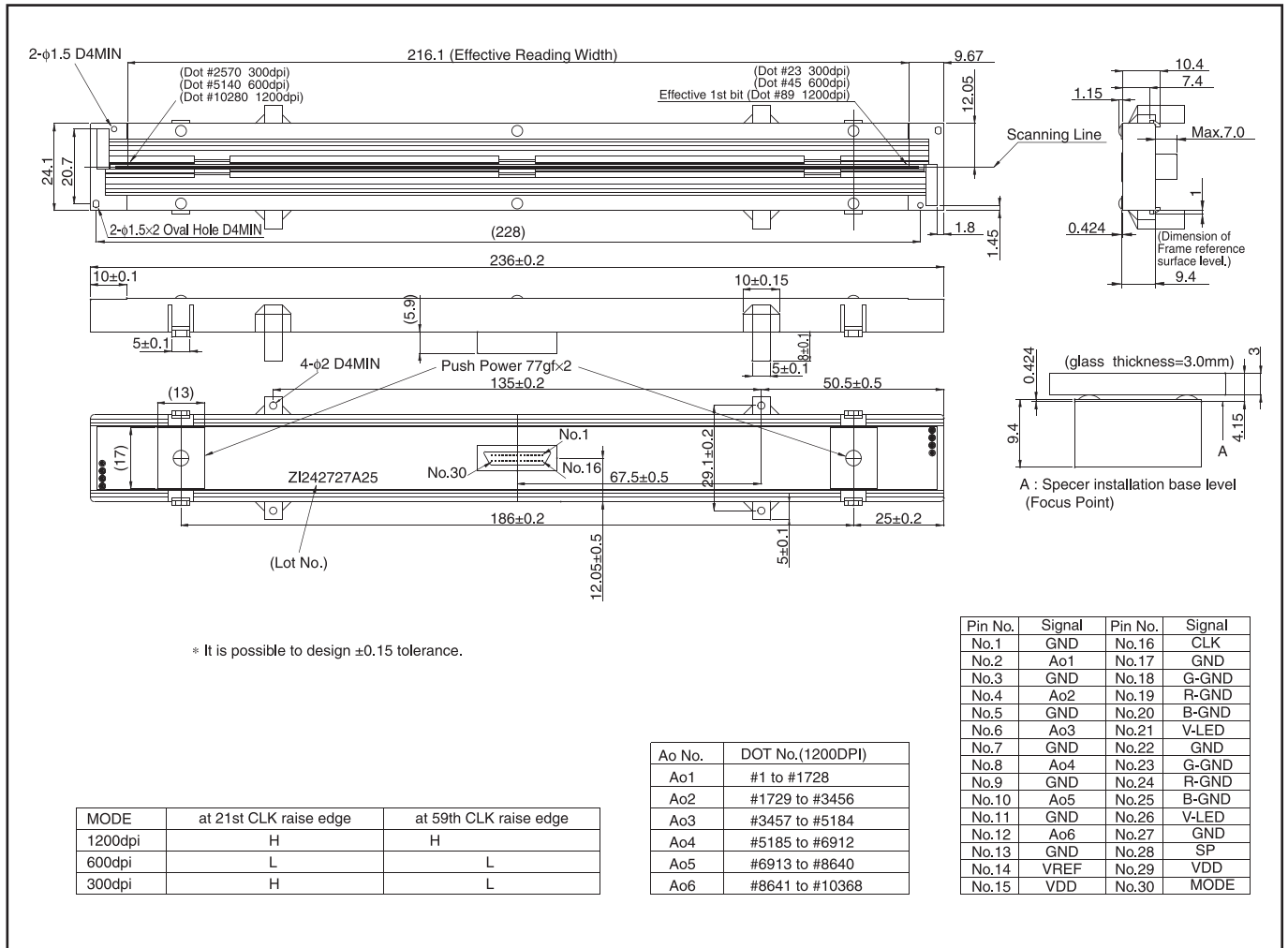
### ●Applications

High speed reading equipment (i.e. document scanners, wide format scanners devices).

### ●Features

- 1) High speed reading capability due to 6 analog output.
- 2) Newly developed shield-structure sensor IC shuts out external noise. Moreover, it reduces malfunction due to applying electro-static as represented by IEC61000-4-2.
- 3) Reduction of shade due to wrinkles and fold lines by adopting dual light source.

### ●Dimensions (Unit : mm)



## ●Characteristics

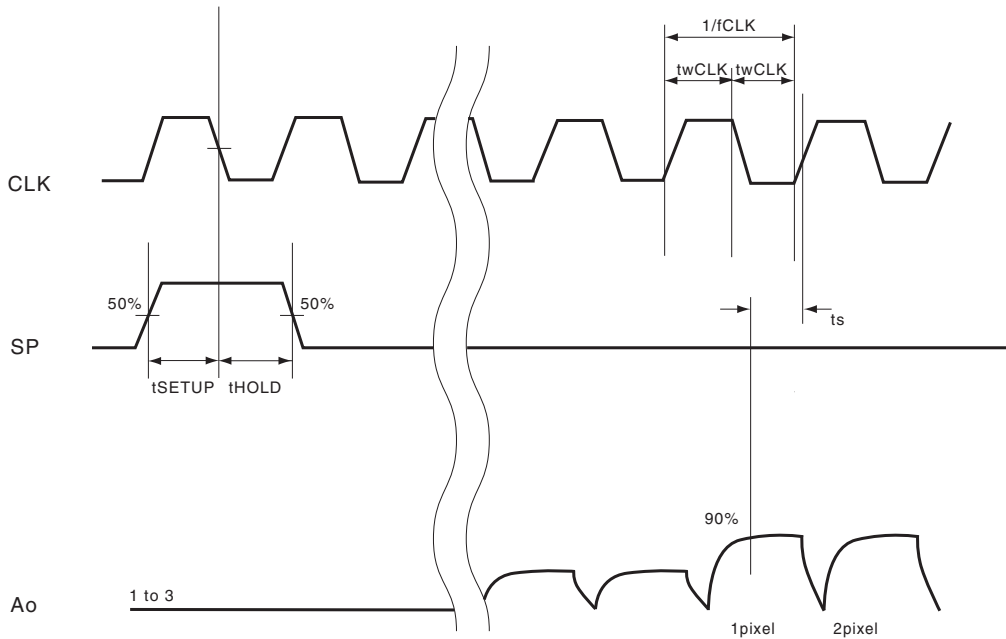
Parameter	Symbol	Typ.	Unit
Effective scanning width	–	216	mm
Primary scan dot density	–	1200	dpi
Total dot number	–	10368	dots
Power supply voltage	V <sub>DD</sub>	3.3	V
Reference voltage	V <sub>REF</sub>	0.8	V
Scanning speed	SLT	0.125×3	ms / line
Clock frequency	CLK	8	MHz
Maximum dynamic range	VR <sub>Max</sub>	0.5	V
Minimum dynamic range	VR <sub>Min.</sub>	0.25	V
Dark output	V <sub>od</sub>	V <sub>REF</sub> ±0.1	V
Operating temperature	–	5 to 45	°C

## ●Pin assignments

Pin No.	Signal	Pin No.	Signal
No.1	GND	No.16	CLK
No.2	Ao1	No.17	GND
No.3	GND	No.18	G-GND
No.4	Ao2	No.19	R-GND
No.5	GND	No.20	B-GND
No.6	Ao3	No.21	V-LED
No.7	GND	No.22	GND
No.8	Ao4	No.23	G-GND
No.9	GND	No.24	R-GND
No.10	Ao5	No.25	B-GND
No.11	GND	No.26	V-LED
No.12	Ao6	No.27	GND
No.13	GND	No.28	SP
No.14	VREF	No.29	VDD
No.15	VDD	No.30	MODE

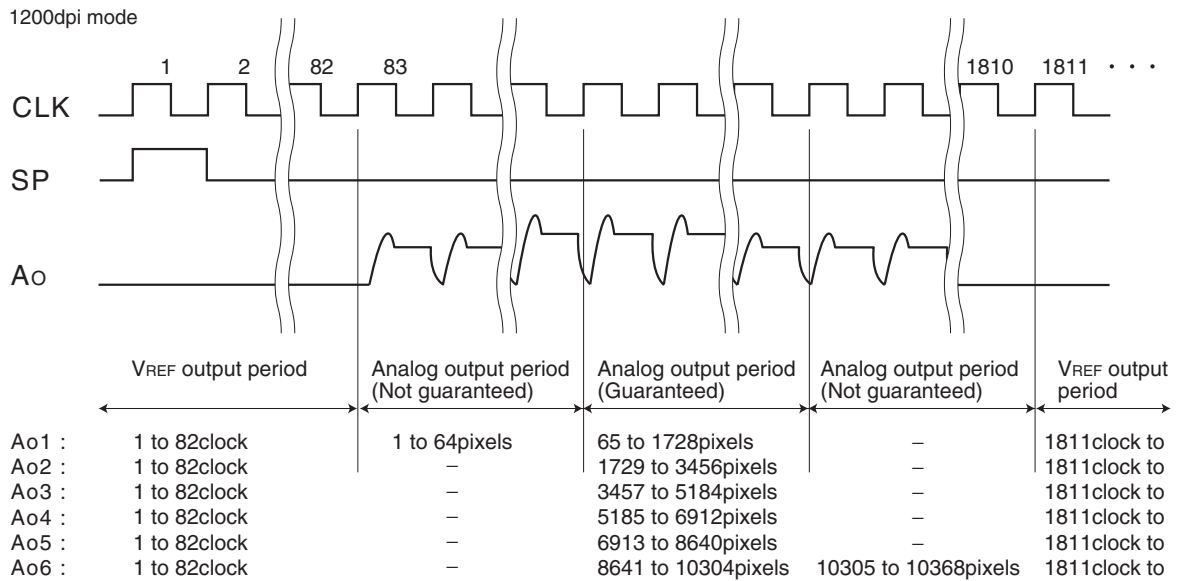
●Timing chart

(a) CLK Timing Chart



(b-1) Data Output Timing Chart (1200dpi mode)

After turning on the SP pulse, the analog output starts from the setting up point of 83 clock pulse.

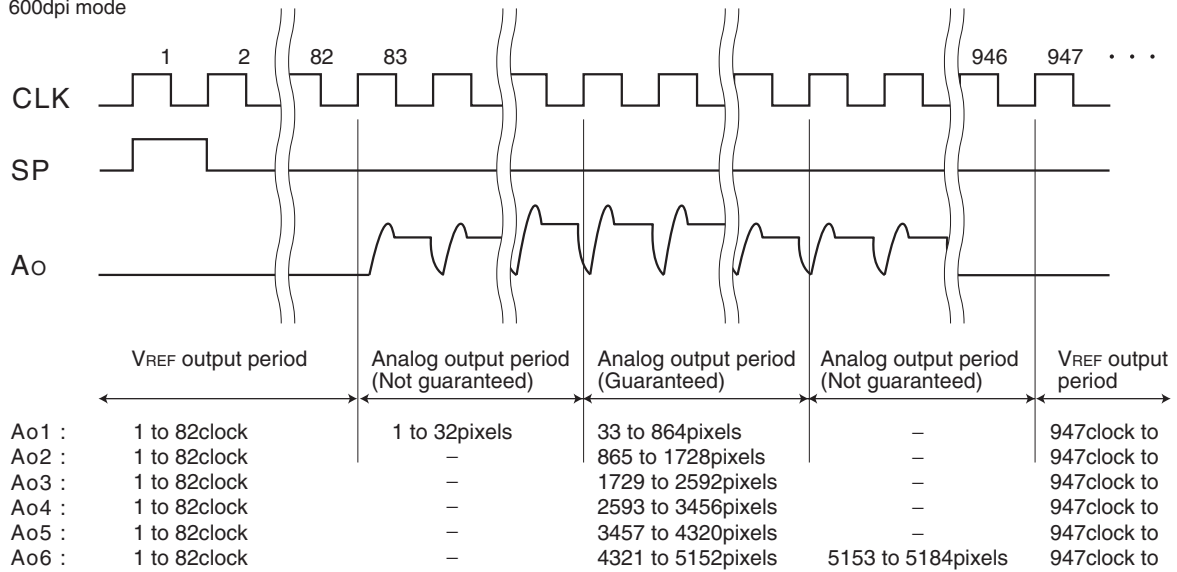


Note)The CLK section area which is over the effective pixel numbers (Output blank part) cannot be used as the analog Output standard level.

(b-2) Data Output Timing Chart (600dpi mode)

After turning on the SP pulse, the analog output starts from the setting up point of 83 clock pulse.

600dpi mode

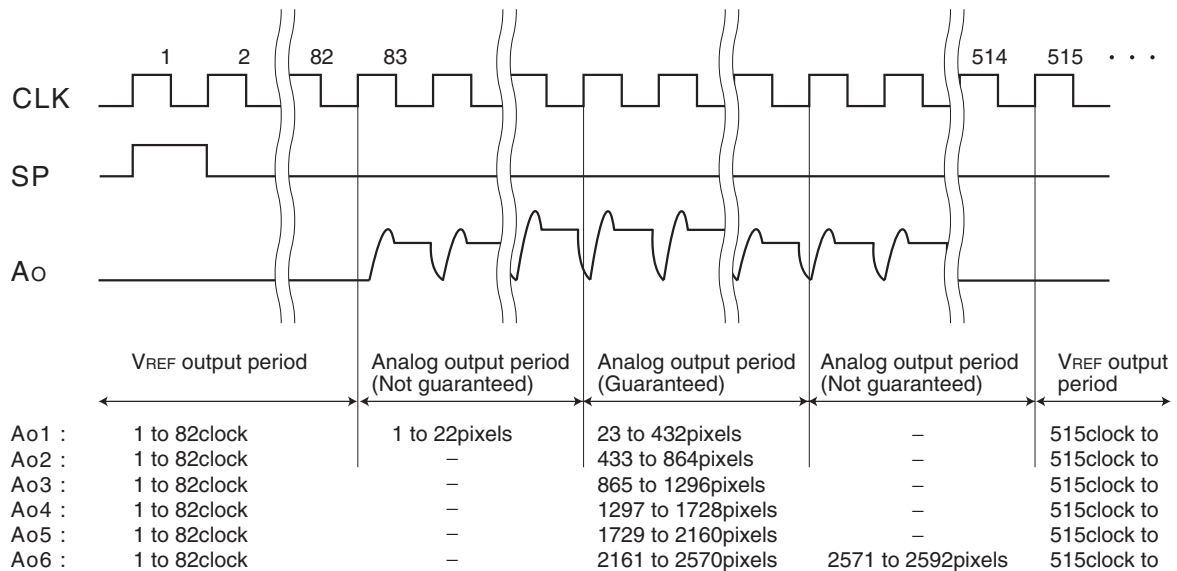


Note)The CLK section area which is over the effective pixel numbers (Output blank part) cannot be used as the analog Output standard level.

(b-3) Data Output Timing Chart (300dpi mode)

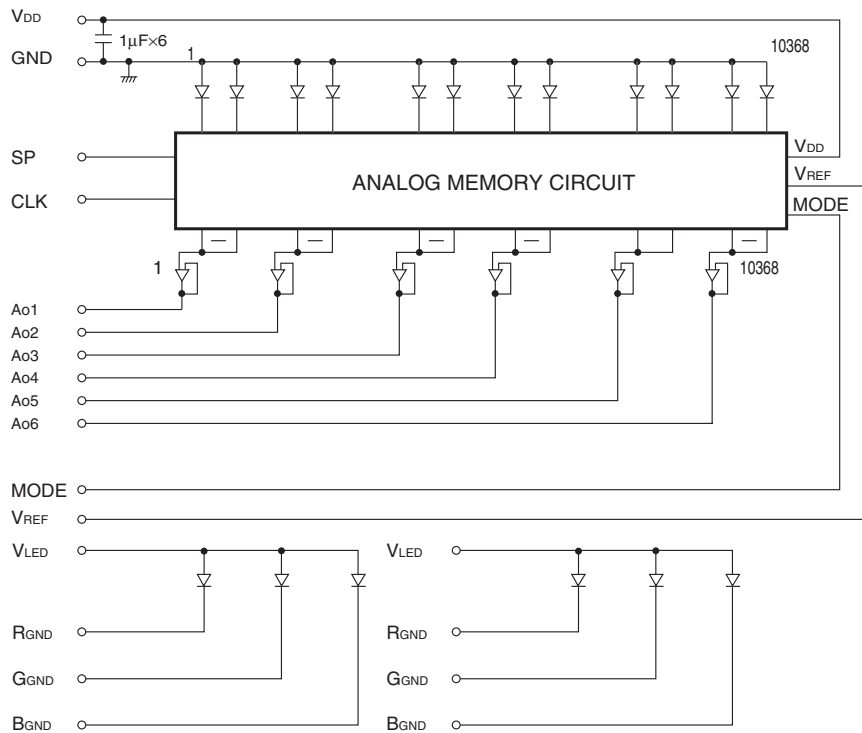
After turning on the SP pulse, the analog output starts from the setting up point of 83 clock pulse.

300dpi mode

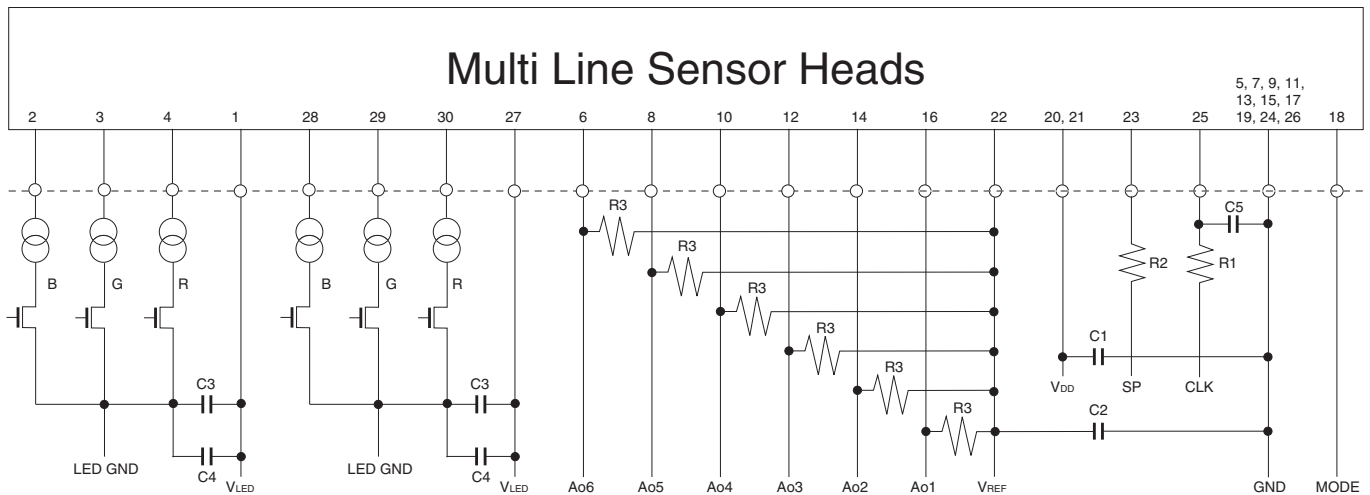


Note)The CLK section area which is over the effective pixel numbers (Output blank part) cannot be used as the analog Output standard level.

● Inner circuit



● Peripheral circuit



R1=R2=100Ω, R3=100KΩ  
 C1=C2=47µF  
 C3=100µF, C4=0.1µF, C5=100pF

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