LINEAR SYSTEMS

LSID100
LOW LEAKAGE
PICO-AMP DUAL DIODE

micross

Linear Systems replaces discontinued Intersil LSID100

The LSID100 is a low leakage Monolithic Dual Pico-Amp Diode

The LSID100 low-leakage monolithic dual diode provides a superior alternative to conventional diode technology when reverse current (leakage) must be minimized. In addition the monolithic dual construction allows excellent capacitance matching per diode. The LSID100 features a leakage current of 0.1 pA and is well suited for use in applications such as input protection for operational amplifiers.

LSID100 Benefits:

- Negligible Circuit Leakage Contribution
- Circuit "Transparent" Except to Shunt High-Frequency Spikes
- Simplicity of Operation

LSID100 Applications:

- Op Amp Input Protection
- Multiplexer Overvoltage Protection

FEATURES	
DIRECT REPLACEMENT FOR INTERSIL LSID100	
REVERSE LEAKAGE CURRENT	I_R = 0.1pA
REVERSE BREAKDOWN VOLTAGE	$BV_R \geq$ 30V
REVERSE CAPACITANCE	C_{rss} = 0.75pF
ABSOLUTE MAXIMUM RATINGS (Note 1) @ 25°C (unless otherwise noted)	
Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Maximum Power Dissipation	
Continuous Power Dissipation	300mW
Maximum Currents	
Forward Current	20mA
Reverse Current	100µA
Maximum Voltages	
Reverse Voltage	30V
Diode to Diode Voltage	±50V

LSID100 ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_R	Reverse Breakdown Voltage	30	--	--	V	I_R = 1µA
V_F	Forward Voltage	0.8	--	1.1	V	I_F = 10mA
I_R	Reverse Leakage Current	--	0.1	--	pA	V_R = 1V
		--	2.0	10		V_R = 10V
$\|I_{R1}-I_{R2}\|$	Differential Leakage Current	--	--	3		
C_{rSS}	Total Reverse Capacitance(Note 2)	--	0.75	1	pF	V_R = 10V, f = 1MHz

Note 1 - Absolute maximum ratings are limiting values above which LSID100 serviceability may be impaired.
Note 2 - Design reference only, not 100% tested

FIGURE 1 – Operational Amplifier Protection

Input Differential Voltage limited to 0.8V (typ) by Diodes LSID100 D_1 and D_2. Common Mode Input voltage limited by Diodes LSID100 D_3 and D_4 to ±15V.

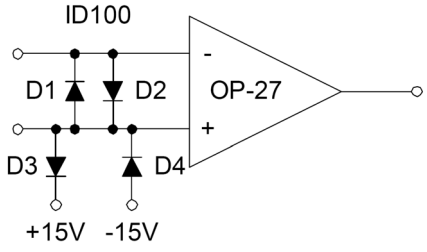
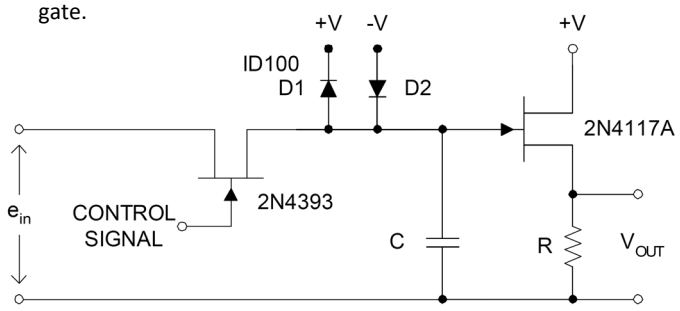
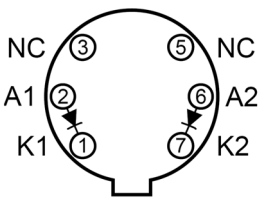


FIGURE 2 – Sample & Hold Circuit

Typical Sample and Hold circuit with clipping. LSID100 diodes reduce offset voltages fed capacitively from the LSID100 switch gate.



TO-78 (Bottom View)



Note pins 3 & 5 must not be connected, in any fashion or manner, to any circuit or node

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Available Packages:

LSID100 in TO-78
LSID100 available as bare die

Please contact Micross for full package and die dimensions