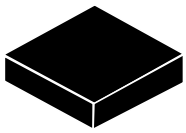
LSM9DS0

iNEMO inertial module: 3D accelerometer, 3D gyroscope, 3D magnetometer

Datasheet - production data



LGA-24 (4x4x1.0 mm)

Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- ±2/±4/±6/±8/±16 *g* linear acceleration full scale
- ±2/±4/±8/±12 gauss magnetic full scale
- ±245/±500/±2000 dps angular rate full scale
- 16-bit data output
- SPI / I^2C serial interfaces
- Analog supply voltage 2.4 V to 3.6 V
- Power-down mode / low-power mode
- Programmable interrupt generators
- Embedded self-test
- Embedded temperature sensor
- Embedded FIFO
- Position and motion detection functions
- Click/double-click recognition
- Intelligent power saving for handheld devices
- ECOPACK®, RoHS and “Green” compliant

Applications

- Indoor navigation
- Smart user interfaces
- Advanced gesture recognition
- Gaming and virtual reality input devices
- Display/map orientation and browsing

Description

The LSM9DS0 is a system-in-package featuring a 3D digital linear acceleration sensor, a 3D digital angular rate sensor, and a 3D digital magnetic sensor.

The LSM9DS0 has a linear acceleration full scale of ±2*g*/±4*g*/±6g/±8*g*/±16*g,* a magnetic field full scale of ±2/±4/±8/±12 gauss and an angular rate of ±245/±500/±2000 dps.

The LSM9DS0 includes an I^2C serial bus interface supporting standard and fast mode (100 kHz and 400 kHz) and an SPI serial standard interface.

The system can be configured to generate interrupt signals on dedicated pins and is capable of motion and magnetic field detection. Thresholds and timing of interrupt generators are programmable by the end user.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in power-down mode separately for smart power management.

The LSM9DS0 is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM9DS0	-40 to +85	LGA-24	Tray
LSM9DS0TR	-40 to +85	LGA-24	Tape and reel

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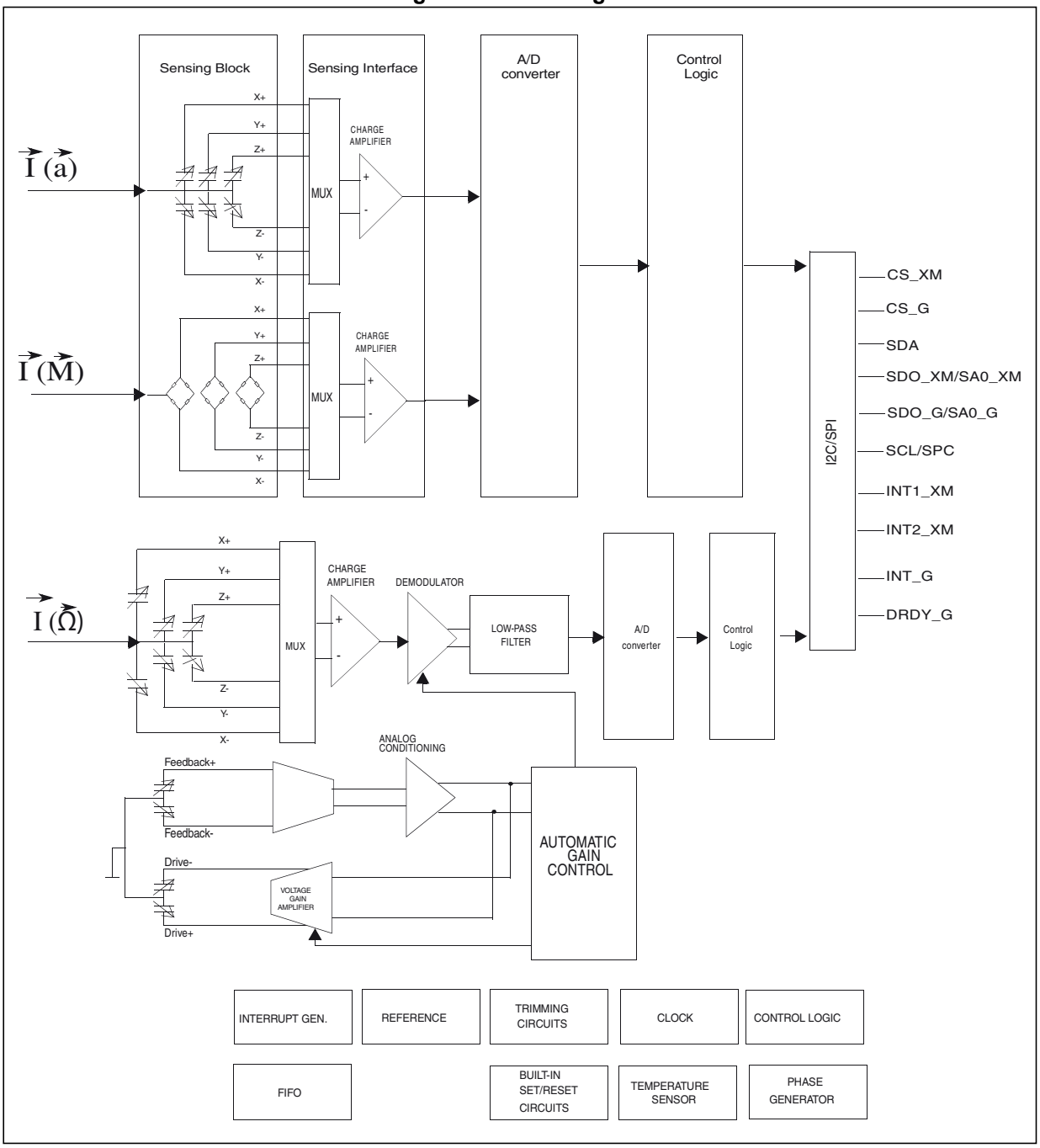
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

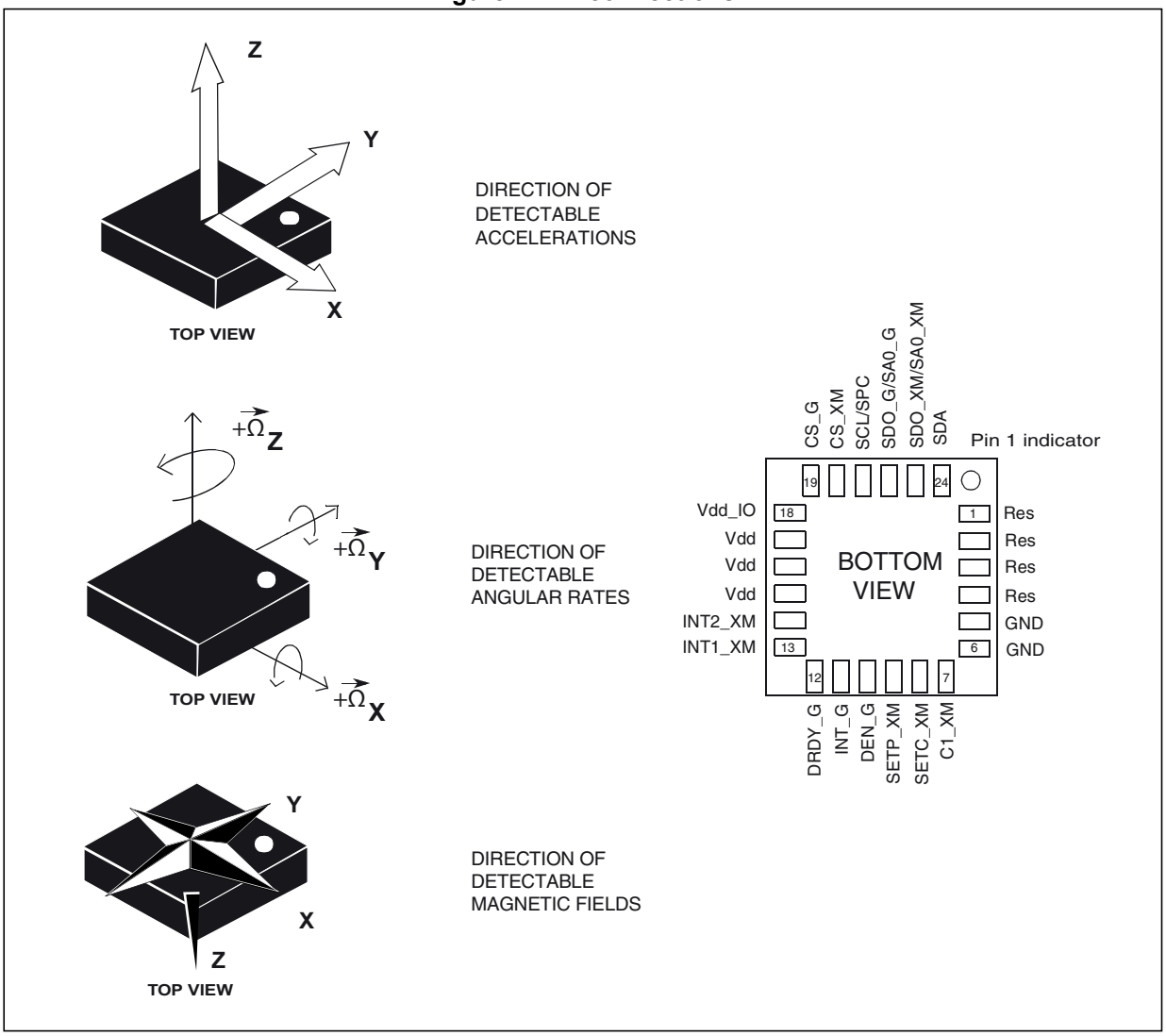


Table 2. Pin description

Pin#	Name	Function
1	Reserved	Leave unconnected
2	Reserved	Connect to GND
3	Reserved	Connect to GND
4	Reserved	Connect to GND
5	GND	0 V supply
6	GND	0 V supply
7	C1_XM	Capacitor connection (C1)
8	SETC_XM	S/R capacitor connection (C2)
9	SETP_XM	S/R capacitor connection (C2)
10	DEN_G	Gyroscope data enable
11	INT_G	Gyroscope programmable interrupt
12	DRDY_G	Gyroscope data ready
13	INT1_XM	Accelerometer and magnetic sensor interrupt 1
14	INT2_XM	Accelerometer and magnetic sensor interrupt 2
15	Vdd	Power supply
16	Vdd	Power supply
17	Vdd	Power supply
18	Vdd_IO	Power supply for I/O pins
19	CS_G	Gyroscope I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
20	CS_XM	Accelerometer and magnetic sensor SPI enabled I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
21	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
22	SDO_G SA0_G	Gyroscope serial data output (SDO) Angular rate sensor I^2C less significant bit of the device address (SA0)
23	SDO_XM SA0_XM	Accelerometer and magnetic sensor SPI serial data output (SDO) Accelerometer and magnetic sensor I^2C less significant bit of the device address (SA0)
24	SDA	I^2C serial data (SDA)

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a]

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]			±2		g
				±4		
				±6		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
G_FS	Angular rate measurement range			±245		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	Linear acceleration FS = ±2 *g*		0.061		mg/LSB
		Linear acceleration FS = ±4 *g*		0.122		
		Linear acceleration FS = ±6 *g*		0.183		
		Linear acceleration FS = ±8 *g*		0.244		
		Linear acceleration FS = ±16 *g*		0.732		
M_GN	Magnetic sensitivity	Magnetic FS = ±2 gauss		0.08		mgauss/ LSB
		Magnetic FS = ±4 gauss		0.16		
		Magnetic FS = ±8 gauss		0.32		
		Magnetic FS = ±12 gauss		0.48		
G_So	Angular rate sensitivity	Angular rate FS = ±245 dps		8.75		mdps/ digit
		Angular rate FS = ±500 dps		17.50		
		Angular rate FS = ±2000 dps		70		
LA_TCSo	Linear acceleration sensitivity change vs. temperature	From -40 °C to +85 °C		±1.5		%
M_TCSo	Magnetic sensitivity change vs. temperature	From -40 °C to +85 °C		±3		%

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

Table 3. Sensor characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
G_SoDr	Angular rate sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
LA_TyOff	Linear acceleration typical zero-g level offset accuracy(3)(4)			±60		mg
G_TyOff	Angular rate typical zero-rate level	FS = 245 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
LA_TCOff	Linear acceleration zero-g level change vs. temperature	Max delta from 25 °C		±0.5		mg/°C
G_TCOff	Zero-rate level change vs. temperature			±0.05		dps/°C
M_EF	Maximum exposed field	No perming effect on zero reading			10000	gauss
M_DF	Magnetic disturbing field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
LA_ST	Linear acceleration self-test positive difference (6)(7)	±2 *g* range, X, Y, Z-axis AST1:0 = 01 see *Table 74*	60		1700	mg
G_ST	Angular rate self-test output change (8)(9)	FS = 245 dps	20		250	dps
		FS = 500 dps	70		400	
		FS = 2000 dps	150		1000	
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Verified by wafer level test and measurement of initial offset and sensitivity
3. Typical zero-*g* level offset value after MSL3 preconditioning
4. Offset can be eliminated by enabling the built-in high-pass filter
5. Set / Reset Pulse is automatically applied at each conversion cycle
6. “Self-test output change” is defined as: OUTPUT[mg]$_{(}$*CTRL_REG2_XM (21h)* $_{\text{AST1:0 enabled)}}$ - OUTPUT[mg]$_{(}$*CTRL_REG2_XM (21h)* $_{\text{AST1:0 disabled)}}$
7. For polarity refer to *Table 77: Self-test mode configuration*
8. “Self-test output change” is defined as: OUTPUT[mg]$_{(}$*CTRL_REG4_G (23h)* $_{\text{ST1:0 enabled)}}$ - OUTPUT[mg]$_{(}$*CTRL_REG4_G (23h)* ST1:0 disabled)
9. For polarity refer to *Table 31: Self-test mode configuration*

2.2 Temperature sensor characteristics

The electrical characteristics concerning the temperature sensor are given in the table below.

@ Vdd = 3.0 V, T=25 °C unless otherwise noted.

Table 4. Temperature sensor electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		8		LSB/°C
TODR	Temperature refresh rate			M_ODR [2:0](2)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Refer to *Table 84: Magnetic data rate configuration*.

2.3 Electrical characteristics

@ Vdd = 3.0V, T = 25 °C unless otherwise noted[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd_XM	Current consumption of the accelerometer and magnetic sensor in normal mode (2)		HR setting CTRL_REG5_XM (M_RES [1,0]) = 11b, see *CTRL_REG5_XM (24h)*	350		µA
Idd_G	Gyroscope current consumption in normal mode(3)			6.1		mA
Idd_G_LP	Gyroscope supply current in sleep mode(4)			2		mA
Idd_Pdn	Current consumption in power-down mode(5)			6		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed
2. Magnetic sensor setting ODR =6.25 Hz, Accelerometer sensor ODR =50 Hz, gyroscope in power-down mode
3. Accelerometer and magnetic sensor in power-down mode
4. Sleep mode introduces a faster turn-on time compared to power-down mode. Accelerometer and magnetic sensor in power-down mode.
5. Linear accelerometer, magnetic sensor and gyroscope in power-down mode

b. LSM9DS0 is factory calibrated at 3.0 V

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

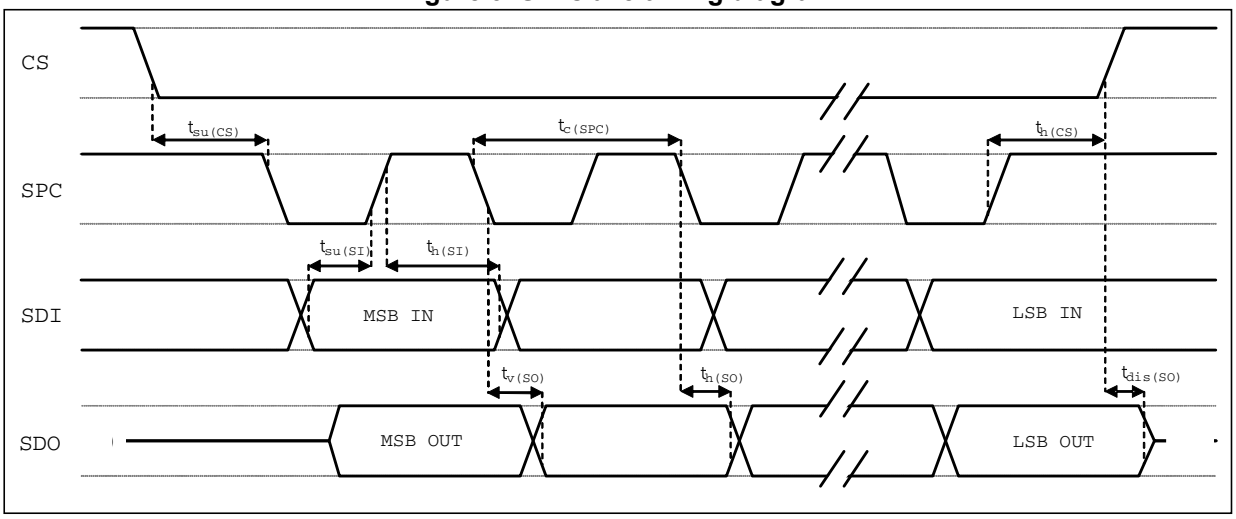
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 Sensor I²C - inter-IC control interface

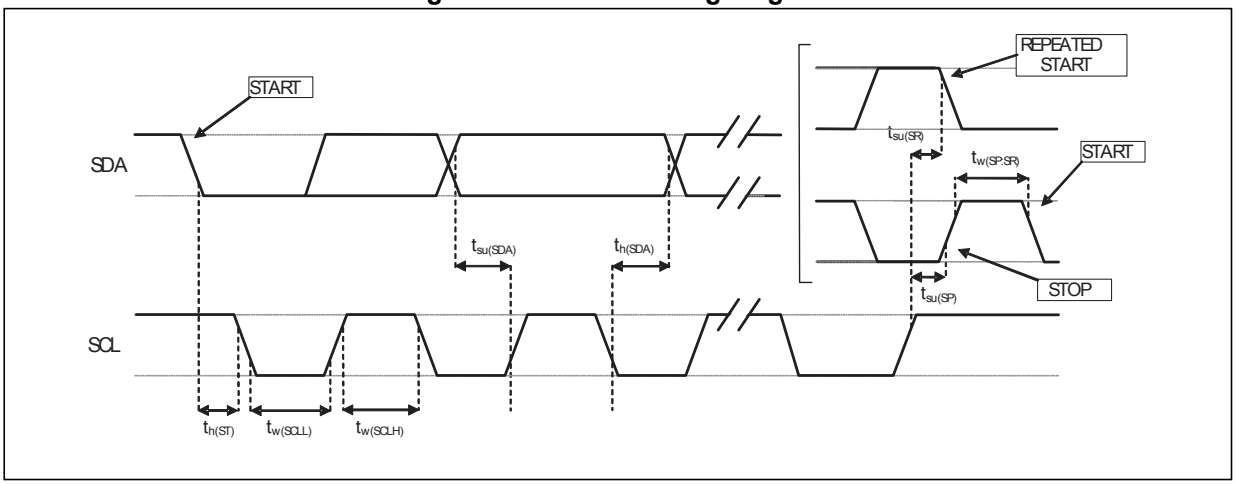
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL/SPC, SDA, SDO_XM/SA0_XM, SDO_G/SA0_G, CS_G, CS_XM, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	g
		10,000 for 0.1 ms	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This is an electrostatic-sensitive device (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Set / reset pulse

The set / reset pulse is an automatic operation performed before each magnetic acquisition cycle to degauss the sensor and to ensure alignment of the magnetic dipoles and thus the linearity of the sensor itself.

3.2 Sensitivity

The methods to determine sensitivity and offset are given below in the following paragraphs.

3.2.1 Linear acceleration sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined by applying a magnetic field of 1 *gauss* to it.

3.2.3 Angular rate sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

3.2.4 Zero-*g* level

The zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* for the X-axis and 0 *g* for the Y-axis whereas the Z-axis will measure 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature" (LA_TCOff in *Table 3*). The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.2.5 Zero-*gauss* level

The zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the Set/Reset Pulse and to the magnetic sensor readout chain, the offset is dynamically cancelled. The Zero-*g*auss level does not show any dependency on temperature or power supply.

3.2.6 Zero-rate level

The zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of highly accurate MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

4 Functionality

The LSM9DS0 is a system-in-package featuring a 3D digital accelerometer, a 3D digital magnetometer, and a 3D digital gyroscope.

The device includes specific sensing elements and two IC interfaces capable of measuring both the acceleration/magnetometer and angular rate applied to the module and to provide a signal to external applications through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM9DS0 may also be configured to generate an inertial *wake-up* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes.

4.1 Self-test

4.1.1 Accelerometer

The self-test allows the linear acceleration sensor functionality to be tested without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0’. When the self-test bit is programmed to ‘1’ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1: Sensor characteristics*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.1.2 Gyroscope

The self-test allows to test the mechanical and electric part of the sensor, allowing the seismic mass to be moved by means of an electrostatic test-force. When the ST is activated by the IC, an actuation force is applied to the sensor, emulating a definite Coriolis force. In this case the sensor output will exhibit an output change.
When the ST is active, the device output is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test-force.

For polarity please refer to *Table 31: Self-test mode configuration*.

4.2 Linear acceleration main digital blocks

4.2.1 FIFO

The LSM9DS0 embeds 32 slots of data FIFO for each of the three output channels: X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed

and burst the significant data out from the FIFO. This buffer can work accordingly in four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_SRC_REG (2Fh)*. Programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1_XM/INT2_XM pin (configured through *FIFO_SRC_REG (2Fh)*).

4.2.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.3 FIFO mode

In FIFO mode, data from the X, Y and Z channels are stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CTRL_REG (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CTRL_REG (2Eh)*. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO stops collecting data from the input channels.

4.2.4 Stream mode

In Stream mode, data from the X, Y and Z measurements are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO discards the older data as the new data arrives.

4.2.5 Stream-to-FIFO mode

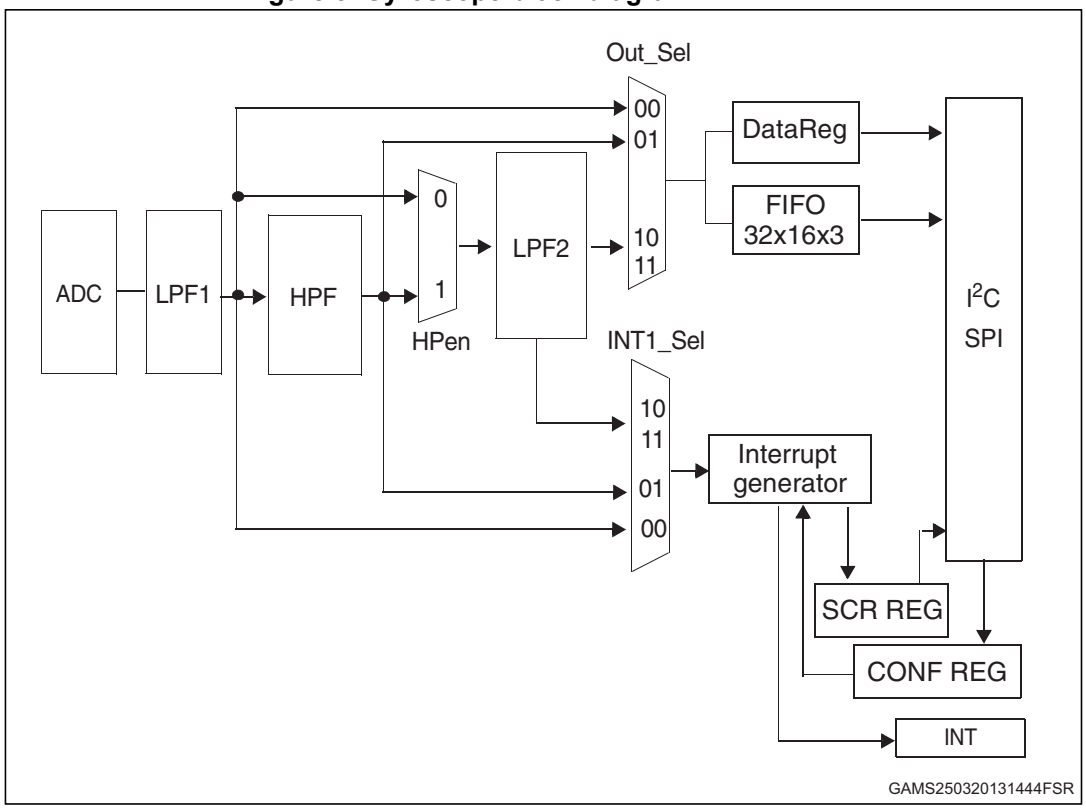
In Stream-to-FIFO mode, data from the X, Y and Z measurements is stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CTRL_REG (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CTRL_REG (2Eh)*. The FIFO continues filling until it is full (32 slots of 8-bit data for X, Y and Z). When full, the FIFO discards the older data as the data new arrives. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.6 Retrieving data from FIFO

A read operation to the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* or *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.3 Gyroscope digital main blocks

Figure 5. Gyroscope block diagram



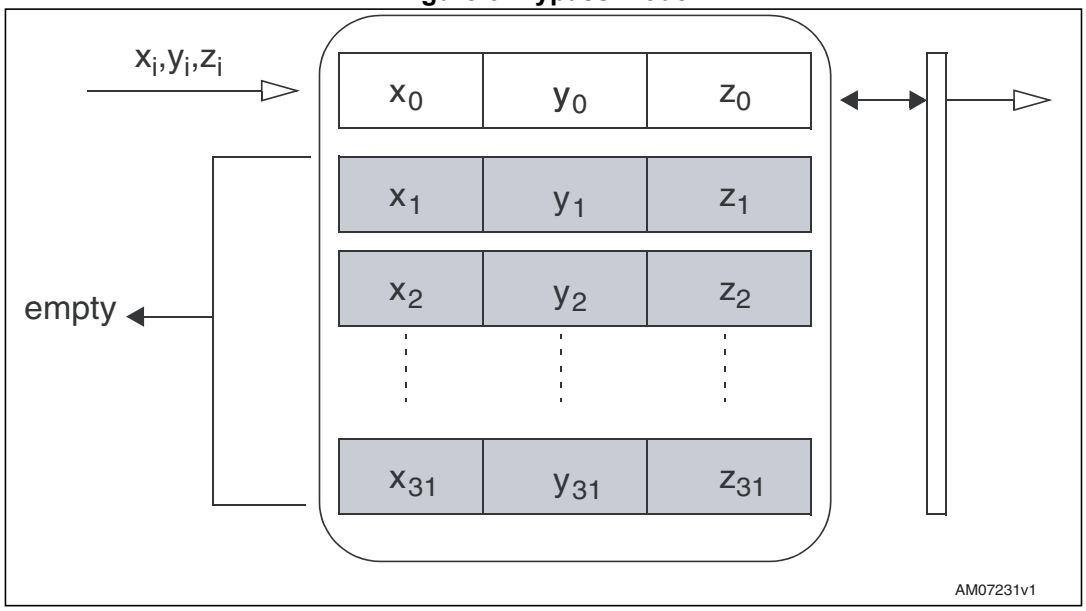
4.3.1 FIFO

The LSM9DS0 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_CTRL_REG_G (2Eh)*. A programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY_G pin (configured through *CTRL_REG3_G (22h)* and event detection information is available in *FIFO_SRC_REG_G (2Fh)*. The watermark level can be configured to WTM4:0 in *FIFO_CTRL_REG_G (2Eh)*.

4.3.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 6*, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

Figure 6. Bypass mode

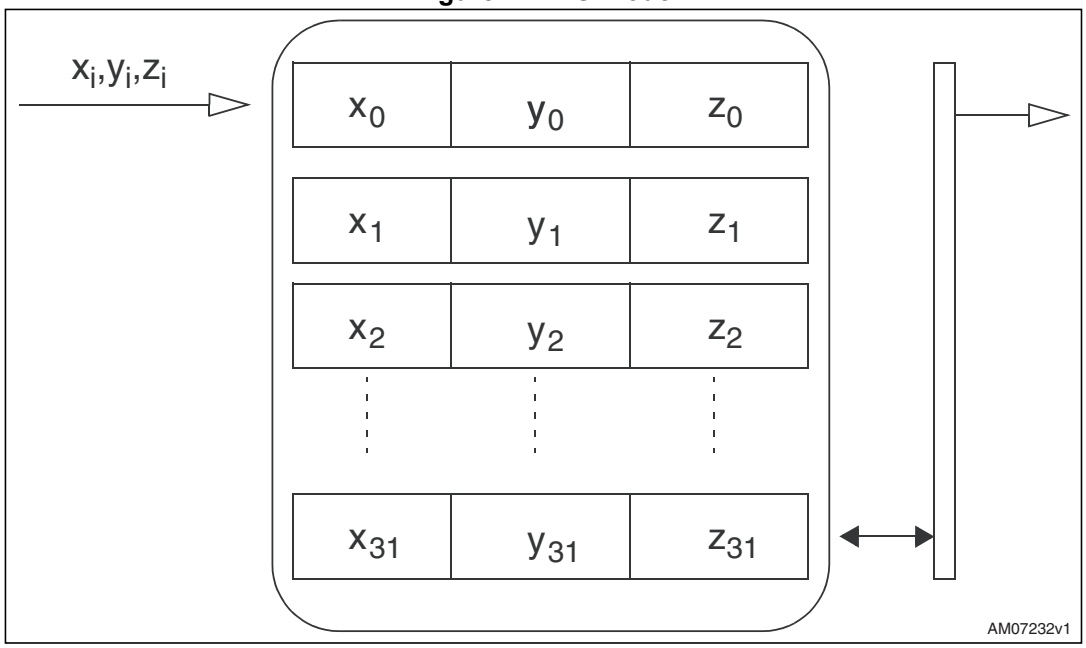


4.3.3 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in *CTRL_REG3_G (22h)*) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, *FIFO_CTRL_REG_G (2Eh)* must be written back to Bypass mode.

FIFO mode is represented in *Figure 7*.

Figure 7. FIFO mode

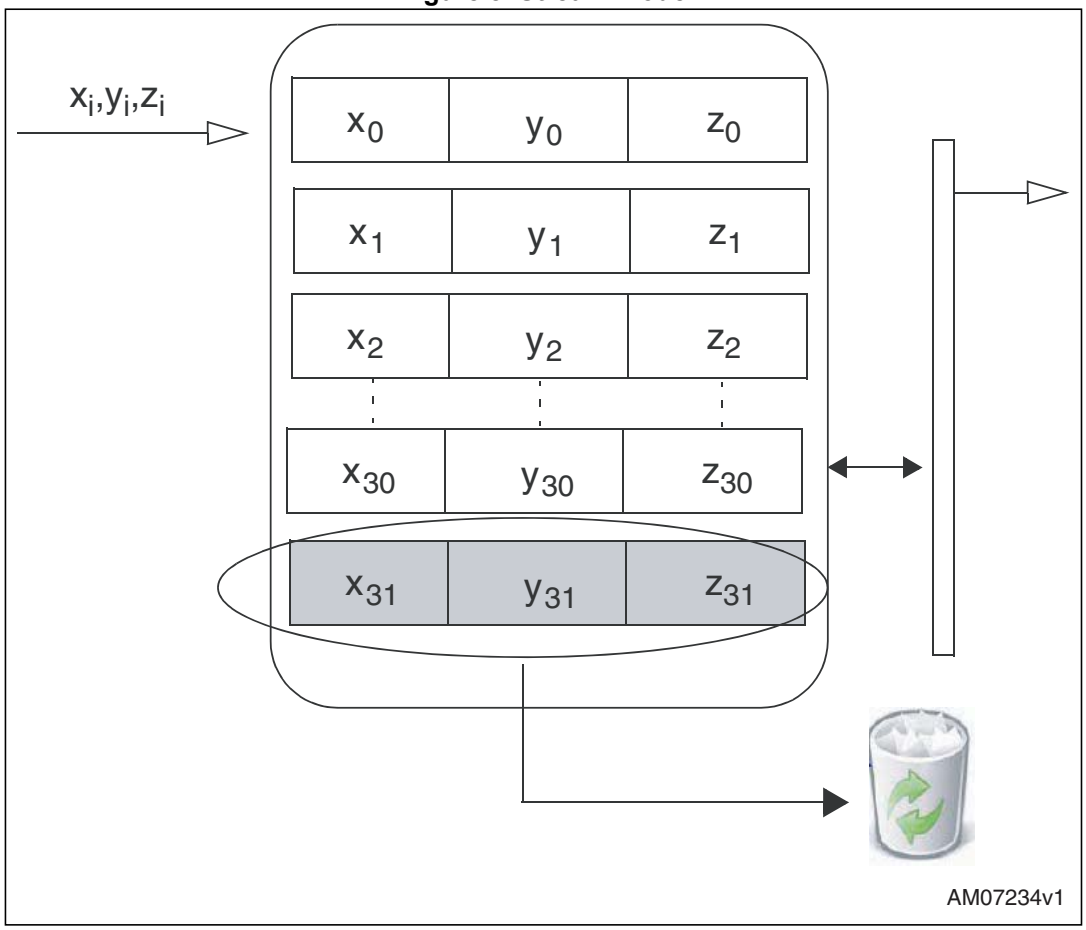


4.3.4 Stream mode

In Stream mode, data from the yaw, pitch and roll measurements is stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G pin (configured through *CTRL_REG3_G (22h)*.

Stream mode is represented in *Figure 8*.

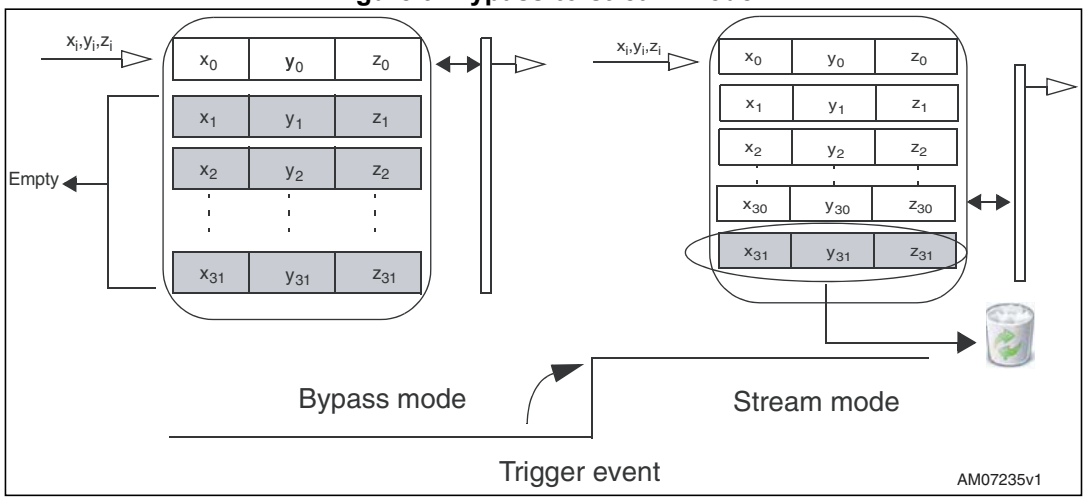
Figure 8. Stream mode



4.3.5 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *INT1_CFG_G (30h)* events) the FIFO starts operating in Stream mode. Refer to *Figure 9* below.

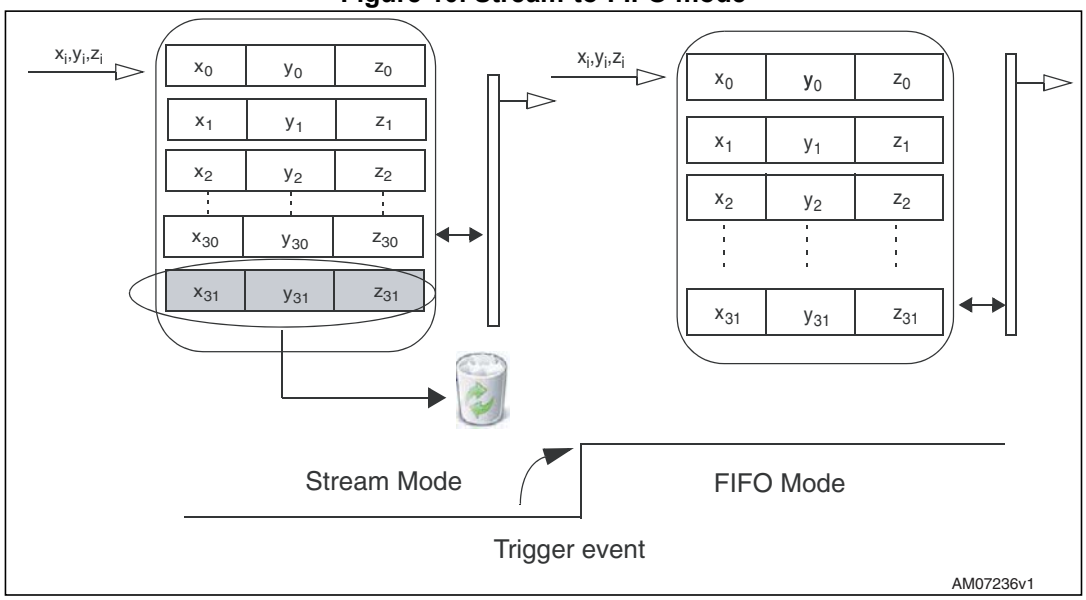
Figure 9. Bypass-to-stream mode



4.3.6 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY_G by setting the I2_WTM bit in *CTRL_REG3_G (22h)* to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to *INT1_CFG_G (30h)* events), the FIFO starts operating in FIFO mode. Refer to *Figure 10*.

Figure 10. Stream-to-FIFO mode



4.3.7 Retrieving data from FIFO

A read operation from the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* or *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data are placed in the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers and both single read and read_burst (X,Y & Z with auto-incremental address) operations can be used. When data included in *OUT_Z_H_G* is read, the system again starts to read information from addr *OUT_X_L_G*.

4.4 Temperature sensor

The LSM9DS0 features an embedded temperature sensor.

Temperature data can be enabled by setting the TEMP_EN bit in the *CTRL_REG5_XM (24h)* register to 1.

Both OUT_TEMP_H_XM and OUT_TEMP_L_XM registers must be read.

Temperature data is stored inside *OUT_TEMP_L_XM (05h), OUT_TEMP_H_XM (06h)* as two's complement data in 12-bit format, right justified.

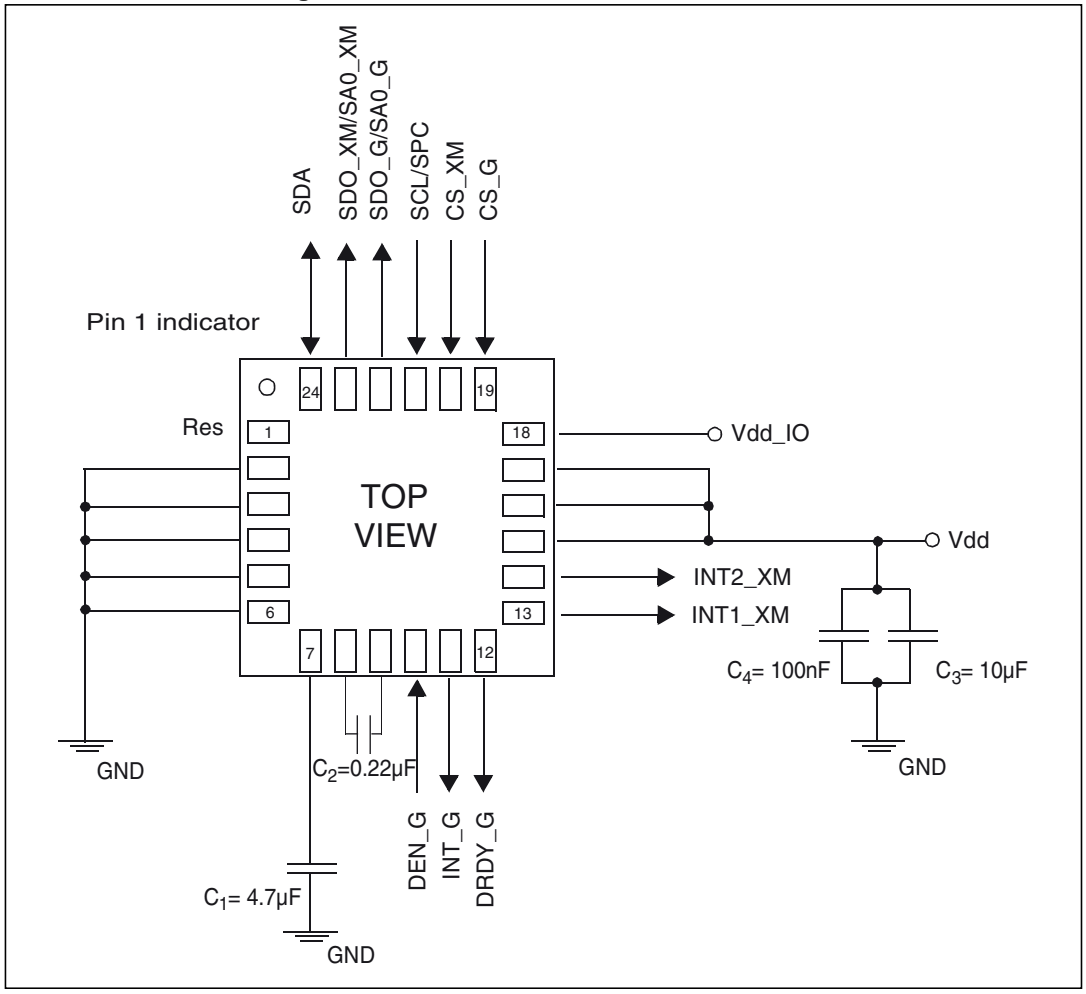
The output data rate of the temperature sensor is set by M_ODR in *CTRL_REG5_XM (24h)* and is equal to the magnetic sensor output data rate.

4.5 Factory calibration

The IC interface is factory calibrated. The trimming values are stored inside the non-volatile memory of the device. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the using the device without further calibration.

5 Application hints

Figure 11. LSM9DS0 electrical connections



5.1 External capacitors

The C1 and C2 external capacitors should be low SR value, ceramic type construction (typ recommended value 200 mOhm). Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C4 = 100 nF ceramic, C3 = 10 µF Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 11*).

The functions of the device and the measured acceleration/magnetic field data are selectable and accessible through the I^2C / SPI interfaces.

The functions, the threshold and the timing of the three interrupt pins (INT_G, INT1_XM and INT2_XM) can be completely programmed by the user through the I^2C / SPI interfaces.

5.2 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendation are available at www.st.com/mems.

5.3 High current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth’s magnetic field leading to errors in compass-heading computation.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

6 Digital interfaces

The registers embedded in the LSM9DS0 may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped to the same pins. To select/exploit the I^2C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS	I^2C/SPI mode selection 1: SPI idle mode / I^2C communication enabled 0: SPI communication mode / I^2C disabled
SCL/SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I^2C less significant bit of the device address

6.1 I^2C serial interface

The LSM9DS0 I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its own address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM9DS0 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) will be transmitted: the 7 LSb represents the actual register address while the MSB enables the address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) will be automatically increased to allow multiple data read/writes.

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DAT A		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can’t receive another complete byte of data until it has performed

some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

Default address:

The **SDO**/**SA0** pins (SDO_XM/SA0_XM or SDO_G/SA0_G) can be used to modify the least significant bit of the device address. If the SA0 pin is connected to the voltage supply, LSb is '1' (ex. address 0011101b) else if SA0 pad is connected to ground, the LSb value is '0' (ex. address 0011110b).

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with the direction unchanged. *Table 15* and *Table 16* explain how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Linear acceleration and magnetic sensor address:

Table 15. Linear acceleration and magnetic sensor SAD+read/write patterns

Command	SDO_XM/SA0_XM pin	SAD[6:2]	SAD[1:0]	R/W	SAD+R/W
Read	0	00111	10	1	00111101 (3D)
Write	0	00111	10	0	00111100 (3C)
Read	1	00111	01	1	00111011 (3B)
Write	1	00111	01	0	00111010 (3A)

Angular rate sensor address:

Table 16. Angular rate SAD+read/write patterns

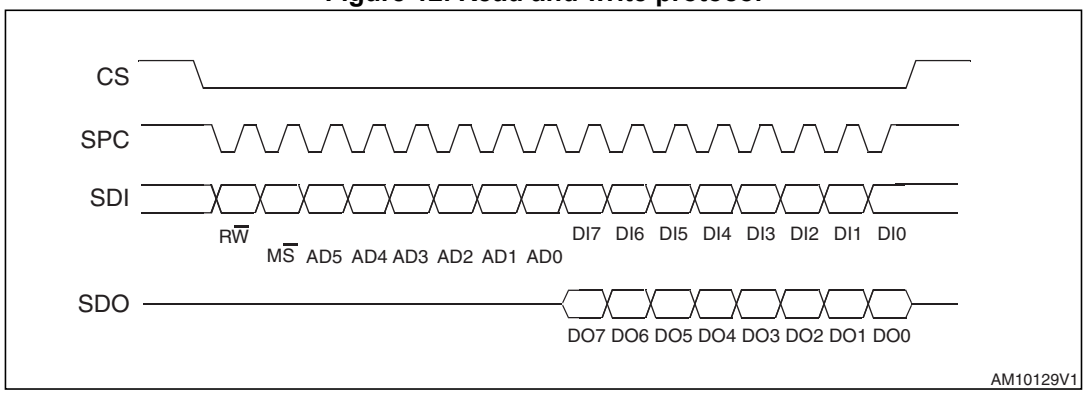
Command	SAD[6:1]	SAD[0] = SDO_G/SA0_G pin	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

6.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 12. Read and write protocol



CS is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

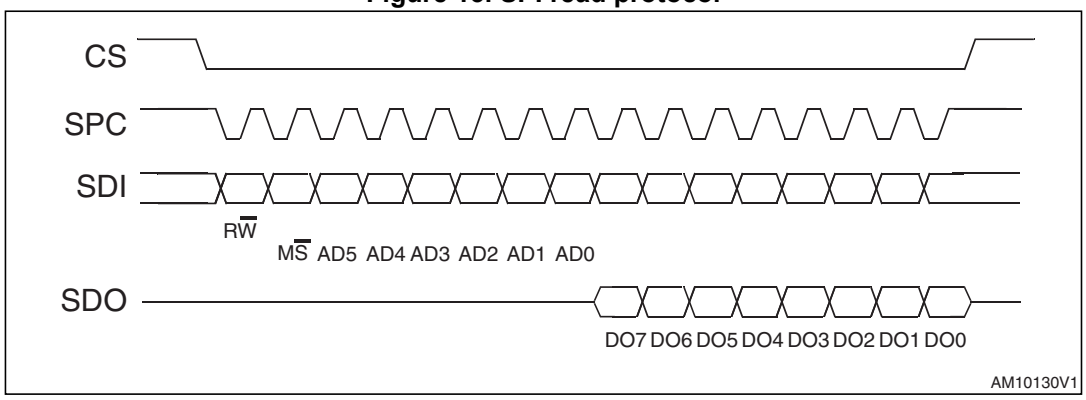
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 13. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

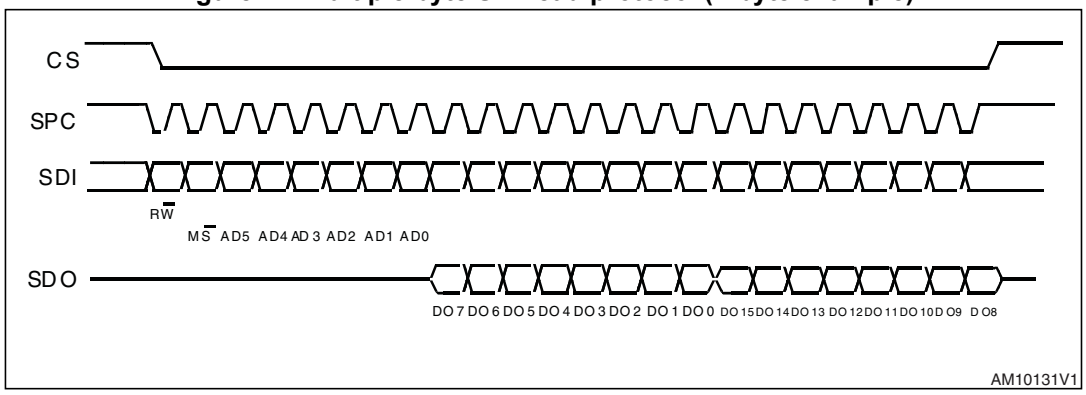
bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

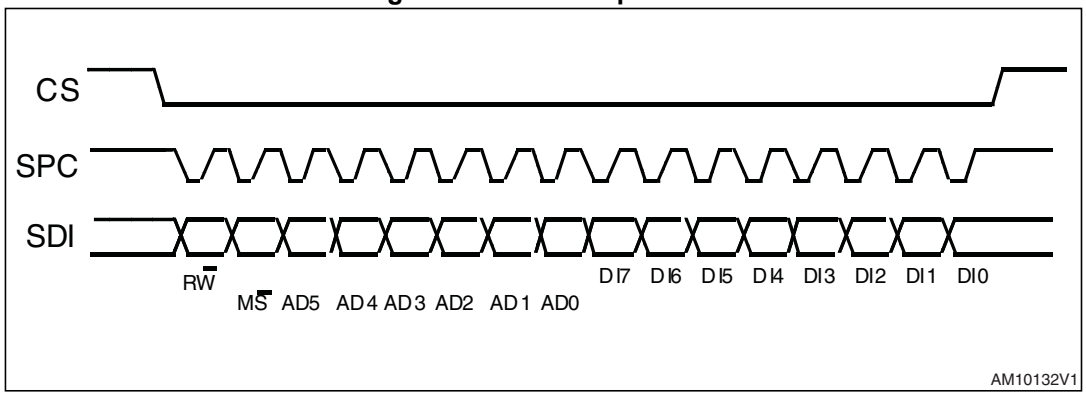
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 14. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 15. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

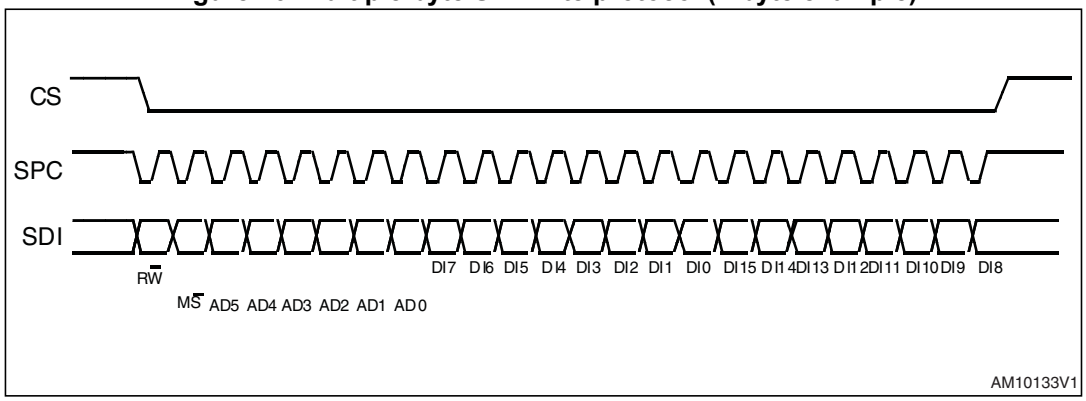
bit 1: MS bit. When 0, does not increment address; when 1, increments address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

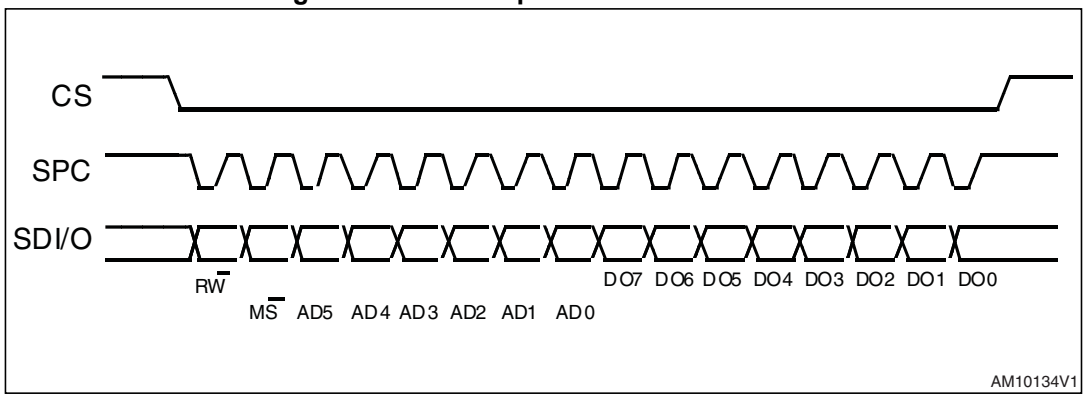
Figure 16. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to ‘1’ in *CTRL_REG2_XM (21h)* for the accelerometer and magnetic sensor and in *CTRL_REG4_G (23h)* for the gyroscope.

Figure 17. SPI read protocol in 3-wire mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: M$\overline{S}$ bit. When 0, does not increment address; when 1, increments address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

The multiple read command is also available in 3-wire mode.

7 Register mapping

The table given below provides a listing of the 8-bit registers embedded in the device and their respective addresses.

Table 17. Register address map

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
Reserved	*Table 16*	--	00-0E	--	--
WHO_AM_I_G	*Table 16*	r	0F	000 1111	11010100
Reserved	*Table 16*	--	10-1F	--	--
CTRL_REG1_G	*Table 16*	rw	20	010 0000	00000111
CTRL_REG2_G	*Table 16*	rw	21	010 0001	00000000
CTRL_REG3_G	*Table 16*	rw	22	010 0010	00000000
CTRL_REG4_G	*Table 16*	rw	23	010 0011	00000000
CTRL_REG5_G	*Table 16*	rw	24	010 0100	00000000
REFERENCE_G	*Table 16*	rw	25	010 0101	00000000
Reserved	*Table 16*	--	26	--	--
STATUS_REG_G	*Table 16*	r	27	010 0111	output
OUT_X_L_G	*Table 16*	r	28	010 1000	output
OUT_X_H_G	*Table 16*	r	29	010 1001	output
OUT_Y_L_G	*Table 16*	r	2A	010 1010	output
OUT_Y_H_G	*Table 16*	r	2B	010 1011	output
OUT_Z_L_G	*Table 16*	r	2C	010 1100	output
OUT_Z_H_G	*Table 16*	r	2D	010 1101	output
FIFO_CTRL_REG_G	*Table 16*	rw	2E	010 1110	00000000
FIFO_SRC_REG_G	*Table 16*	r	2F	010 1111	output
INT1_CFG_G	*Table 16*	rw	30	011 0000	00000000
INT1_SRC_G	*Table 16*	r	31	011 0001	output
INT1_TSH_XH_G	*Table 16*	rw	32	011 0010	00000000
INT1_TSH_XL_G	*Table 16*	rw	33	011 0011	00000000
INT1_TSH_YH_G	*Table 16*	rw	34	011 0100	00000000
INT1_TSH_YL_G	*Table 16*	rw	35	011 0101	00000000
INT1_TSH_ZH_G	*Table 16*	rw	36	011 0110	00000000
INT1_TSH_ZL_G	*Table 16*	rw	37	011 0111	00000000
INT1_DURATION_G	*Table 16*	rw	38	011 1000	00000000
Reserved	*Table 15*	--	00-04	--	--

Table 17. Register address map (continued)

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
OUT_TEMP_L_XM	Table 15	r	05	000 0101	output
OUT_TEMP_H_XM	Table 15	r	06	000 0110	output
STATUS_REG_M	Table 15	r	07	000 0111	output
OUT_X_L_M	Table 15	r	08	000 1000	output
OUT_X_H_M	Table 15	r	09	000 1001	output
OUT_Y_L_M	Table 15	r	0A	000 1010	output
OUT_Y_H_M	Table 15	r	0B	000 1011	output
OUT_Z_L_M	Table 15	r	0C	000 1100	output
OUT_Z_H_M	Table 15	r	0D	000 1101	output
Reserved	Table 15	--	0E	000 1110	--
WHO_AM_I_XM	Table 15	r	0F	000 1111	01001001
Reserved	Table 15	--	10-11	--	--
INT_CTRL_REG_M	Table 15	rw	12	001 0010	11101000
INT_SRC_REG_M	Table 15	r	13	001 0011	output
INT_THS_L_M	Table 15	rw	14	001 0100	00000000
INT_THS_H_M	Table 15	rw	15	001 0101	00000000
OFFSET_X_L_M	Table 15	rw	16	001 0110	00000000
OFFSET_X_H_M	Table 15	rw	17	001 0111	00000000
OFFSET_Y_L_M	Table 15	rw	18	001 01000	00000000
OFFSET_Y_H_M	Table 15	rw	19	001 01001	00000000
OFFSET_Z_L_M	Table 15	rw	1A	001 01010	00000000
OFFSET_Z_H_M	Table 15	rw	1B	001 01011	00000000
REFERENCE_X	Table 15	rw	1C	001 01100	00000000
REFERENCE_Y	Table 15	rw	1D	001 01101	00000000
REFERENCE_Z	Table 15	rw	1E	001 01110	00000000
CTRL_REG0_XM	Table 15	rw	1F	001 1111	00000000
CTRL_REG1_XM	Table 15	rw	20	010 0000	00000111
CTRL_REG2_XM	Table 15	rw	21	010 0001	00000000
CTRL_REG3_XM	Table 15	rw	22	010 0010	00000000
CTRL_REG4_XM	Table 15	rw	23	010 0011	00000000
CTRL_REG5_XM	Table 15	rw	24	010 0100	00011000
CTRL_REG6_XM	Table 15	rw	25	010 0101	00100000
CTRL_REG7_XM	Table 15	rw	26	010 0110	00000001

Table 17. Register address map (continued)

Name	Slave Address	Type	Register address		Default
			Hex	Binary	
STATUS_REG_A	Table 15	r	27	010 0111	output
OUT_X_L_A	Table 15	r	28	010 1000	output
OUT_X_H_A	Table 15	r	29	010 1001	output
OUT_Y_L_A	Table 15	r	2A	010 1010	output
OUT_Y_H_A	Table 15	r	2B	010 1011	output
OUT_Z_L_A	Table 15	r	2C	010 1100	output
OUT_Z_H_A	Table 15	r	2D	010 1101	output
FIFO_CTRL_REG	Table 15	rw	2E	010 1110	00000000
FIFO_SRC_REG	Table 15	r	2F	010 1111	output
INT_GEN_1_REG	Table 15	rw	30	011 0000	00000000
INT_GEN_1_SRC	Table 15	r	31	011 0001	output
INT_GEN_1_THS	Table 15	rw	32	011 0010	00000000
INT_GEN_1_DURATION	Table 15	rw	33	011 0011	00000000
INT_GEN_2_REG	Table 15	rw	34	011 0100	00000000
INT_GEN_2_SRC	Table 15	r	35	011 0101	output
INT_GEN_2_THS	Table 15	rw	36	011 0110	00000000
INT_GEN_2_DURATION	Table 15	rw	37	011 0111	00000000
CLICK_CFG	Table 15	rw	38	011 1000	00000000
CLICK_SRC	Table 15	r	39	011 1001	output
CLICK_THS	Table 15	rw	3A	011 1010	00000000
TIME_LIMIT	Table 15	rw	3B	011 1011	00000000
TIME _LATENCY	Table 15	rw	3C	011 1100	00000000
TIME_WINDOW	Table 15	rw	3D	011 1101	00000000
Act_THS	Table 15	rw	3E	011 1110	00000000
Act_DUR	Table 15	rw	3F	011 1111	00000000

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory-calibrated values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 WHO_AM_I_G (0Fh)

Table 18. WHO_AM_I_G register

1	1	0	1	0	1	0	0

Device identification register.

8.2 CTRL_REG1_G (20h)

Table 19. CTRL_REG1_G register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 20. CTRL_REG1_G description

DR1-DR0	Output data rate selection. Refer to *Table 21*
BW1-BW0	Bandwidth selection. Refer to *Table 21*
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

DR[1:0] is used for ODR selection. **BW [1:0]** is used for Bandwidth selection.

In *Table 21* all frequencies resulting in combinations of DR / BW bits are given.

Table 21. DR and BW configuration setting

DR [1:0]	BW [1:0]	ODR (Hz)	Cutoff
00	00	95	12.5
00	01	95	25
00	10	95	25

Table 21. DR and BW configuration setting (continued)

DR [1:0]	BW [1:0]	ODR (Hz)	Cutoff
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD, Zen, Yen, Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with *Table 22* below.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

8.3 CTRL_REG2_G (21h)

Table 23. CTRL_REG2_G register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. These bits must be set to ‘0’ to ensure proper operation of the device

Table 24. CTRL_REG2_G description

HPM1-HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 25*
HPCF3-HPCF0	High-pass filter cutoff frequency selection Refer to *Table 26*

Table 25. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High-pass filter cutoff frequency configuration (Hz)

HPCF[3:0]	ODR = 95 Hz	ODR = 190 Hz	ODR = 380 Hz	ODR = 760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

8.4 CTRL_REG3_G (22h)

Table 27. CTRL_REG3_G register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 28. CTRL_REG3_G description

I1_Int1	Interrupt enable on INT_G pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT_G. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT_G. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push- pull; 1: open drain)
I2_DRDY	Date-ready on DRDY_G. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY_G. Default value: 0. (0: disable; 1: enable)

8.5 CTRL_REG4_G (23h)

Table 29. CTRL_REG4_G register

BDU	BLE	FS1	FS0	-	ST1	ST0	SIM

Table 30. CTRL_REG4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb read)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full-scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
ST1-ST0	Self-test enable. Default value: 00 (00: Self-test disabled; Other: See *Table 31*)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

Table 31. Self-test mode configuration

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self-test 0 (1)(X positive sign, Y and Z negative sign)
1	0	--
1	1	Self-test 1 (1) (X negative sign, Y and Z positive sign)

1. DST sign (absolute value in *Table 3*)

8.6 CTRL_REG5_G (24h)

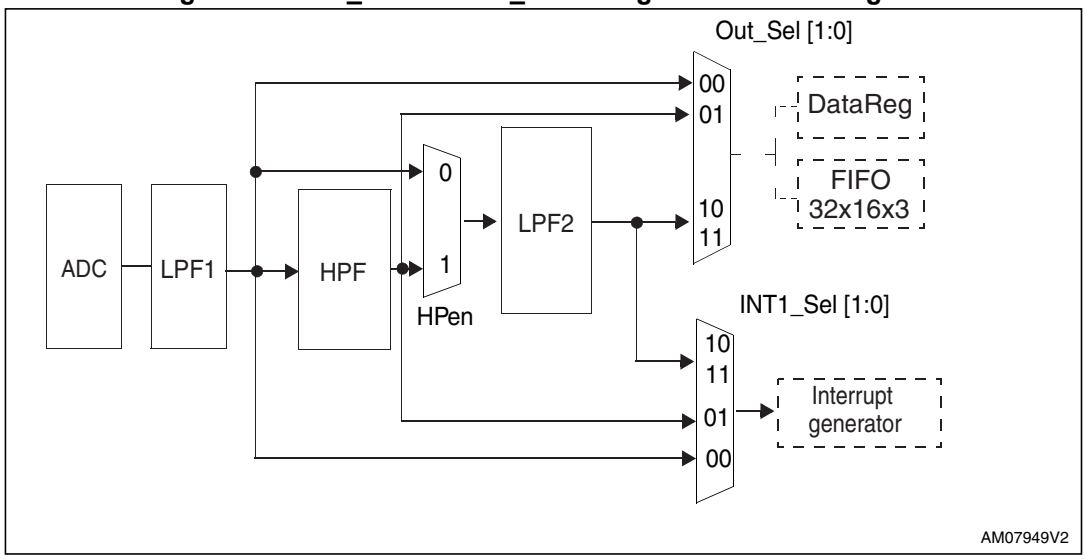
Table 32. CTRL_REG5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

Table 33. CTRL_REG5_G description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled) (See *Figure 18*)
INT1_Sel1-INT1_Sel0	INT1 selection configuration. Default value: 00 (See *Figure 18*)
Out_Sel1-Out_Sel0	Out selection configuration. Default value: 00 (See *Figure 18*)

Figure 18. INT1_Sel and Out_Sel configuration block diagram



8.7 REFERENCE/DATACAPTURE_G (25h)

Table 34. REFERENCE/DATACAPTURE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 35. REFERENCE/DATACAPTURE_G description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

8.8 STATUS_REG_G (27h)

Table 36. STATUS_REG_G register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 37. STATUS_REG_G description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)

Table 37. STATUS_REG_G description (continued)

ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.9 OUT_X_L_G (28h), OUT_X_H_G (29h)

X-axis angular rate data. The value is expressed as two's complement.

8.10 OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

8.11 OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

8.12 FIFO_CTRL_REG_G (2Eh)

Table 38. FIFO_CTRL_REG_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 39. FIFO_CTRL_REG_G description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 40*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 40. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

8.13 FIFO_SRC_REG_G (2Fh)

Table 41. FIFO_SRC_REG_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 42. FIFO_SRC_REG_G description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal to or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1: FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

8.14 INT1_CFG_G (30h)

Table 43. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 44. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

Table 44. INT1_CFG_G description (continued)

XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

8.15 INT1_SRC_G (31h)

Interrupt source register. Read-only register.

Table 45. INT1_SRC_G register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 46. INT1_SRC_G description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the INT1_SRC IA bit (and eventually the interrupt signal on the INT_G pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

8.16 INT1_THS_XH_G (32h)

Table 47. INT1_THS_XH_G register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 48. INT1_THS_XH_G description

THSX14 - THSX8	Interrupt threshold. Default value: 000 0000

8.17 INT1_THS_XL_G (33h)

Table 49. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 50. INT1_THS_XL_G description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

8.18 INT1_THS_YH_G (34h)

Table 51. INT1_THS_YH_G register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 52. INT1_THS_YH_G description

THSY14 - THSY8	Interrupt threshold. Default value: 000 0000

8.19 INT1_THS_YL_G (35h)

Table 53. INT1_THS_YL_G register

THSR7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 54. INT1_THS_YL_G description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

8.20 INT1_THS_ZH_G (36h)

Table 55. INT1_THS_ZH_G register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 56. INT1_THS_ZH_G description

THSZ14 - THSZ8	Interrupt threshold. Default value: 000 0000

8.21 INT1_THS_ZL_G (37h)

Table 57. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 58. INT1_THS_ZL_G description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

8.22 INT1_DURATION_G (38h)

Table 59. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 60. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = ‘0’: the interrupt falls immediately if the signal crosses the selected threshold

Wait = ‘1’: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait bit disabled

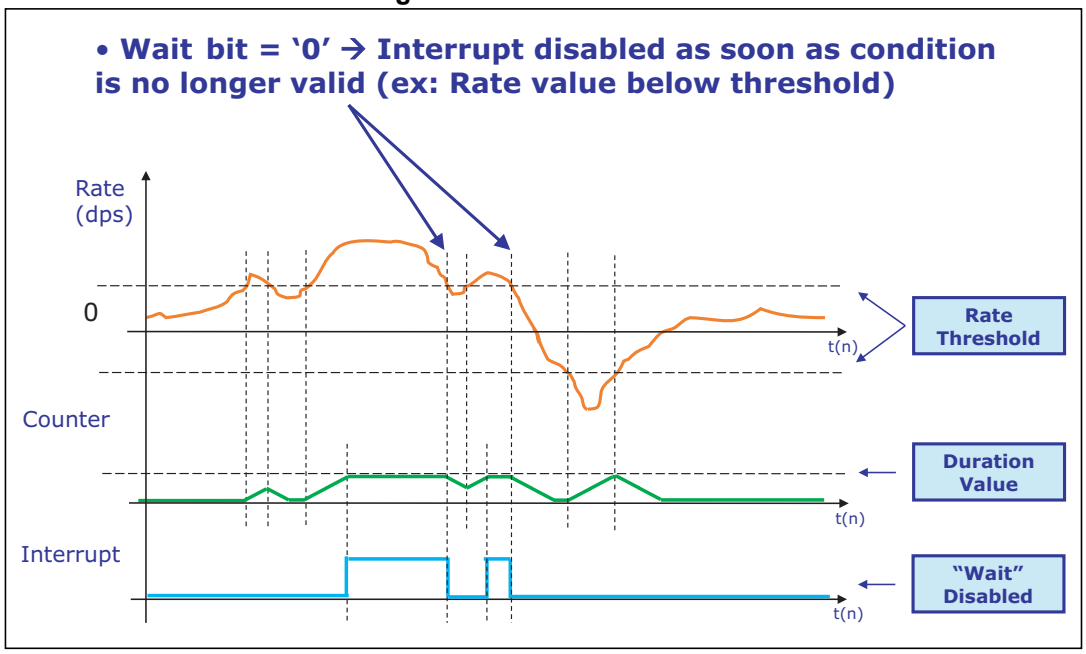
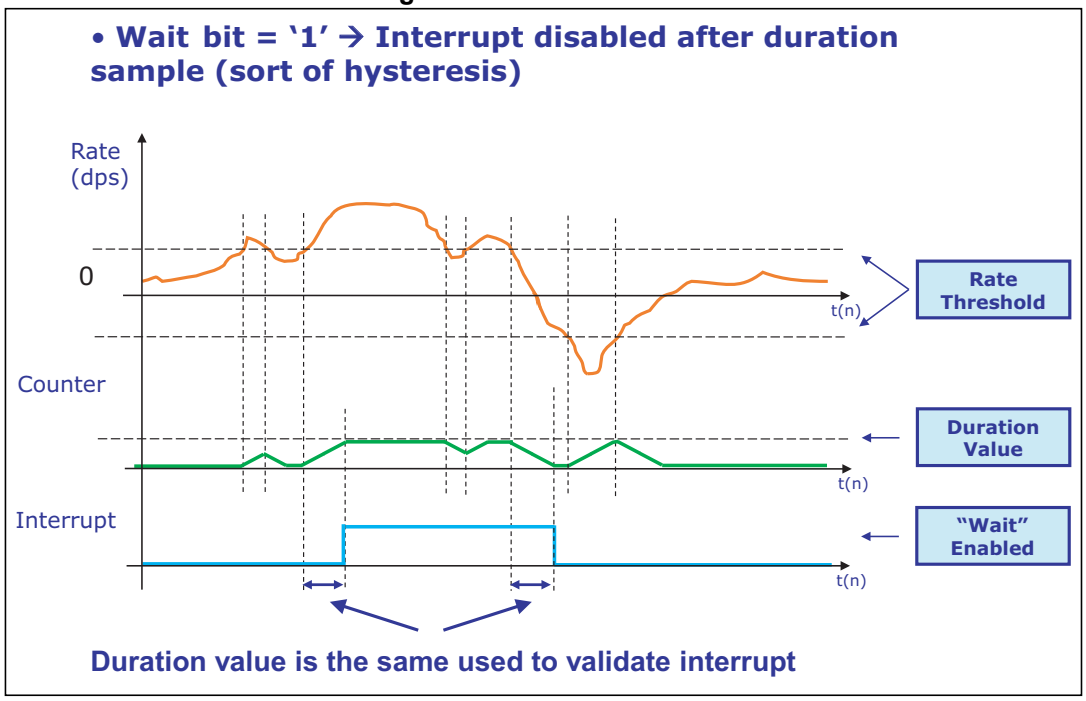


Figure 20. Wait bit enabled



8.23 OUT_TEMP_L_XM (05h), OUT_TEMP_H_XM (06h)

Temperature sensor data.

Refer to *Section 4.4: Temperature sensor* for details on how to enable and read the temperature sensor output data.

8.24 STATUS_REG_M (07h)

Table 61. STATUS_REG_M register

ZYXMOR	ZMOR	YMOR	XMOR	ZYXMDA	ZMDA	YMDA	XMDA

Table 62. STATUS_REG_M description

ZYXMOR	Magnetic X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous ones).
ZMOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YMOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XMOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXMDA	X, Y and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available).
ZMDA	Z-axis new data available. Default value: 0 (0: a new set of data for the Z-axis is not yet available; 1: a new set of data for the Z-axis is available)
YMDA	Y-axis new data available. Default value: 0 (0: a new set of data for the Y-axis is not yet available; 1: a new set of data for the Y-axis is available)
XMDA	X-axis new data available. Default value: 0 (0: a new set of data for the X-axis is not yet available; 1: a new set of data for the X-axis is available)

8.25 OUT_X_L_M (08h), OUT_X_H_M (09h)

X-axis magnetic data.

The value is expressed in 16-bit as two’s complement left justified.

8.26 OUT_Y_L_M (0Ah), OUT_Y_H_M (0Bh)

Y-axis magnetic data.

The value is expressed in 16-bit as two’s complement left justified.

8.27 OUT_Z_L_M (0Ch), OUT_Z_H_M (0Dh)

Z-axis magnetic data.

The value is expressed in 16-bit as two's complement left justified.

8.28 WHO_AM_I_XM (0Fh)

Table 63. WHO_AM_I_XM register

0	1	0	0	1	0	0	1

Device identification register.

8.29 INT_CTRL_REG_M (12h)

Table 64. INT_CTRL_REG_M register

XMIEN	YMIEN	ZMIEN	PP_OD	IEA	IEL	4D	MIEN

Table 65. INT_CTRL_REG_M description

XMIEN	Enable interrupt recognition on X-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
YMIEN	Enable interrupt recognition on Y-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
ZMIEN	Enable interrupt recognition on Z-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
PP_OD	Interrupt pin configuration. Default value: 0. (0: push-pull; 1: open drain)
IEA	Interrupt polarity for both accelerometer and magnetometer. Default value: 0. (0: interrupt active-low; 1: interrupt active-high)
IEL	Latch interrupt request on accelerometer *INT_GEN_1_SRC (31h)* and *INT_GEN_2_SRC (35h)* registers, and magnetometer *INT_SRC_REG_M (13h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched) Once the IEL is set to '1' the interrupt is cleared by reading for the accelerometer the *INT_GEN_1_SRC (31h)* and *INT_GEN_2_SRC (35h)* registers, and for the magnetometer the *INT_SRC_REG_M (13h)* register.
4D	4D enable: 4D detection on acceleration data is enabled when 6D bit in *INT_GEN_1_REG (30h)* is set to 1.
MIEN	Enable interrupt generation for magnetic data. Default value: 0. (0: disable interrupt generation;1: enable interrupt generation)

8.30 INT_SRC_REG_M (13h)

Table 66. INT_SRC_REG_M register

M_PTH_X	M_PTH_Y	M_PTH_Z	M_NTH_X	M_NTH_Y	M_NTH_Z	MROI	MINT

Table 67. INT_SRC_REG_M description

M_PTH_X	Magnetic value on X-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Y	Magnetic value on Y-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Z	Magnetic value on Z-axis exceeds the threshold on the positive side. Default value: 0.
M_NTH_X	Magnetic value on X-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Y	Magnetic value on Y-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Z	Magnetic value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0. To enable this feature need to set to 1 MIEN bit in *8.29: INT_CTRL_REG_M (12h)*
MINT	Magnetic interrupt event. The magnetic field value exceeds the threshold. Default value: 0.

8.31 INT_THS_L_M (14h), INT_THS_H_M (15h)

Magnetic interrupt threshold. Default value: 0.

The value is expressed in 16-bit unsigned.

Even if the threshold is expressed in absolute value, the device detects both positive and negative thresholds.

8.32 OFFSET_X_L_M (16h), OFFSET_X_H_M (17h)

Magnetic offset for X-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.33 OFFSET_Y_L_M (18h), OFFSET_Y_H_M (19h)

Magnetic offset for Z-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.34 OFFSET_Z_L_M (1Ah), OFFSET_Z_H_M (1Bh)

Magnetic offset for Y-axis. Default value: 0.

The value is expressed in 16-bit as two’s complement left justified.

8.35 REFERENCE_X (1Ch)

Reference value for high-pass filter for x-axis acceleration data.

8.36 REFERENCE_Y (1Dh)

Reference value for high-pass filter for y-axis acceleration data.

8.37 REFERENCE_Z (1Eh)

Reference value for high-pass filter for z-axis acceleration data.

8.38 CTRL_REG0_XM (1Fh)

Table 68. CTRL_REG0_XM register

BOOT	FIFO_EN	WTM_EN	0(1)	0(1)	HP_Click	HPIS1	HPIS2

1. These bits must be set to '0' for the correct operation of the device

Table 69. CTRL_REG0_XM description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
WTM_EN	FIFO programmable watermark enable. Default value: 0 (0: disable; 1: Enable)
HP_Click	High-pass filter enabled for Click function. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for interrupt generator 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.39 CTRL_REG1_XM (20h)

Table 70. CTRL_REG1_XM register

AODR3	AODR2	AODR1	AODR0	BDU	AZEN	AYEN	AXEN

Table 71. CTRL_REG1_XM description

AODR3-AODR0	Acceleration data rate selection. Default value: 0000 (0000: power-down mode; others: refer to *Table 72: Acceleration data rate configuration*)
BDU	Block data update for acceleration and magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
AZEN	Acceleration Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
AYEN	Acceleration Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
AXEN	Acceleration X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

AODR[3:0] is used to set the power mode and ODR selection. The following table indicates all frequencies resulting from the combination of AODR[3:0].

Table 72. Acceleration data rate configuration

AODR3	AODR2	AODR1	AODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	200 Hz
1	0	0	0	400 Hz
1	0	0	1	800 Hz
1	0	1	0	1600 Hz

8.40 CTRL_REG2_XM (21h)

Table 73. CTRL_REG2_XM register

ABW1	ABW0	AFS2	AFS1	AFS0	AST1	AST0	SIM

Table 74. CTRL_REG2_XM description

ABW[1:0]	Accelerometer anti-alias filter bandwidth. Default value: 00 Refer to *Table 75: Acceleration anti-alias filter bandwidth*
AFS[2:0]	Acceleration full-scale selection. Default value: 000 Refer to *Table 76: Acceleration full-scale selection*
AST[1:0]	Acceleration self-test enable. Default value: 00 (00: self-test disabled; see *Table 77: Self-test mode configuration*)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 75. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
0	0	773 Hz
0	1	194 Hz
1	0	362 Hz
1	1	50 Hz

Table 76. Acceleration full-scale selection

AFS2	AFS1	AFS0	Acceleration full scale
0	0	0	±2 *g*
0	0	1	±4 *g*
0	1	0	±6 *g*
0	1	1	±8 *g*
1	0	0	±16 *g*

Table 77. Self-test mode configuration

AST1	AST0	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

8.41 CTRL_REG3_XM (22h)

Table 78. CTRL_REG3_XM register

P1_BOOT	P1_TAP	P1_INT1	P1_INT2	P1_INTM	P1_DRDYA	P1_DRDYM	P1_EMPTY

Table 79. CTRL_REG3_XM description

P1_BOOT	Boot on INT1_XM pin enable. Default value: 0 (0: disable; 1: enable)
P1_TAP	Tap generator interrupt on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INT1	Inertial interrupt generator 1 on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INT2	Inertial interrupt generator 2 on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_INTM	Magnetic interrupt generator on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYA	Accelerometer data-ready signal on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYM	Magnetometer data-ready signal on INT1_XM pin. Default value: 0 (0: disable; 1: enable)
P1_EMPTY	FIFO empty indication on INT1_XM pin. Default value: 0 (0: disable; 1: enable)

8.42 CTRL_REG4_XM (23h)

Table 80. CTRL_REG4_XM register

P2_TAP	P2_INT1	P2_INT2	P2_INTM	P2_DRDYA	P2_DRDYM	P2_Overrun	P2_WTM

Table 81. CTRL_REG4_XM description

P2_TAP	Tap generator interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INT1	Inertial interrupt generator 1 on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INT2	Inertial interrupt generator 2 on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_INTM	Magnetic interrupt generator on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYA	Accelerometer data-ready signal on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYM	Magnetometer data-ready signal on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_Overrun	FIFO overrun interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)
P2_WTM	FIFO watermark interrupt on INT2_XM pin. Default value: 0 (0: disable; 1: enable)

8.43 CTRL_REG5_XM (24h)

Table 82. CTRL_REG5_XM register

TEMP_EN	M_RES1	M_RES0	M_ODR2	M_ODR1	M_ODR0	LIR2	LIR1

Table 83. CTRL_REG5_XM description

TEMP_EN	Temperature sensor enable. Default value: 0 (0: temperature sensor disabled; 1: temperature sensor enabled)
M_RES[1:0]	Magnetic resolution selection. Default value: 00 (00: low resolution, 11: high resolution)
M_ODR[2:0]	Magnetic data rate selection. Default value: 110 Refer to *Table 84: Magnetic data rate configuration*
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)

Table 84. Magnetic data rate configuration

M_ODR2	M_ODR1	M_ODR0	Power mode selection
0	0	0	3.125 Hz
0	0	1	6.25 Hz
0	1	0	12.5 Hz
0	1	1	25 Hz
1	0	0	50 Hz
1	0	1	100 Hz(1)
1	1	0	Reserved
1	1	1	Reserved

1. Available only for accelerometer ODR > 50 Hz or accelerometer in power-down mode (refer to *Table 72,* AODR setting).

8.44 CTRL_REG6_XM (25h)

Table 85. CTRL_REG6_XM register

0(1)	MFS1	MFS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to ‘0’ for the correct operation of the device

Table 86. CTRL_REG6_XM description

MFS1-MFS0	Magnetic full-scale selection. Default value: 01 Refer to *Table 87: Magnetic full-scale selection*

Table 87. Magnetic full-scale selection

MFS1	MFS0	Magnetic full scale
0	0	± 2 gauss
0	1	± 4 gauss
1	0	± 8 gauss
1	1	± 12 gauss

8.45 CTRL_REG7_XM (26h)

Table 88. CTRL_REG7_XM register

AHPM1	AHPM0	AFDS	0(1)	0(1)	MLP	MD1	MD0

1. These bits must be set to '0' for the correct operation of the device

Table 89. CTRL_REG7_XM description

AHPM1-AHPM0	High-pass filter mode selection for acceleration data. Default value: 00 Refer to *Table 90: High-pass filter mode selection*
AFDS	Filtered acceleration data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
MLP	Magnetic data low-power mode. Default value: 0 If this bit is '1' the MODR is set to 3.125 Hz independently from the MODR settings. Once the bit is set to '0' the magnetic data rate is configured by MODR bits in *CTRL_REG5_XM (24h)* register.
MD1-MD0	Magnetic sensor mode selection. Default 10 Refer to *Table 91: Magnetic sensor mode selection*

Table 90. High-pass filter mode selection

AHPM1	AHPM0	High-pass filter mode
0	0	Normal mode (resets x, y and z-axis reading *REFERENCE_X (1Ch)*, *REFERENCE_Y (1Dh)* and *REFERENCE_Y (1Dh)* registers respectively)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 91. Magnetic sensor mode selection

MD1-0	MD1-0	Magnetic sensor mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.46 STATUS_REG_A (27h)

Table 92. STATUS_REG_A register

ZYXAOR	ZAOR	YAOR	XAOR	ZYXADA	ZADA	YADA	XADA

Table 93. STATUS_REG_A description

ZYXAOR	Acceleration X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous one)
ZAOR	Acceleration Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the Z-axis has overwritten the previous one)
YAOR	Acceleration Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the Y-axis has overwritten the previous one)
XAOR	Acceleration X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data for the X-axis has overwritten the previous one)
ZYXADA	Acceleration X-, Y- and Z-axis new value available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZADA	Acceleration Z-axis new value available. Default value: 0 (0: a new set of data for the Z-axis is not yet available; 1: a new set of data for the Z-axis is available)
YADA	Acceleration Y-axis new value available. Default value: 0 (0: a new set of data for the Y-axis is not yet available; 1: a new set of data for the Y-axis is available)
XADA	Acceleration X-axis new value available. Default value: 0 (0: a new set of data for the X-axis is not yet available; 1: a new set of data for the X-axis is available)

8.47 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data.

The value is expressed in 16 bit as two’s complement left justified.

8.48 OUT_Y_L_A (2Ah), OUT_Y_H_A (2Bh)

Y-axis acceleration data.

The value is expressed in 16-bit as two's complement left justified.

8.49 OUT_Z_L_A (2Ch), OUT_Z_H_A (2Dh)

Z-axis acceleration data.

The value is expressed in 16-bit as two's complement left justified.

8.50 FIFO_CTRL_REG (2Eh)

Table 94. FIFO_CTRL_REG register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 95. FIFO_CTRL_REG description

FM2-FM0	FIFO mode selection. Default value: 000
FTH4-FTH0	FIFO watermark level. Default value: 00000

Table 96. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

Interrupt generator 2 can change the FIFO mode.

8.51 FIFO_SRC_REG (2Fh)

Table 97. FIFO_SRC_REG register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 98. FIFO_SRC_REG description

WTM	Watermark status. WTM bit is set to '1' when FIFO content exceeds watermark level.
OVRN	FIFO Overrun status. OVRN bit is set to '1' when FIFO buffer is full.

Table 98. FIFO_SRC_REG description (continued)

EMPTY	Empty status. EMPTY bit is set to '1' when all FIFO samples have been read and FIFO is empty.
FSS4-FSS0	FIFO stored data level. FSS4-FSS0 bits contain the current number of unread FIFO levels.

8.52 INT_GEN_1_REG (30h)

This register contains the settings for the inertial interrupt generator 1.

Table 99. INT_GEN_1_REG register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 100. INT_GEN_1_REG description

AOI	And/Or combination of Interrupt events. Default value: 0. Refer to *Table 101: Interrupt mode*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 101: Interrupt mode*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Table 101. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’ is as follows:

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal stays until the orientation is inside the zone.

8.53 INT_GEN_1_SRC (31h)

This register contains the status for the inertial interrupt generator 1.

Table 102. INT_GEN_1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 103. INT_GEN_1_SRC description

IA	Interrupt Status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_1_SRC (31h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_1_SRC (31h)* register if the latched option was chosen.

8.54 INT_GEN_1_THS (32h)

Table 104. INT1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 105. INT1_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.55 INT_GEN_1_DURATION (33h)

Table 106. INT1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 107. INT1_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.56 INT_GEN_2_REG (34h)

This register contains the settings for the inertial interrupt generator 2.

Table 108. INT_GEN_2_REG register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 109. INT_GEN_2_REG description

AOI	And/Or combination of Interrupt events. Default value: 0. Refer to *Table 109: INT_GEN_2_REG description*
6D	6 direction detection function enabled. Default value: 0. Refer to *Table 109: INT_GEN_2_REG description*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWNE	Enable interrupt generation on X low event or on Direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Table 110. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’ is as follows:

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal stays until the orientation is inside the zone.

8.57 INT_GEN_2_SRC (35h)

This register contains the status for the inertial interrupt generator 2.

Table 111. INT_GEN_2_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 112. INT_GEN_2_SRC description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_2_SRC (35h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_2_SRC (35h)* register if the latched option was chosen.

8.58 INT_GEN_2_THS (36h)

Table 113. INT_GEN_2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 114. INT_GEN_2_THS description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.59 INT_GEN_2_DURATION (37h)

Table 115. INT_GEN_2_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 116. INT_GEN_2_DURATION description

D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.60 CLICK_CFG (38h)

Table 117. CLICK_CFG register

--	--	ZD	ZS	YD	YS	XD	XS

Table 118. CLICK_CFG description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

Table 118. CLICK_CFG description

XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.61 CLICK_SRC (39h)

Table 119. CLICK_SRC register

--	IA	DClick	SClick	Sign	Z	Y	X

Table 120. CLICK_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double-click enable. Default value: 0 (0: double-click detection disabled, 1: double-click detection enabled)
SClick	Single-click enable. Default value: 0 (0: single-click detection disabled, 1: single-click detection enabled)
Sign	Click sign. 0: positive detection, 1: negative detection
Z	Z click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

8.62 CLICK_THS (3Ah)

Table 121. CLICK_THS register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 122. CLICK_SRC description

Ths6-Ths0	Click threshold. Default value: 000 0000

8.63 TIME_LIMIT (3Bh)

Table 123. TIME_LIMIT register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 124. TIME_LIMIT description

TLI7-TLI0	Click time limit. Default value: 000 0000

8.64 TIME_LATENCY (3Ch)

Table 125. TIME_LATENCY register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 126. TIME_LATENCY description

TLA7-TLA0	Click time latency. Default value: 0000 0000

8.65 TIME WINDOW (3Dh)

Table 127. TIME_WINDOW register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 128. TIME_WINDOW description

TW7-TW0	Click time window

8.66 Act_THS (3Eh)

Table 129. TIME_WINDOW register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 130. TIME_WINDOW description

Acth[6:0]	Sleep-to-Wake, Return-to-Sleep activation threshold 1 LSb = 16 mg

8.67 Act_DUR (3Fh)

Table 131. Act_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 132. Act_DUR description

ActD[7:0]	Sleep-to-Wake, Return-to-Sleep duration DUR = (Act_DUR + 1)*8/ODR

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 133. LGA 4x4x1 mm 24-lead mechanical data (see note 1 and 2)

Databook				
Symbol	**Min.**	**Typ.**	**Max.**	**Note**
A			1.070	
A1	0.000	-	0.050	4
b		0.200		7
D		4.000		6
D2		1.750		
E		4.000		6
E2		1.750		
e1		0.500		
e2		2.500		
L		0.350		7
L1	-	0.100	-	
L2	-	0.100	-	
N		24		5
R1	-	0.080	-	

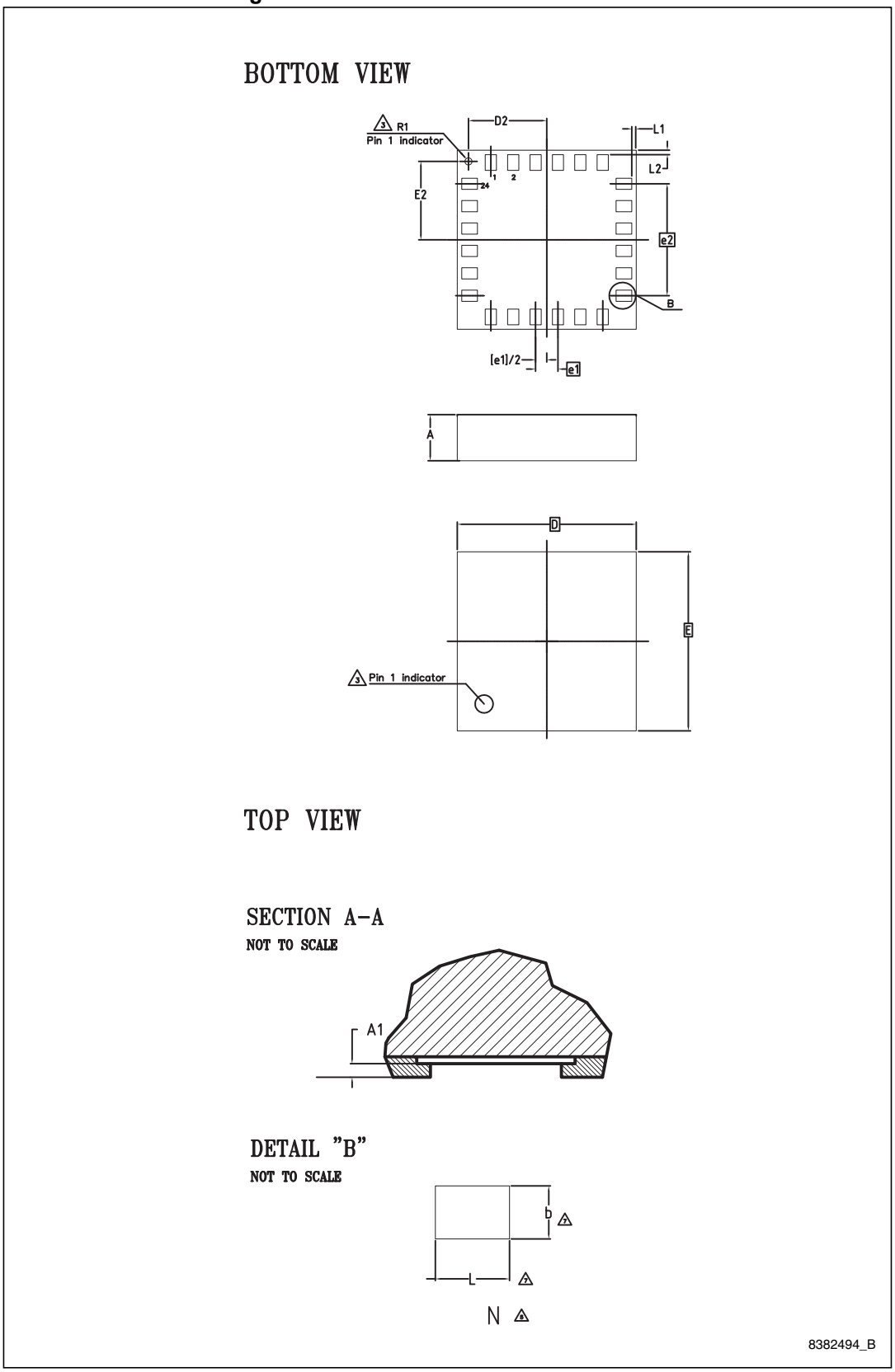
Symbol	**Tolerance of Form and Position**
	Databook
D/E	0.15
Notes	1 and 2
REF	-

Δ

Note:

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *All dimensions are in millimeters.*
3. *The “Pin 1 Indicator” is identified on top and/or bottom surfaces of the package.*
4. *A1 is defined as the distance from the seating plane to the land.*
5. *“N” is the maximum number of terminal positions for the specified body size.*
6. *The tolerance of the typical value is specified in table "Tolerance of Form and Position".*
7. *Dimensions “b” and “L” are specified:*
   For solder mask defined: at terminal plating surface
   For non-solder mask defined: at solder mask opening

Figure 21. LGA 4x4x1 mm 24-lead outline



10 Revision history

Table 134. Document revision history

Date	Revision	Changes
24-Jun-2013	1	Initial release
05-Aug-2013	2	Updated LA_So in *Table 3* Updated *Figure 4*, *Figure 5*, and *Table 7* Updated *Section 5.1* Updated *Section 9: Package information* Minor textual updates throughout *Section 8: Register description*

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