

### 2A Synchronous TDFN3\*3-10L Step-Down Converter

#### ■ FEATURES

- High Efficiency Up to 95%
- Low 300µA Quiescent Current
- Guaranteed 2A Output Current
- 1.2MHz Constant Frequency Operation
- Internal Synchronous Rectifier Eliminates Schottky Diode
- 2.5V to 6V input voltage range
- Adjustable Output Voltages From 0.6V to V<sub>IN</sub>
- Fixed Output Voltage Options Available
- 100% Duty Cycle Low-Dropout Operation
- <1µA Shutdown Current</li>
- Soft start function
- Short circuit protection
- Thermal shutdown protection
- TDFN3\*3-10L Package

### APPLICATIONS

- Microprocessor and DSP core power supplies
- Cellular and smart Phones
- Wireless and DSL Modems
- Portable Instruments

#### GENERAL DESCRIPTION

The LSP3105 is a fixed-frequency current-mode synchronous PWM step down converter that is capable of delivering 2A of output current while achieving peak efficiency of 95%.LSP3105 operates in a 100% Duty Cycle Low-Dropout Operation, maximizing battery life in portable applications. The LSP3105 operates with a fixed frequency of 1.2MHz, allowing the use of small external components. The LSP3105 is an ideal solution for applications powered by Li-Ion batteries or other portable applications that require small board space. The LSP3105 is available in 1.8V fixed output voltage and an adjustable output voltage version capable of generating output voltages from 0.6V to  $V_{IN}$  The LSP3105 is available in the small TDFN3\*3-10L



package.

Figure1. Typical Application Circuit and Efficiency



### 2A Synchronous TDFN3\*3-10L Step-Down Converter

### ■ PIN CONFIGURATION



#### PIN DESCRIPTION

PIN NUMBER	PIN NAME	PIN FUNCTION	
1	EN	Regulator Enable control input. Drive RUN above 1.2V to turn on the part. Drive RUN below 0.6V to turn it off. In shutdown, all functions are disable drawing < $1\mu$ A supply current. Do not leave RUN floating.	
2	IN	Supply Input Pin. Must be closely decoupled to GND, pin2, with a 2.2 $\mu$ F or greater ceramic capacitor.	
3	AIN	Analog supply input pin. Provides bias for internal circuitry.	
4,6	AGND	Analog Power Ground Pin	
5	FB/Out	Out (LSP3105-1.8): Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage. FB (LSP3105): Feedback Input Pin. Connected FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.	
7,8	LX	Power Switch Output. It is the Switch node connection to inductor. This pin connects to the drains of the internal P-CH and N-CH MOSFET switches.	
9,10	PGND	Power Ground Pin	
	EP	Power ground exposed pad. Must be connected to bare copper ground plane.	



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#### **ABSOLUTE MAXIMUM RATINGS**

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

PARAMETER	VALUE	UNIT
IN, FB, EN to G	-0.3 to 6.5	V
SW to G	-0.3 to V <sub>IN</sub> + 0.3	V
Junction to Ambient Thermal Resistance ( $\theta_{JA}$ )	45	°C/W
Junction to Case Thermal Resistance $(\theta_{JC})$	5	°C/W
Maximum Power Dissipation	2.2	W
Operating Junction Temperature	-40 to 125	°C
Storage Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

### ELECTRICAL CHARACTERISTICS

 $(V_{IN} = V_{EN} = 3.6V, T_A = 25^{\circ}C$  unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Range	V <sub>IN</sub>		2.5		6	V
Operating Supply Current		$V_{FB} = 0.5V, I_{OUT} = 0$		300	500	μA
Shutdown Supply Current		$V_{EN} = 0V, V_{IN} = 4.2V$		0.1	1	μA
Adjustable Versian Desulation		T <sub>A</sub> = 25°C	0.5880	0.6000	0.6120	
Voltage (LSP3105WAD)	$V_{FB}$	0 < T <sub>A</sub> < 85°C	0.5865	0.6000	0.6135	V
· · · · · · · · · · · · · · · · · · ·		-40°C < T <sub>A</sub> < 85°C	0.5850	0.6000	0.6150	
Fixed Output Regulation Voltage	V <sub>OUT</sub>	LSP3105L18AD	1.746	1.800	1.854	V
Output Voltage Line Regulation		$V_{IN}$ = 2.5V to 6V, $I_{OUT}$ = 10mA		0.10	0.20	%/V
Output Voltage Load Regulation		I <sub>OUT</sub> = 10mA to 2000mA		0.20		%/A
Inductor Current Limit	I <sub>LIM</sub>		2.5	3.5		Α
Oscillator Frequency	$f_{SW}$	$V_{\text{FB}}$ or $V_{\text{OUT}}$ in regulation	0.96	1.2	1.44	MHz
PMOS On Resistance	R <sub>ONP</sub>	V <sub>IN</sub> = 3.6V		135	200	mΩ
NMOS On Resistance	R <sub>ONN</sub>	V <sub>IN</sub> = 3.6V		95	150	mΩ
SW Leakage Current		$EN = G, V_{IN} = 6V, V_{SW} = 6V \text{ or } 0V$			± 1	μA
RUN Logic High Threshold	V <sub>IH</sub>	$V_{IN}$ = 2.7V to 6V	1.5			V
RUN Logic Low Threshold	V <sub>IL</sub>	$V_{IN}$ = 2.7V to 6V			0.3	V
RUN Input Bias Current	IEN	VIN = 6V, EN = G or IN	-1.0		1.0	μA
Over-Temperature Shutdown Threshold	TSD			170		°C
Over-Temperature Shutdown Hysteresis	THYS			10		°C



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FUNCTIONAL BLOCK DIAGRAM



### FUNCTIONAL DESCRIPTION

#### CONTROL SCHEME

The LSP3105 utilizes a fixed-frequency, current-mode PWM control scheme combined with fully-integrated power MOSFETs to produce a compact and efficient step-down DC-DC solution. During normal operation the high-side MOSFET turns on each cycle and remains on until the current comparator turns it off. At this point the low-side MOSFET turns on and remains on until either the end of the switching cycle or until the inductor current approaches zero. The error amplifier adjusts the current comparator's threshold as necessary in order to ensure that the output voltage remains in regulation.

#### DROPOUT OPERATION

When the input voltage decreases toward the value of the output voltage, the LSP3105 allows the main switch to remain on for more than one switching cycle and increases the duty cycle until it reaches 100%. The duty cycle D of a step-down converter is defined as:

$$D=T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where  $T_{ON}$  is the main switch on time and  $f_{OSC}$  is the oscillator frequency (1.5MHz).

The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor. At low input supply voltage, the  $R_{DS(ON)}$  of the P-Channel MOSFET increase, and the efficiency of the converter decreases. Caution must be exercised to ensure the heat dissipated not to exceed the maximum junction temperature of the IC.

#### MAXIMUM LOAD CURRENT

The LSP3105 will operate with input supply voltages as low as 2.5V, however, the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.



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### APPLICATION INFORMATION

#### INDUCTOR SELECTION

Under normal operation, the inductor maintains continuous current to the output. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. In general, select an inductance value L based on ripple current requirement:

(1)

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}}$$

where  $V_{IN}$  is the input voltage,  $V_{OUT}$  is the output voltage,  $f_{SW}$  is the switching frequency,  $I_{OUTMAX}$  is the maximum output current, and  $K_{RIPPLE}$  is the ripple factor. Typically, choose  $K_{RIPPLE}$  = 35% to correspond to the peak-to-peak ripple current being 35% of the maximum output current.

With this inductor value (Table 1), the peak inductor current is  $I_{OUT} \cdot (1 + K_{RIPPLE} / 2)$ . Make sure that this peak inductor current is less than the 1.2A current limit. Finally, select the inductor core size so that it does not saturate at the current limit value.

Table 1. Typical Inductor Values

V <sub>OUT</sub>	0.6V to 0.9V	0.9V to 1.8V	>1.8V
L	1.5µH	2.2µH	2.7µH

#### INPUT CAPACITOR SELECTION

The input capacitor reduces input voltage ripple to the converter; a  $4.7\mu$ F ceramic capacitor is recommended for most applications. The input capacitor should be placed as close as possible to IN and G, with short, wide traces. **OUTPUT CAPACITOR SELECTION** 

A low ESR output capacitor is required in order to maintain low output voltage ripple. Output ripple voltage is given by:

$$V_{RIPPLE} = I_{OUTMAX} K_{RIPPLE} R_{ESR} + \frac{V_{IN}}{28 \bullet f_{SW}^2 L C_{OUT}}$$
(2)

where  $I_{OUTMAX}$  is the maximum output current,  $K_{RIPPLE}$  is the ripple factor,  $R_{ESR}$  is the ESR of the output capacitor,  $f_{SW}$  is the switching frequency, L is the inductor value, and  $C_{OUT}$  is the output capacitance. In the case of ceramic output capacitors,  $R_{ESR}$  is very small and does not contribute to the ripple. Therefore, a lower capacitance value is acceptable when ceramic capacitors are used. A 10µF ceramic output capacitor is suitable for most applications.

#### **OUTPUT VOLTAGE PROGRAMMING**



#### Figure 3. Output Voltage Programming

Figure 3 shows the feedback network necessary to set the output voltage when the adjustable version is used. Select the proper ratio of the two feedback resistors  $R_{FB1}$  and  $R_{FB2}$  based on the desired output voltage. Typically choose  $R_{FB2} \approx 100 k\Omega$  and determine  $R_{FB1}$  from the output voltage:

$$R_{FB1} = R_{FB2} \left( \frac{V_{OUT}}{0.6V} - 1 \right)$$
(3)

Connect a small capacitor across RFB1 for Feed forward capacitance at the FB pin:

$$C_{\rm ff} = 2E - 5/R_{\rm FB1} \tag{4}$$

where  $R_{FB1} = 600K\Omega$ , use 22pF. When using very low ESR output capacitors, such as ceramic, check for stability while examining load-transient response, and increase the compensation capacitor C1 if needed.



**2A Synchronous TDFN3\*3-10L Step-Down Converter** TYPICAL PERFORMANCE CHARACTERISTICS









TYPICAL PERFORMANCE CHARACTERISTICS









Quiescent Current vs. Temperature

 $(L = 2.2 \mu H, C_{IN} = C_{OUT} = 22 \mu F)$ 





### 2A Synchronous TDFN3\*3-10L Step-Down Converter



#### MARKING INFORMATION



#### **PACKAGE INFORMATION**

