LINEAR SYSTEMS

LSU425
HIGH INPUT IMPEDANCE MONOLITHIC DUAL N-CHANNEL JFET

micross

Linear Systems replaces discontinued Siliconix U425

The LSU425 is a high input impedance Monolithic Dual N-Channel JFET

The LSU425 monolithic dual n-channel JFET is designed to provide very high input impedance for differential amplification and impedance matching. Among its many unique features, this series offers operating gate current specified at -500 fA. The LSU425 is a direct replacement for discontinued Siliconix U425.

The hermetically sealed TO-71 & TO-78 packages are well suited for military applications. The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LSU425 Applications:

- Ultra Low Input Current Differential Amps
- High-Speed Comparators
- Impedance Converters

FEATURES	
HIGH INPUT IMPEDANCE	I_G = 0.25pA MAX
HIGH GAIN	gfs = 120µmho MIN
LOW POWER OPERATION	$V_{GS(OFF)}$ = 2V MAX

ABSOLUTE MAXIMUM RATINGS
@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1		
$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA

Maximum Power Dissipation	
Device Dissipation @ Free Air – Total	400mW @ +125°C

MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$\lvert\Delta V_{GS1-2}/\Delta T\rvert$ max.	DRIFT VS. TEMPERATURE	25	µV/°C	V_{DG}=10V, I_D=30µA T_A=-55°C to +125°C
$\lvert V_{GS1-2}\rvert$ max.	OFFSET VOLTAGE	15	mV	V_{DG}=10V, I_D=30µA

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

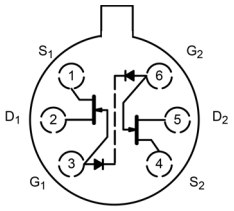
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	40	60	--	V	V_{DS} = 0 I_G =1nA
BV_{GGO}	Gate-To-Gate Breakdown	40	--	--	V	I_G = 1µA I_D = 0 I_S= 0
	TRANSCONDUCTANCE					
Y_{fss}	Full Conduction	300	--	1500	µmho	V_{DS} = 10V V_{GS} = 0V f = 1kHz
Y_{fs}	Typical Operation	120	200	350	µmho	V_{DG} = 10V I_D = 30µA f = 1kHz
	DRAIN CURRENT					
I_{DSS}	Full Conduction	60	--	1000	µA	V_{DS} = 10V V_{GS} = 0V
	GATE VOLTAGE					
$V_{GS(off)}$	Pinchoff voltage	--	--	2.0	V	V_{DS} = 10V I_D = 1nA
V_{GS}	Operating Range	--	--	1.8	V	V_{DG} = 10V I_D = 30µA
	GATE CURRENT					
$I_G$max.	Operating	--	--	.25	pA	V_{DG} = 10V I_D = 30µA
$-I_G$max.	High Temperature	--	--	250	pA	T_A = +125°C
I_{GSS}max.	At Full Conduction	--	--	1.0	pA	V_{DS} = 0V V_{GS} = 20V
$-I_{GSS}$max.	High Temperature	--	--	1.0	nA	T_A = +125°C
	OUTPUT CONDUCTANCE					
Y_{OSS}	Full Conduction	--	--	10	µmho	V_{DS} = 10V V_{GS} = 0V
Y_{OS}	Operating	--	0.1	3.0	µmho	V_{DG} = 10V I_D = 30µA
	COMMON MODE REJECTION					
CMR	-20 log $\lvert\Delta V_{GS1-2}/\Delta V_{DS}\rvert$	--	90	--	dB	ΔV_{DS} = 10 to 20V I_D = 30µA
	-20 log $\lvert\Delta V_{GS1-2}/\Delta V_{DS}\rvert$	--	90	--	dB	ΔV_{DS} = 5 to 10V I_D = 30µA
	NOISE					V_{DG} = 10V I_D = 30µA R_G = 10MΩ
NF	Figure	--	--	1	dB	f = 10Hz
e_n	Voltage	--	20	70	nV/√Hz	V_{DG} = 10V I_D = 30µA f = 10Hz
		--	10	--		V_{DG} = 10V I_D = 30µA f = 1KHz
	CAPACITANCE					
C_{ISS}	Input	--	--	3.0	pF	V_{DS}= 10V V_{GS} = 0 f = 1MHz
C_{RSS}	Reverse Transfer	--	--	1.5	pF	

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LSU425 in TO-71 & TO-78
LSU425 in PDIP & SOIC
LSU425 available as bare die
Please contact Micross for full package and die dimensions
Email: chipcomponents@micross.com

TO-71 / TO-78 (Top View)



P-DIP / SOIC (Top View)