PRODUCT SPECIFICATION

DESCRIPTION

TFT Module – 7.0” WVGA
800 x (RGB) x 480
Full Viewing Angle
High Brightness

PART NUMBER

LT180408-070NT

VERSION

1.1

ROHS COMPLIANT

Revision Status

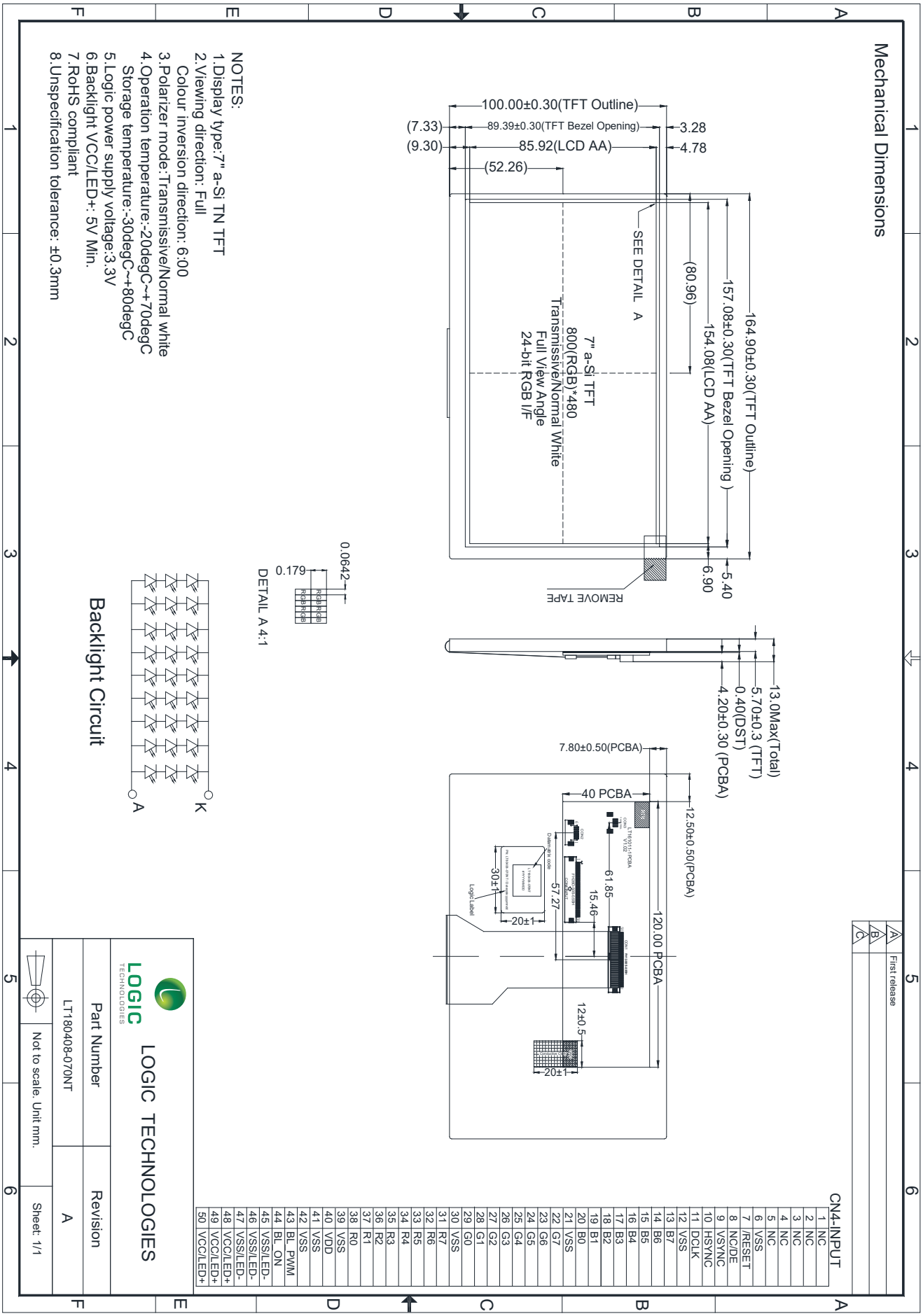
Revision	Revision Date	Page	Content	Notes
1.0	20.11.2018		Initial release	
1.1	04.12.2018		Add mA back on page6	

Table of Contents

- GENERAL INFORMATION

Item	Contents	Unit
LCD Type	TFT Transmissive, anti-glare	---
Technology	a-Si TFT	---
Viewing Direction	Full View	O'clock
Viewing Angle (Colours Inversion Direction)	6:00	O'clock
Module dimensions (W x H x T)	164.9 x 100.0x 12.0	mm
Active area (W x H)	154.08 x 85.92	mm
Number of pixels	800 x 3 (RGB) x 480	---
Pixel pitch (W x H)	0.1926 x 0.179	mm2
Colours	16.7M	---
Contrast ratio	500:1 (typical)	---
Backlight	27LEDs (3 serial LEDs x 9)	---
Backlight Brightness	500	cd/m2
Interface	24-bit RGB	---
Touch Screen	Without Touch	---
Operating temperature	-20 to +70	°C
Storage temperature	-30 to +80	°C

- MECHANICAL DIMENSIONS



- ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Min.	Max.	Unit	Note
Power Voltage	VDD	- 0.5	5.0	V	---
Backlight LED Forward Current	I_F	---	25	mA	One LED
Operating Temperature	T_{OPR}	- 20	70	°C	---
Storage temperature	T_{ST}	- 30	80	°C	---

- ELECTRICAL CHARACTERISTICS (Ta = 25°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Digital Supply Voltage	VDD	3.0	3.3	3.6	V	---
Backlight Supply Voltage	VCC	4.5	5	6	V	
Input Signal Voltage	V_{IL}	0	---	0.3xDVDD	V	R0-R7, G0-G7, B0-B7, DE, DCLK, HSD, VSD, RESET
	V_{IH}	0.7xDVDD	---	DVDD	V	
Current of supply voltage	IVDD		82	120	mA	
	IVCC		456	593	mA	
Power Consumption	Panel and Gamma		271	432	mW	All pixels on and black
	Backlight		2.28	2.96	W	
	Total		2.55	3.36	W	

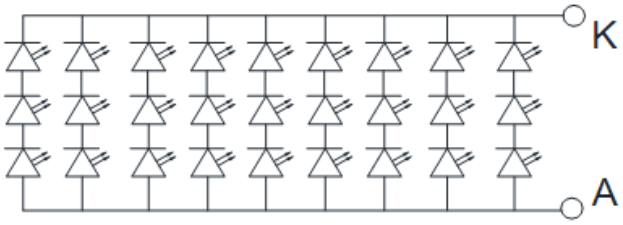
- BACKLIGHT UNIT CHARACTERISTICS

Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Driver Input Voltage	V_{LED}	---	5	6	V	
Current of driver IC	I_{VLED}	---	456	550	mA	
Power Consumption	P_{BL}	---	2.28	2.96	W	Notes
PWM Frequency	PWM	100	150	200	Hz	
Forward Current	IF	---	180	200	mA	Notes
Forward Current Voltage	VF	---	9.9	10.8	V	Notes
LED Lifetime	---	30k	---	---	Hrs	Notes

NOTES:

Backlight drive conditions: constant current driving method.

- The LED driving condition is defined for each LED module (3 LED Serial, 9 LED Parallel).
- The LED driving condition is defined for total backlight consumption.
- Forward Voltage adjustment depends on the Forward Current setting.
- One LED : max IF = 25mA, VF = 3.3V
- The LED lifetime is estimated data at 25degC operating.
- I_F defined for whole backlight without driver.
- If the LEDs are driven by high current, high ambient temperature & humidity condition the lifetime of the LEDs will be reduced.
- Operating life means brightness reduces to 50% of initial brightness.
- Backlight diagram.



- ELECTRO-OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Refer	Note
Response Time		T_{ON}	25°C	---	10	15	Ms	Fig 1	1
		T_{OFF}		---	15	20			
Contrast ratio		Cr	$\theta = 0°$	400	500	---	---	Fig 2	1
Uniformity		U	---	---	75	---	%	Fig 2	3
Surface Luminance		Lv	---	400	500	---	cd/m^2	Fig 2	2
Viewing Angle ratio		θ	$\varnothing = 90°$	60	75	---	---	Fig 3	6
			$\varnothing = 270°$	60	75	---			
			$\varnothing = 0°$	60	75	---			
			$\varnothing = 180°$	60	75	---			
CIE (x,y) chromaticity	Red	x	Backlight On	0.559	0.609	0.659	---	Fig 2.	5
		y		0.305	0.355	0.405			
	Green	x		0.277	0.315	0.364			
		y		0.505	0.555	0.605			
	Blue	x		0.089	0.136	0.189			
		y		0.089	0.139	0.189			
	White	x		0.254	0.304	0.354			
		y		0.294	0.344	0.394			

Optical performance should be evaluated at Ta=25℃.

Note

1. Contrast ratio (CR) is defined mathematically in Figure 2.

Contrast Ratio = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)
Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5…)

Note 3. Uniformity of surface luminance, White, is defined mathematically in figure 2.

White = Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)
Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 4. Response time is the time required for the display to transition form white to black (rise time Tr) and from black to white (decay or fall time, Tf). The industry standard test equipment used is the Autronic-Melcher's Conoscope.

Note 5. CIE (x,y) chromaticity. The x,y value is determined by measuring luminance at each test position 1 through 5, then calculating the average value.

Note 6. The Viewing angle is the angle at which the contrast ratio is greater than 2. For a TFT module, the contrast ratio is greater than 10. The angles are determined for the horizontal or 'x' axis and the vertical or 'y' axis with respect to the 'z' axis, being the LCD surface reference. Also see figure 3.

Note 7. For viewing angle and response time testing, the testing data is based on Autronic-Melcher's BM-7A. For the contrast ratio, surface luminance, luminance uniformity and chromaticity (CIE), the test data is based on the industry's standard SR-3A photo detector.

Note 8. For TFT modules, grey scale reversing occurs in the direction of the panel viewing angle.

Figure 1. Definition of response time

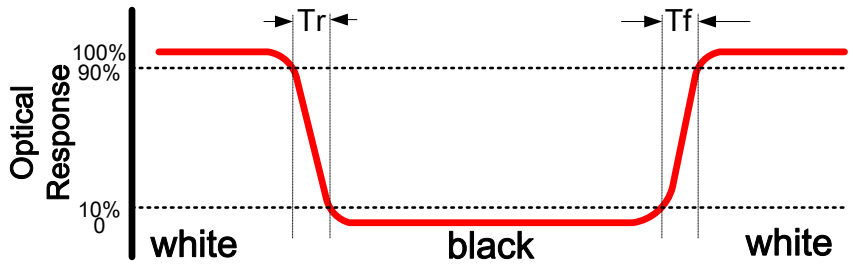


Figure 2. Measuring contrast ratio, surface luminance, luminance uniformity and CIE (chromaticity.)

A : 5mm, B : 5mm, H, V : Active area, Light spot size q = 7mm, 500mm distance from the LCD surface to the detector lens.
Measurement instrument is Topcon's luminance meter BM-5.

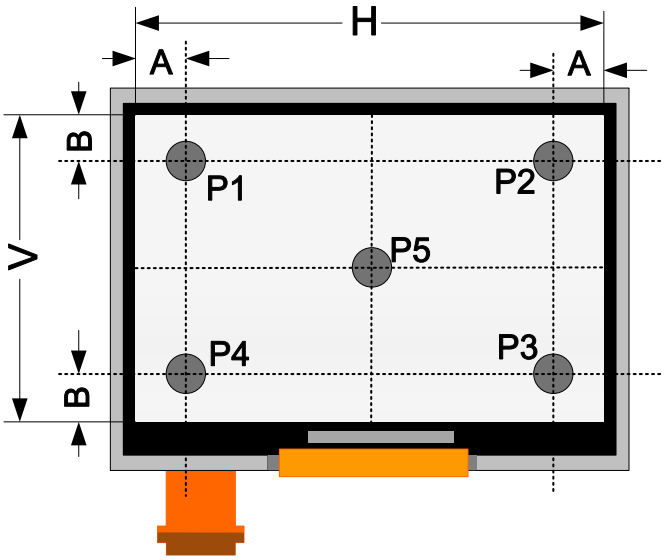
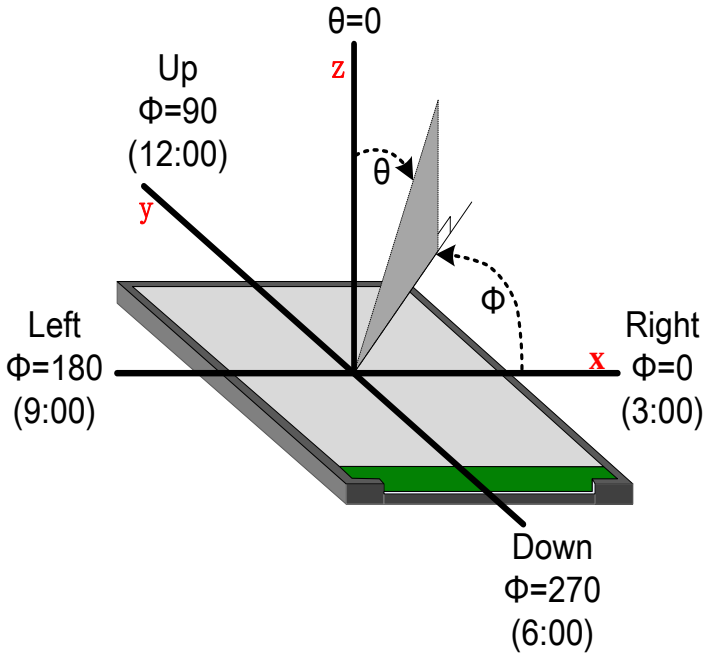


Figure 3. Definition of viewing angle



- INTERFACE DESCRIPTION

Pin	Symbol	I/O	Description	Note
1	T_/INT(YU)	I/O	Cap touch wake up /Interrupt; Resistive touch YU terminal; NC when no touch.	
2	T_NC(XL)	I/O	Resistive touch XU terminal; NC when with cap touch or no touch.	
3	T_/RST(YD)	I/O	Cap touch /Reset pin; Resistive touch YD terminal; NC when no touch.	
4	T_SDA(XR)	I/O	Cap touch I2C data input/output pin; Resistive touch XR terminal; NC when no touch.	
5	T_SCL	I	Cap touch I2C clock input pin; NC when with resistive touch or no touch.	
6	VSS	P	TFT&CTP Ground	
7	/RESET	I	TFT display system reset	
8	NC/DE	I	Data Input Enable when in DE mode. DE/SYNC mode set by R6&R14. R6=10K, R14=NC:DE mode; R6=NC, R14=10K: SYNC mode.	
9	VSYNC	I	Vertical Synch Input	
10	HSYNC	I	Horizontal Synch Signal	
11	DCLK	I	Display Pixel Clock	
12	VSS	I	TFT&CTP Ground	
13	B7	I	Blue data signal (MSB)	
14	B6	I	Blue data signal	
15	B5	I	Blue data signal	
16	B4	I	Blue data signal	
17	B3	I	Blue data signal	
18	B2	I	Blue data signal	
19	B1	I	Blue data signal	
20	B0	I	Blue data signal (LSB)	
21	VSS	P	TFT&CTP Ground	
22	G7	I	Green data signal (MSB)	
23	G6	I	Green data signal	
24	G5	I	Green data signal	
25	G4	I	Green data signal	
26	G3	I	Green data signal	

27	G2	I	Green data signal	
28	G1	I	Green data signal	
29	G0	I	Green data signal (LSB)	
30	VSS	P	TFT&CTP Ground	
31	R7	I	Red data signal (MSB)	
32	R6	I	Red data signal	
33	R5	I	Red data signal	
34	R4	I	Red data signal	
35	R3	I	Red data signal	
36	R2	I	Red data signal	
37	R1	I	Red data signal	
38	R0	I	Red data signal (LSB)	
39	VSS	P	TFT&CTP Ground	
40	VDD	P	TFT&CTP Power supply, 3.3V	
41	VSS	P	TFT&CTP Ground	
42	VSS	P	TFT&CTP Ground	
43	BL_PWM	I	PWM signal to control backlight diming. Valid frequency is 100~200Hz.	
44	BL_ON	I	Backlight on/off control pin. H: On ; L: Off	
45	VSS/LED-	P	Backlight Ground which is LED Cathode. R19=0ohm to connect it to TFT&CTP Ground	
46	VSS/LED-	P		
47	VSS/LED-	P		
48	VCC/LED+	P	Backlight supply voltage input, 5V typical	
49	VCC/LED+	P		
50	VCC/LED+	P		

I -Input only; O -Output only; I/O -Input /output; P -Power or Ground.

Suggested connection for this connector is 0.5pitch 50pins FFC or FPC.

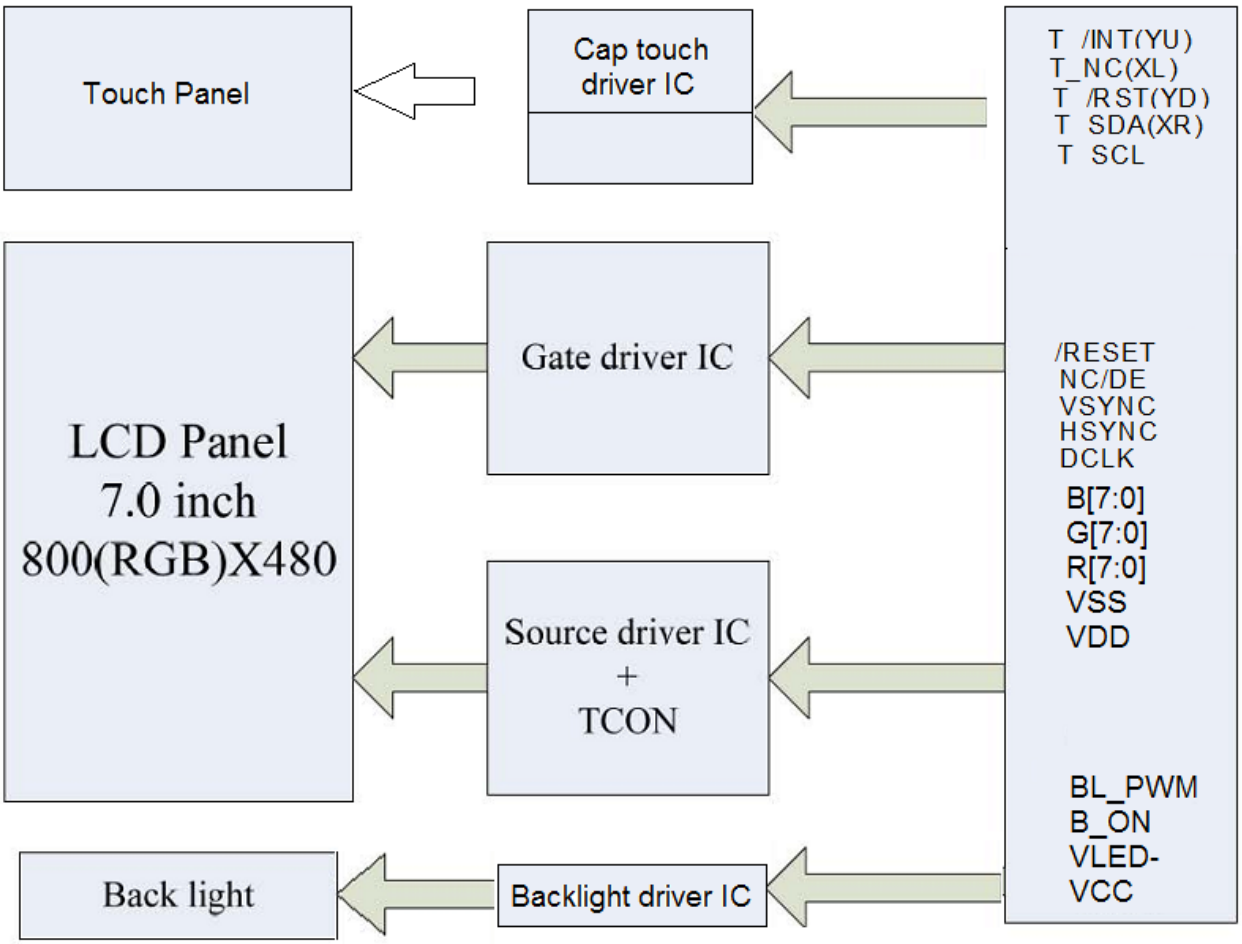
Note 1: Default R6=NC, R14=10K and mode is set to SYNC mode
In SYNC mode, MODE= ”0”, which means DE must be grounded.
When select DE mode, MODE=”1”, VS and HS must be pulled high.
(Above is the suggestion follows IC specification. In our testing, actually no matter DE or SYNC mode, those signals which do not using can be open, connect to VDD or GND and display still works ok.)

Note 2: When input 18 bits RGB data, the two low bits of R,G and B data must be grounded.

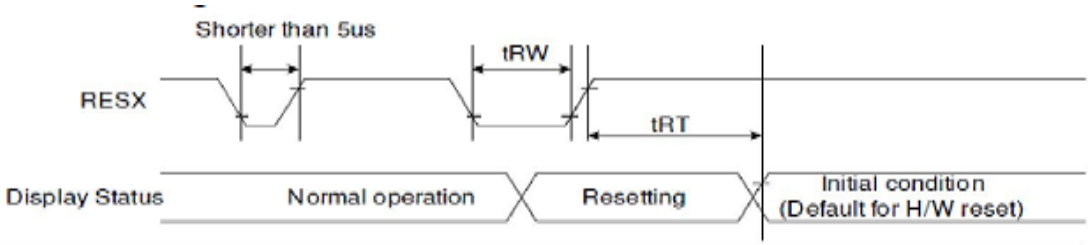
Note 3: Data shall be latched at the falling edge of DCLK.

Note 4: Global reset pin, low active. Suggest it connect with an RC reset circuit for stability. Normally pull high.

Block Diagram

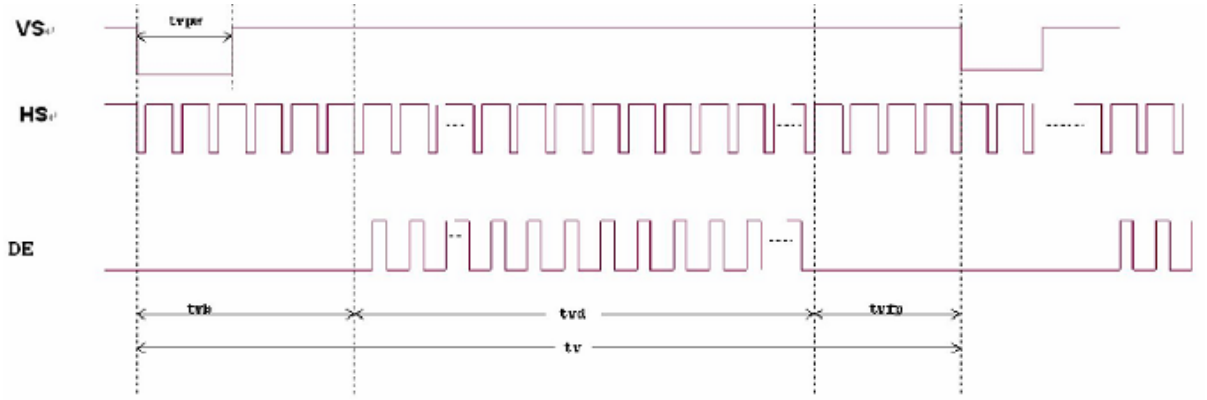


- **RESET TIMING CHARACTERISTICS**



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

- **RGB TIMING CHARACTERISTICS**



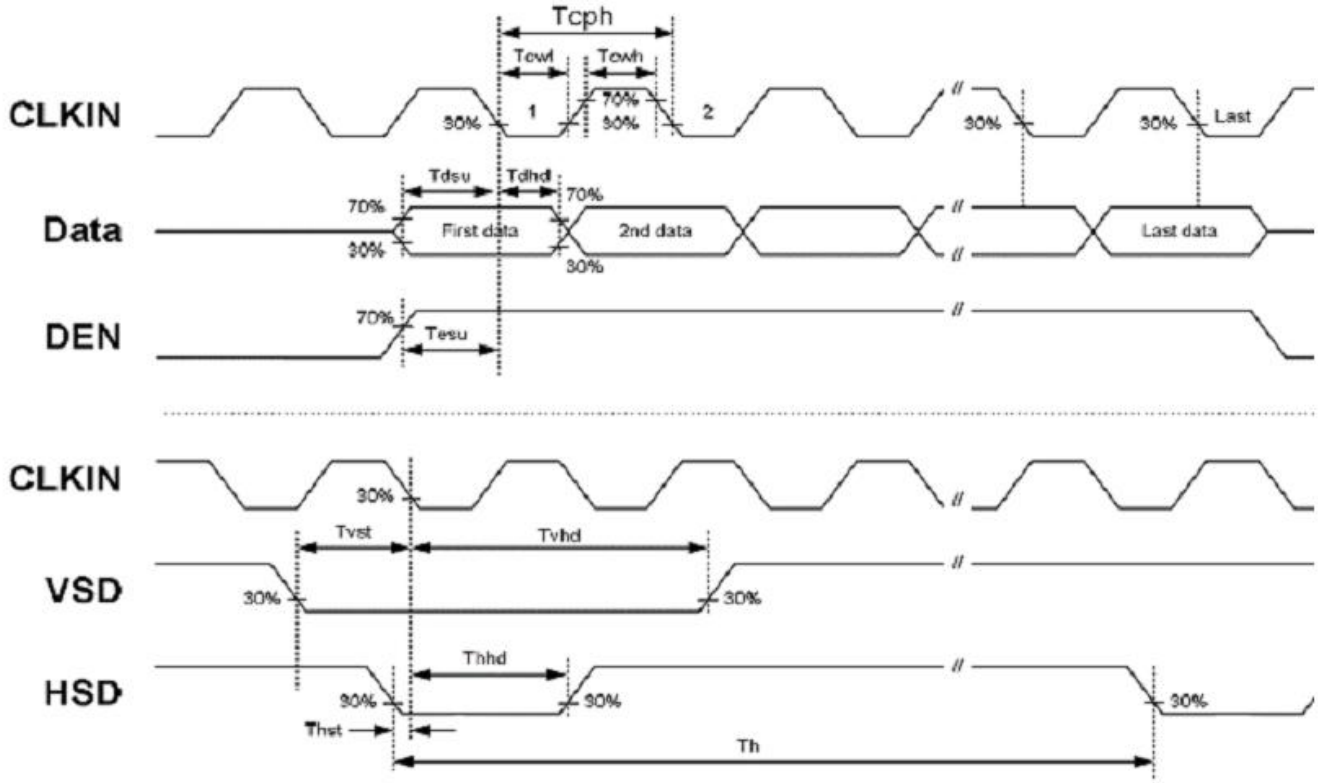
TCON (Embedded In Source IC) Input Timing (DCLK, HS, VS, DE)

VCC=3.3V, GND=0V, Ta=25℃

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DCLK	F_{clk}	26.4	33.3	46.8	MHZ	
	t_{clk}	21.4	30	37.8	ns	
HS	t_h	862	1056	1200	t_{clk}	
	t_{hd}		800		t_{clk}	
	t_{hpw}	1		40	t_{clk}	
	t_{hb}	46	46	46	t_{clk}	
	t_{hfp}	16	210	354	t_{clk}	
VS	t_v	510	525	650	t_h	
	t_{vd}		480		t_h	
	t_{vpw}	1		20	t_h	
	t_{vb}	23	23	23	t_h	
	t_{vfp}	7	22	147	t_h	

Note 1: DE timing refer to HS, VS input timing.

- **AC TIMING CHARACTERISTICS**



Parameter	Symbol	Min	Typ	Max	Unit	Note
DCLK Frequency	Fclk	---	33.3	46.8	MHz	
DCLK Cycle Time	Tcph	20			ns	
DCLK Pulse Width	Tcw	40	50	60	Tcph	
VSD Setup Time	Tvst	8	---	---	ns	
VSD Hold Time	Tvhd	8	---	---	ns	
HSD Setup Time	Thst	8	---	---	ns	
HSD Hold Time	Thhd	8	---	---	ns	
Data Setup Time	Tdsu	8	---	---	ns	Data to DCLK
Data Hold Time	Tdhd	8	---	---	ns	Data to DCLK
DE Setup Time	Tesu	8	---	---	ns	
DE Hold Time	Tehd	8	---	---	ns	