LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT2911R

2-Port LVDS/TTL to MIPI Converter With Frame Rotation

Datasheet

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1. Features

- **Dual-Port LVDS Receiver**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - Up to 1080P 60Hz
  - Data Port ,Data Lane and Polarity Swapping
  - Internal Rterm Calibration with Less than 5% Error
  - Programmable Equalization
  - Support input Dessc(30KHz±5%)
- **MIPI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - Two Port Simultaneous Display Supported
  - Up to 1.8Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **DDR3 Controller**
  - Compliant with DDR3 JESD79-3F
  - BandWidth up to 1866Mbps
  - Support X16 SDRAM Organization
  - Programmable CAS Latency
  - BL8 Supported Only
  - Programmable Output Driver Impedance
  - SR Supported
- **Miscellaneous**
  - 1.5V, 1.8V Power Supply
  - 90/270 Degree Video Rotation
  - External DDR3 SDRAM
  - Support 100KHz and 400KHz I2C Slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40°C ~ +85°C
  - Packaged in QFN128 14mm x 14mm

2. General Description

The Lontium® LT2911R is a high performance Dual-Port LVDS to MIPIDSI/CSI-2 bridge chip with Video Frame Rotation between AP and mobile display panel or camera.

The LT2911R can be configured as single-port or dual-port with optional De-SSC function. The bridge converts formatted video data stream from LVDS source to MIPI DSI/CSI-2 transmitter output with frame rotation 90/270 degree.

For MIPI DSI/CSI-2 output, the LT2911R features a single port MIPI DSI or CSI-2 transmitter with 1 high-speed clock lane and 1~4 configurable high-speed data lanes operating at maximum 1.8Gb/s/lane, which can support a total bandwidth of up to 7.2Gb/s. The LT2911R supports both Non-Burst and Burst DSI/CSI data transferring, as well as Command Mode through Lane-0. And also, the LT2911R can be configured as two port simultaneous display mode.

The LT2911R is fabricated in advanced CMOS process and implemented in 14mm x 14mm QFN128 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

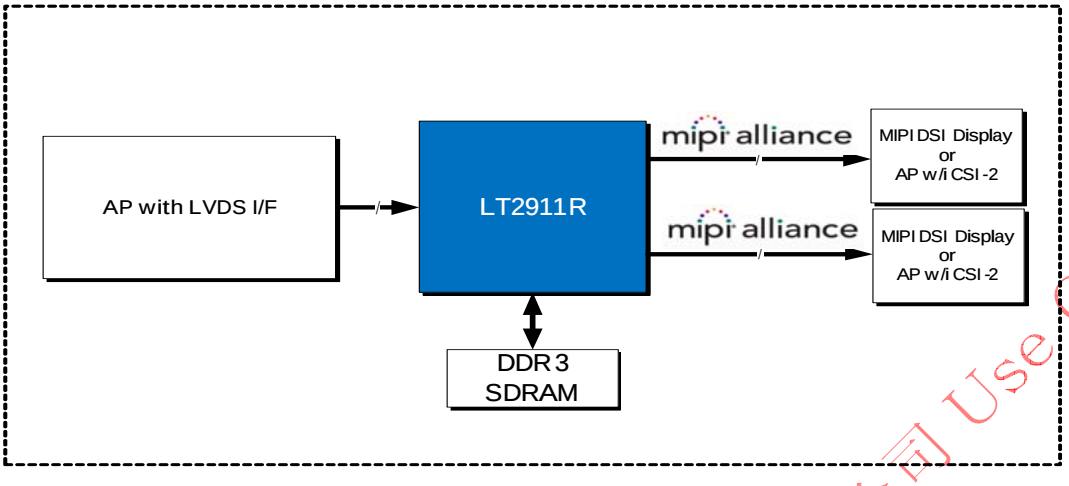

Figure 3.1 LT2911R Typical Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT2911R	-40°C to +85°C	QFN128 (14*14)	

5. IC Version Information

Table 5.1 IC Version Information

Version	Mark
LT2911R	

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6. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	03/30/2018
R2.0	Y C	Add content for MIPI output	07/10/2018

7. Pinning Information

7.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance and all DDR signals should be routed with 40~60Ω impedance. Maximum trace length mismatch should be less than 2.5mil and keep total trace length to a minimum for all differential traces. It is highly recommended to route differential pairs on top or bottom layer with no vias on signal path.

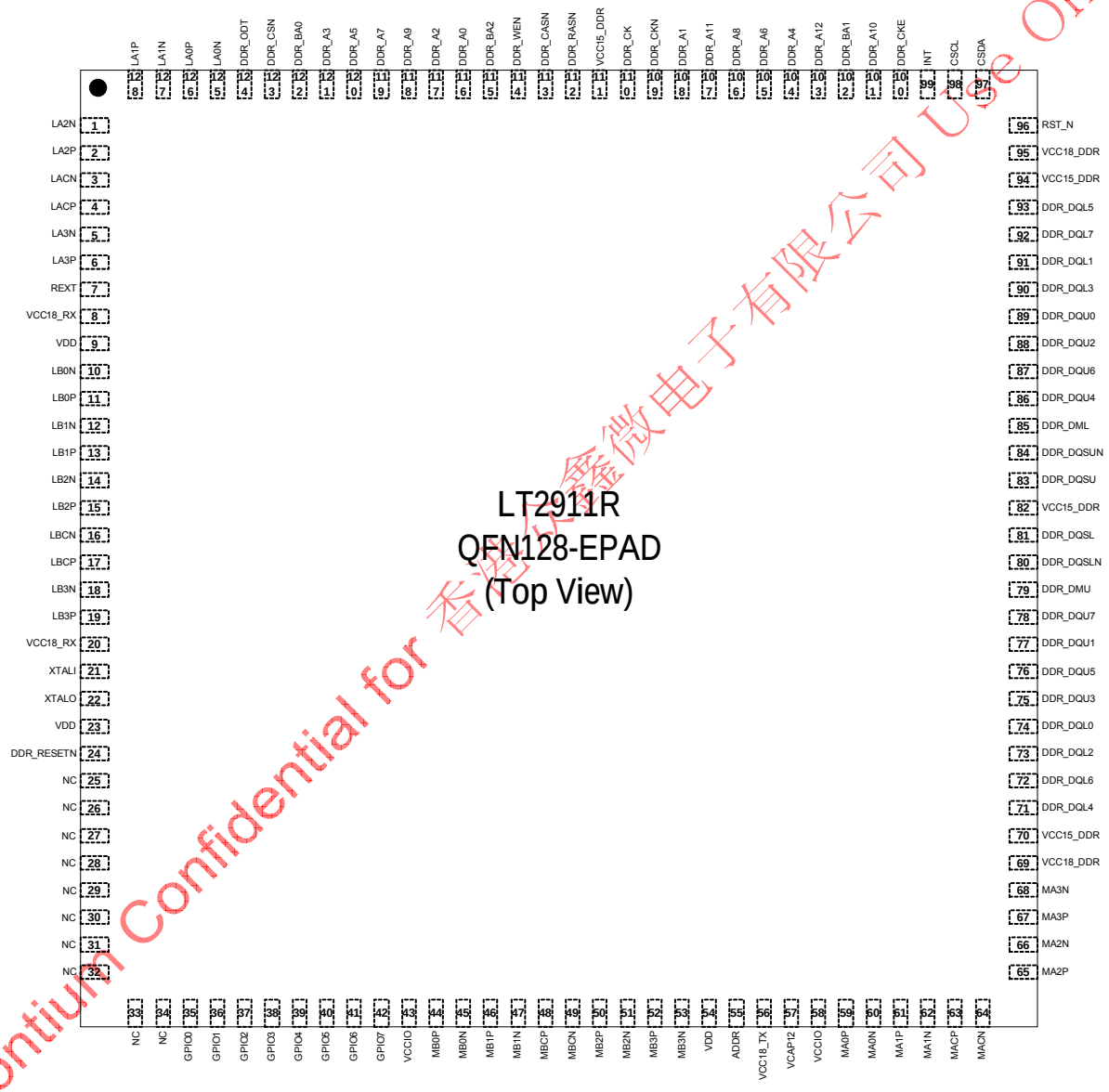


Figure 7.1.1 QFN128 Pin Configuration

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT2911R 1.5V/1.8V/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power input pins must be minimized.

7.2 Pin Description

Table 7.2.1 QFN128 Pin Description

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
125,126	LA0N LA0P	Analog	I	**LVDS Port-A RX Lane-0 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
127,128	LA1N LA1P	Analog	I	**LVDS Port-A RX Lane-1 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
1,2	LA2N LA2P	Analog	I	**LVDS Port-A RX Lane-2 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
3,4	LACN LACP	Analog	I	**LVDS Port-A RX Lane-C Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
5,6	LA3N LA3P	Analog	I	**LVDS Port-A RX Lane-3 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
10,11	LB0N LB0P	Analog	I	**LVDS Port-B RX Lane-0 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
12,13	LB1N LB1P	Analog	I	**LVDS Port-B RX Lane-1 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
14,15	LB2N LB2P	Analog	I	**LVDS Port-B RX Lane-2 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
16,17	LBCN LBCP	Analog	I	**LVDS Port-B RX Lane-C Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
18,19	LB3N LB3P	Analog	I	**LVDS Port-B RX Lane-3 Input** LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
35,36,37,38, 39,40,41,42	GPIO0,GPIO1 GPIO2,GPIO3 GPIO4,GPIO5 GPIO6,GPIO7	Analog	I/O	**Debug GPIO**
59,60	MA0P MA0N	Analog	O/I	**MIPI Port-A TX Lane-0 Output and Input** MIPI output of polarity swappable differential pairs up to 1.8Gb/s .The low power communication is bi-directional.
61,62	MA1P MA1N	Analog	O	**MIPI Port-A TX Lane-1 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
63,64	MACP MACN	Analog	O	**MIPI Port-A TX Lane-C Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
65,66	MA2P MA2N	Analog	O	**MIPI Port-A TX Lane-2 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
67,68	MA3P MA3N	Analog	O	**MIPI Port-A TX Lane-3 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
44,45	MB0P MB0N	Analog	O/I	**MIPI Port-B TX Lane-0 Output and Input** MIPI output of polarity swappable differential pairs up to 1.8Gb/s. The low power communication is bi-directional.
46,47	MB1P MB1N	Analog	O	**MIPI Port-B TX Lane-1 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
48,49	MBCP MBCN	Analog	O	**MIPI Port-B TX Lane-C Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
50,51	MB2P MB2N	Analog	O	**MIPI Port-B TX Lane-2 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
52,53	MB3P MB3N	Analog	O	**MIPI Port-B TX Lane-3 Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
71	DDR_DQL4	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
72	DDR_DQL6	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
73	DDR_DQL2	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
74	DDR_DQL0	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
75	DDR_DQU3	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
76	DDR_DQU5	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
77	DDR_DQU1	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
78	DDR_DQU7	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
79	DDR_DMU	Analog	O	**DDR3 Controller Data Mask Output** Output data is masked when DMU is sampled HIGH coincident with that output data during a Write access.
81,80	DDR_DQSL DDR_DQSLN	Analog	I/O	**DDR3 Controller Input and Output Data Strobe** Bi-directional data strobe differential pairs up to 933Mhz.
83,84	DDR_DQSU DDR_DQSUN	Analog	I/O	**DDR3 Controller Input and Output Data Strobe** Bi-directional data strobe differential pairs up to 933Mhz.
85	DDR_DML	Analog	O	**DDR3 Controller Data Mask Output** Output data is masked when DML is sampled HIGH coincident with that output data during a Write access.
86	DDR_DQU4	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
87	DDR_DQU6	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
88	DDR_DQU2	Analog	I/O	**DDR3 Controller Input and Output Data Strobe** Bi-directional data strobe differential pairs up to 933Mhz.
89	DDR_DQU0	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
90	DDR_DQL3	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
91	DDR_DQL1	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
92	DDR_DQL7	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
93	DDR_DQL5	Analog	I/O	**DDR3 Controller Input and Output Data** Bi-directional data up to 1866Gbps.
110 109	DDR_CK DDR_CKN	Analog	O	**DDR3 Controller CLK Output** Differential clock output up to 933MHz.
112 113 114	DDR_RASN DDR_CASN DDR_WEN	Analog	O	**DDR3 Controller Command Output**
124	DDR_ODT	Analog	O	**DDR3 Controller On Die Termination Control Output** ODT (registered HIGH) enables termination resistance.
123	DDR_CSN	Analog	O	**DDR3 Controller Chip Select Output** All commands are masked when CSN is registered high.
100	DDR_CKE	Analog	O	**DDR3 Controller Clock Enable Output** CKE high activates, and CKE low deactivates.
122 102 115	DDR_BA2 DDR_BA1 DDR_BA0	Analog	O	**DDR3 Controller Bank Address Output**
103 107 101 118 106 119 105 120 104 121 117 108 116	DDR_A12 DDR_A11 DDR_A10 DDR_A9 DDR_A8 DDR_A7 DDR_A6 DDR_A5 DDR_A4 DDR_A3 DDR_A2 DDR_A1 DDR_A0	Analog	O	**DDR3 Controller Address Output**
24	DDR_RESETN	Analog	O	**DDR3 Controller Asynchronous Reset Output** Active low, a 10K resistor pull up to 1.5V is needed with this pin.
7	REXT	Analog	I/O	**BandGap External Resistor** External 6.04K (1%) resistor for setting internal reference current.
21,22	XTALI XTALO	Analog	I/O	**25M Crystal oscillator interface**
55	ADDR	Schmitt	I	**I2C Device Address Select** This pin is configured as I2C address select.
96	RST_N	Schmitt	I	**Hardware Reset Input** Chip reset signal. Active LOW.
97,98	CSDA CSCL	Schmitt OPD	I/O	**I2C Serial Clk and Data Input and Output** It serves as 3.3V/1.8V serial port clk and data IO slave for register access.
99	INT	Schmitt OPD	I/O	**Interrupt Request Output** This pin is interrupt request output. It can be set as Open-drain or CMOS output, when configured as CMOS output,

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
				the output high voltage is 1.8V.
8,20	VCC18_RX	PWR	I/O	**1.8V RX Power** 1.8V power for RX.
56	VCC18_TX	PWR	I/O	**1.8V TX Power** 1.8V power for TX.
43,58	VCCIO	PWR	I/O	**IO Power** 1.8V or 3.3V IO power.
70,82,94,111	VCC15_DDR	PWR	I/O	**1.5V Power for DDR PHY** 1.5V power for DDR PHY.
69,95	VCC18_DDR	PWR	I/O	**1.8V Power for DDR PHY** 1.8V power for DDR PHY.
9,23,54	VDD	PWR	I/O	**1.8V Power** 1.8V power for digital block.
57	VCAP12	PWR	I/O	**Internal 1.2V Power Output** Connect this pin to a bypass capacitor no less than 1uF. When configured as using internal bypass capacitor, please put this pin floating.
25,26,27,28, 29,30,31,32, 33,34	NC	—	—	**No Connection**
129	#EPAD	—	—	**EPAD** Connect to VSS on PCB.

8. Function Description

8.1 Function Block Diagram

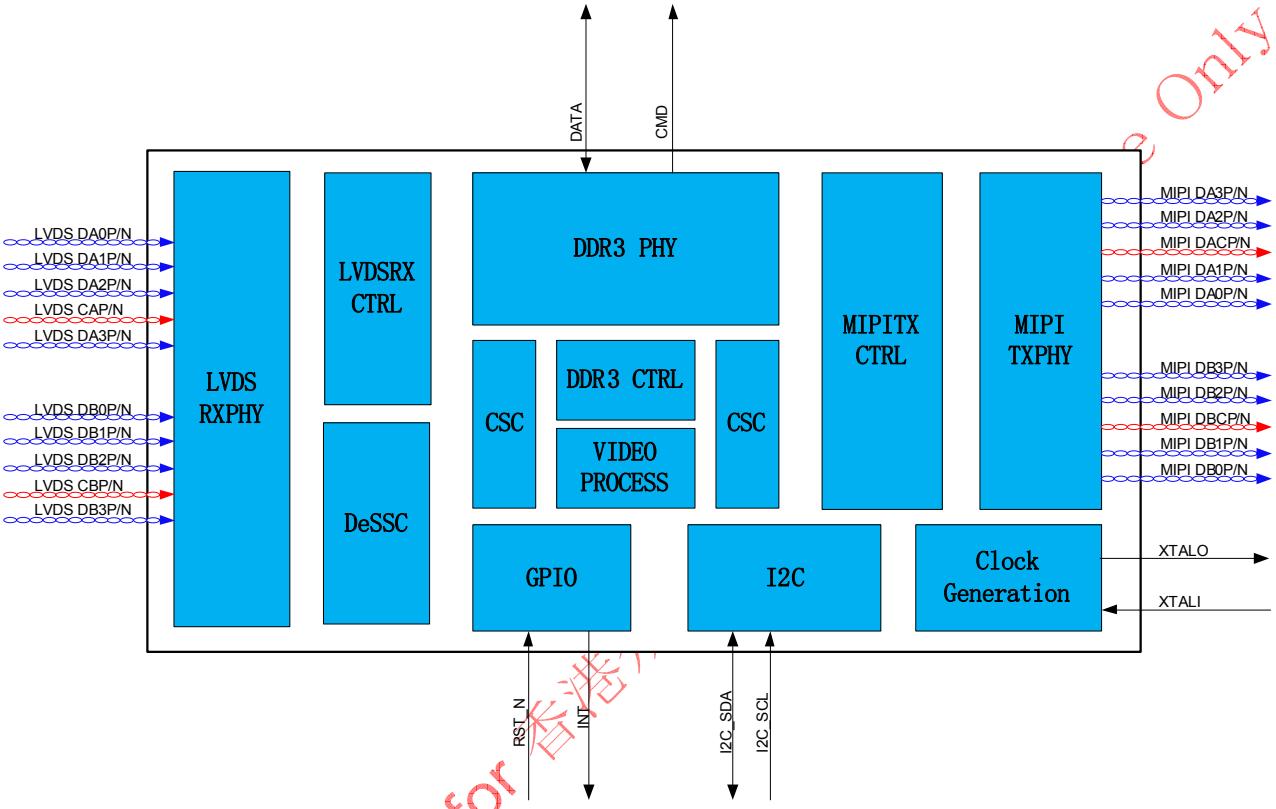


Figure 8.1.1 Function Block Diagram

9. Specification

9.1 Absolute Maximum Conditions

Table 9.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18_DDR,VDD	1.8V Power Supply Voltage	-0.3		2.0	V
VCC15_DDR	1.5V Power Supply Voltage	-0.3		1.6	V
VCCIO	1.8V/3.3V Power Supply Voltage	-0.3		3.63	V
V_I	CMOS Terminal Input Voltage Range	-0.3		2.0	V
V_O	CMOS Terminal Output Voltage Range	-0.3		2.0	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Electrostatic Discharge Level		4K		V

Notes:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

9.2 Normal Operating Conditions

Table 9.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18_DDR,VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCC15_DDR	1.5V Power Supply Voltage	1.425	1.5	1.575	V
VCC33	3.3V Power Supply Voltage	2.97	3.3	3.63	V
	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

9.3 DC Characteristics

Table 9.3.1 DC Characteristics

MIPI HS Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
Vcm	HS Transmit Static Common mode Voltage	150	200	250	mV
Δ Vcm	HS Transmit Static Common mode Voltage Mismatch			5	mV
Vod	HS Transmit Differential Voltage	140	200	270	mV
Δ Vod	HS Transmit Differential Voltage Mismatch			14	mV
Vohhs	HS Transmit Output High Voltage			360	mV
Zos	Single ended output impedance	40	50	62.5	Ω
Δ Zos	Single ended output impedance Mismatch			10	%
MIPI LP Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**

VIL	Input low voltage			550	mV
VIH	Input high voltage，data rate<1.5Gbps	880			mV
	Input high voltage，data rate>1.5Gbps	740			mV
VHYST	Input hysteresis	25			mV
MIPI LP Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOL	Output low-level SE voltage	-50	0	50	mV
VOH	Output high-level SE voltage	1.1	1.2	1.3	V
ZOLP	Single-ended output impedance	110			Ω
ΔZOLP(01,10)	Single-ended output impedance mismatch driving opposite level			20	%
ΔZOLP(00,11)	Single-ended output impedance mismatch driving same level			5	%
LVDS Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			50	mV
VIDTL	Differential input low voltage threshold	-50			mV
VCMRXDC	Input common mode voltage	0	1200	1800	mV
Rterm	Termination Resister	80	100	125	Ω
VIDTH	Differential input high voltage threshold			50	mV
DDR3 Single-Ended DC Specifications for Address and Command output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIH.CA	DC input logic high	vref+0.1		VDD	V
VIL.CA	DC input logic low	VSS		vref-0.1	V
Vref.CA	Reference Voltage for ADD,CMD	0.49*VDD		0.51*VDD	V
Rterm	Termination Resister		50		Ω
DDR3 Single-Ended DC Specifications for DQ output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIH.DQ	DC input logic high	vref+0.1		VDD	V
VIL.DQ	DC input logic low	VSS		vref-0.1	V
Vref.DQ	Reference Voltage for DQ,DM	0.49*VDD		0.51*VDD	V
Ron	Output driver impedance	34			Ω
DDR3 Differential DC Specifications for Clock and Strobe output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIHdiff	Differential input high	0.2			V
VILdiff	Differential input low			-0.2	V
VSEH	Single-ended high level for strobes and clock	vref+0.175			V
VSEL	Single-ended low level for strobes and clock			vref-0.175	V
DDR3 Single-Ended DC Specifications for DQ input					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOH	DC output high measurement level	0.8*VDD			mV
VOM	DC output mid measurement level	0.5*VDD			mV
VOL	DC output low measurement level	0.2*VDD		200	mV
Rodt	On Die termination	20			Ω

9.4 AC Characteristics

Table 9.4.1 AC Characteristics

MIPI HS Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
ΔVcmtx(hf)	Common mode Voltage variation above 450MHz			15	mVrms
ΔVcmtx(lf)	Common mode Voltage variation between 50-450MHz			25	mVpeak
Rise/Fall Time 20%-80%	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
	Data rate >1.5Gbps	50		0.4UI	ps
MIPI LP Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
trlp , tflp	Single ended output rise/fall time,15% to 85%, CL< 70pF			25	ns
treot	Single ended output rise/fall time,30% to 85%, CL< 70pF			35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive-OR clock	20			ns
TLP-PER-TX	Period of the LP exclusive-OR clock	90			ns
δV/δtSR	Slew rate @ CLOAD = 0			500	mV/ns
	Slew rate @ CLOAD = 5pF			350	mV/ns
	Slew rate @ CLOAD = 20pF			250	mV/ns
	Slew rate @ CLOAD = 70pF			150	mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30–0.075*(VO,INST-700)			mV/ns
MIPI LP Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
LVDS Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
CLK	Output clk cycle	6.25	Tc	37	ns
T0	Input data position0	-0.15	0	0.15	ns
T1	Input data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Input data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Input data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Input data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Input data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Input data position6	6Tc/7-0.15		6Tc/7+0.15	ns

DDR3 Single-Ended AC Specifications for Address and Command output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIH.CA	AC input logic high	vref+0.175			V
VIL.CA	AC input logic low			vref-0.175	V
Vref.CA	Reference Voltage for ADD,CMD	0.49*VDD		0.51*VDD	V
Rterm	Termination Resister		50		Ω

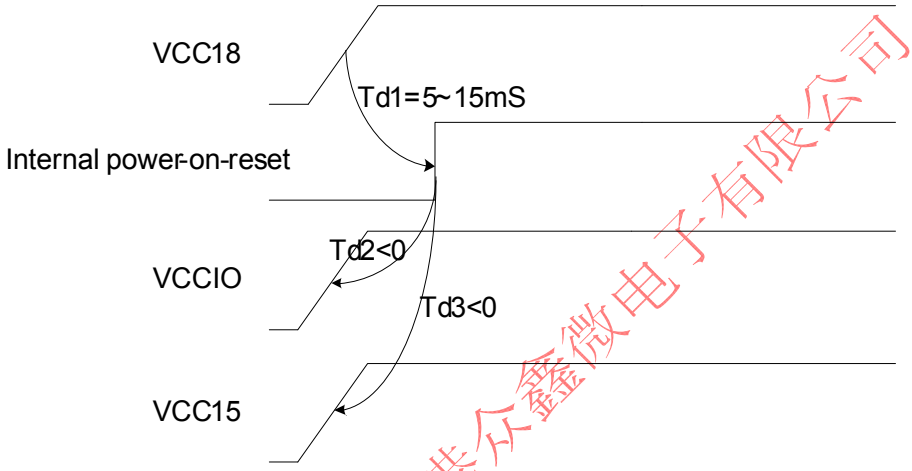
Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Single-Ended AC Specifications for DQ output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIH.DQ	AC input logic high	vref+0.175			V
VIL.DQ	AC input logic low			vref-0.175	V
Rterm	Termination Resister		50		Ω
Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Differential AC Specifications for Clock and Strobe output					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIHdiff	Differential input high	2*(VIH-Vref)			V
VILdiff	Differential input low			2*(VIL+Vref)	V
VIX.CK	Differential Output Cross Point Voltage relative to VDD/2 for CK	-175		175	mV
VIX.DQS	Differential Output Cross Point Voltage relative to VDD/2 for DQS	-150		150	V
Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Single-Ended AC Specifications for DQ input					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOH	AC output high measurement level	VTT+0.1*VDDQ			mV
VOL	AC output low measurement level			VTT-0.1*VDDQ	mV
DDR3 Differential AC Specifications for DQS input					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOHdiff	AC differential output high measurement level	0.2*VDDQ			mV
VOLdiff	AC differential output low measurement level			-0.2*VDDQ	mV

9.5 Power Consumption

Table 9.5.1 Dual-Port LVDS to MIPI Power Consumption

Symbol	Test Condition	Power Consumption	Unit
I_{VCC18}		TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

9.6 Power-up and Reset Sequence



Note：Internal power-on-reset is generated by VCC18, VCCIO and VCC15 should be stable when Internal power-on-reset is high.

Figure 9.6.1 Power-up Sequence

10. Package Information

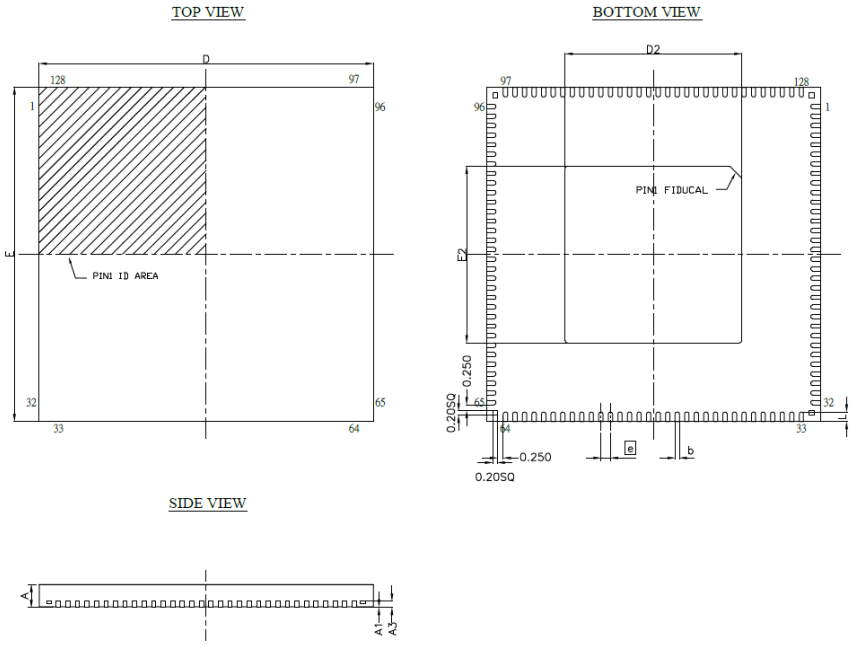
10.1 ePad Enhancement

The LT2911R is packaged in QFN128 package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

10.2 Package Dimensions



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20 REF	
b	0.13	0.18	0.25
D	13.90	14.00	14.10
D2	7.30	7.40	7.50
E	13.90	14.00	14.10
E2	7.30	7.40	7.50
e		0.40 BSC	
L	0.30	0.40	0.50

Figure 10.2.1 QFN128 Package Dimensions

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