



LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT2911R

2-Port LVDS/TTL to MIPI Converter
With Frame Rotation

Datasheet

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1. Features

● Dual-Port LVDS Receiver

- Compatible with VESA and JEIDA standard
- 1~2 Configurable Port
- Up to 1080P 60Hz
- Data Port ,Data Lane and Polarity Swapping
- Internal Rterm Calibration with Less than 5% Error
- Programmable Equalization
- Support input Dssc(30KHz \pm 5%)

● MIPI Transmitter

- Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
- 1 Clock Lane and 1~4 Configurable Data Lanes
- Two Port Simultaneous Display Supported
- Up to 1.8Gb/s per Data Lane
- Resolution Up to 1080P 60Hz
- Data Lane and Polarity Swapping
- Both Non-Burst and Burst Video Mode Supported
- Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format

● DDR3 Controller

- Compliant with DDR3 JESD79-3F
- BandWidth up to 1866Mbps
- Support X16 SDRAM Organization
- Programmable CAS Latency
- BL8 Supported Only
- Programmable Output Driver Impedance
- SR Supported

● Miscellaneous

- 1.5V, 1.8V Power Supply
- 90/270 Degree Video Rotation
- External DDR3 SDRAM
- Support 100KHz and 400KHz I2C Slave

- External 25MHz Crystal Reference Clock
- Temperature Range: -40°C ~ +85°C
- Packaged in QFN128 14mm x 14mm

2. General Description

The Lontium® LT2911R is a high performance Dual-Port LVDS to MIPIDSI/CSI-2 bridge chip with Video Frame Rotation between AP and mobile display panel or camera.

The LT2911R can be configured as single-port or dual-port with optional De-SSC function. The bridge converts formatted video data stream from LVDS source to MIPI DSI/CSI-2 transmitter output with frame rotation 90/270 degree.

For MIPI DSI/CSI-2 output, the LT2911R features a single port MIPI DSI or CSI-2 transmitter with 1 high-speed clock lane and 1~4 configurable high-speed data lanes operating at maximum 1.8Gb/s/lane, which can support a total bandwidth of up to 7.2Gb/s. The LT2911R supports both Non-Burst and Burst DSI/CSI data transferring, as well as Command Mode through Lane-0. And also, the LT2911R can be configured as two port simultaneous display mode.

The LT2911R is fabricated in advanced CMOS process and implemented in 14mm x 14mm QFN128 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

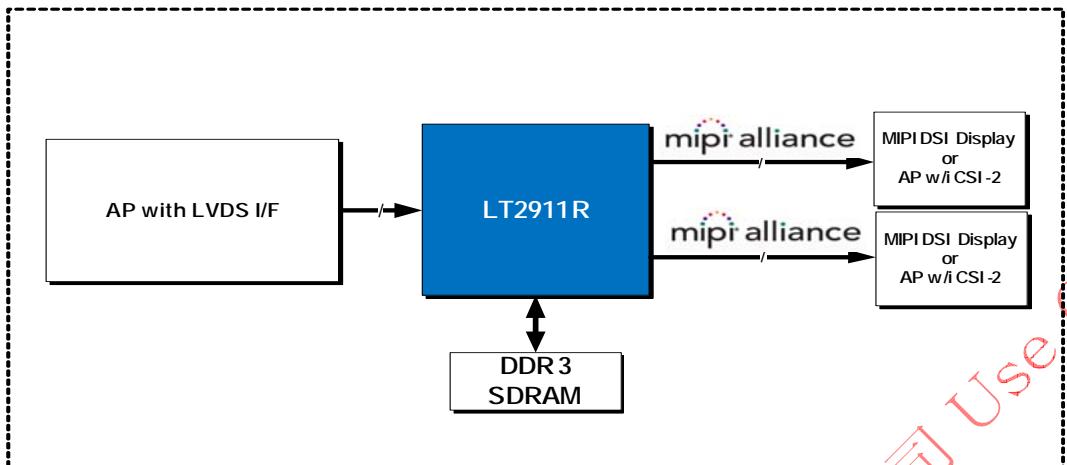


Figure 3.1 LT2911R Typical Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT2911R	-40°C to +85°C	QFN128 (14*14)	

5. IC Version Information

Table 5.1 IC Version Information

Version	Mark
LT2911R	



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6. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	03/30/2018
R2.0	Y C	Add content for MIPI output	07/10/2018

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7. Pinning Information

7.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with $100\Omega \pm 10\%$ differential impedance and all DDR signals should be routed with $40\sim 60\Omega$ impedance. Maximum trace length mismatch should be less than 2.5mil and keep total trace length to a minimum for all differential traces. It is highly recommended to route differential pairs on top or bottom layer with no vias on signal path.

●	12	LA1P	13	LA1N	14	LA0P	15	LA0N	16	DRB_ODT	17	DRB_CS_N	18	DRB_BA0	19	DDR_A3	20	DDR_A5	21	DDR_A7	22	DDR_A9	23	DDR_A10	24	DDR_A2	25	DDR_A40	26	DDR_BA2	27	DDR_WEN	28	DDR_CASN	29	DDR_RASN	30	VCC15_DDR	31	DDR_CK	32	DDR_CKN	33	DDR_A1	34	DDR_A11	35	DDR_A46	36	DDR_A46	37	DDR_A4	38	DDR_A12	39	DDR_BA1	40	DDR_A10	41	DDR_CKE	42	INT	43	CSDL	44	CSDA	45	36	RST_N	37	VCC18_DDR	38	VCC15_DDR	39	DDR_DQL5	40	DDR_DQL7	41	DDR_DQL1	42	DDR_DQL3	43	DDR_DQ0	44	DDR_DQ2	45	DDR_DQ6	46	DDR_DQ4	47	DDR_DML	48	DDR_DQSUN	49	DDR_DQSU	50	VCC15_DDR	51	DDR_DQL	52	DDR_DQL1	53	DDR_DQL3	54	DDR_DQ0	55	DDR_DQ2	56	DDR_DQ6	57	DDR_DQ4	58	DDR_DML	59	DDR_DQSUN	60	DDR_DQSU	61	VCC18_DDR	62	DDR_DQL	63	DDR_DQL1	64	DDR_DQL3	65	DDR_DQ0	66	DDR_DQ2	67	DDR_DQ6	68	DDR_DQ4	69	DDR_DML	70	DDR_DQSUN	71	DDR_DQSU	72	VCC15_DDR	73	DDR_DQL2	74	DDR_DQL0	75	DDR_DQL2	76	DDR_DQL6	77	DDR_DQL4	78	VCC15_DDR	79	DDR_DMU	80	DDR_DQ7	81	DDR_DQ1	82	DDR_DQ5	83	DDR_DQ3	84	DDR_DQ1	85	DDR_DQ5	86	DDR_DQ3	87	DDR_DQ7	88	DDR_DQ1	89	DDR_DQ5	90	DDR_DQ3	91	DDR_DQ7	92	DDR_DQ1	93	DDR_DQ5	94	DDR_DQ3	95	DDR_DQ7	96	DDR_DQ1	97	DDR_DQ5	98	DDR_DQ3	99	DDR_DQ7	100	DDR_DQ1	101	DDR_DQ5	102	DDR_DQ3	103	DDR_DQ7	104	DDR_DQ1	105	DDR_DQ5	106	DDR_DQ3	107	DDR_DQ7	108	DDR_DQ1	109	DDR_DQ5	110	DDR_DQ3	111	DDR_DQ7	112	DDR_DQ1	113	DDR_DQ5	114	DDR_DQ3	115	DDR_DQ7	116	DDR_DQ1	117	DDR_DQ5	118	DDR_DQ3	119	DDR_DQ7	120	DDR_DQ1	121	DDR_DQ5	122	DDR_DQ3	123	DDR_DQ7	124	DDR_DQ1	125	DDR_DQ5	126	DDR_DQ3	127	DDR_DQ7	128	DDR_DQ1	129	DDR_DQ5	130	DDR_DQ3	131	DDR_DQ7	132	DDR_DQ1	133	DDR_DQ5	134	DDR_DQ3	135	DDR_DQ7	136	DDR_DQ1	137	DDR_DQ5	138	DDR_DQ3	139	DDR_DQ7	140	DDR_DQ1	141	DDR_DQ5	142	DDR_DQ3	143	DDR_DQ7	144	DDR_DQ1	145	DDR_DQ5	146	DDR_DQ3	147	DDR_DQ7	148	DDR_DQ1	149	DDR_DQ5	150	DDR_DQ3	151	DDR_DQ7	152	DDR_DQ1	153	DDR_DQ5	154	DDR_DQ3	155	DDR_DQ7	156	DDR_DQ1	157	DDR_DQ5	158	DDR_DQ3	159	DDR_DQ7	160	DDR_DQ1	161	DDR_DQ5	162	DDR_DQ3	163	DDR_DQ7	164	DDR_DQ1	165	DDR_DQ5	166	DDR_DQ3	167	DDR_DQ7	168	DDR_DQ1	169	DDR_DQ5	170	DDR_DQ3	171	DDR_DQ7	172	DDR_DQ1	173	DDR_DQ5	174	DDR_DQ3	175	DDR_DQ7	176	DDR_DQ1	177	DDR_DQ5	178	DDR_DQ3	179	DDR_DQ7	180	DDR_DQ1	181	DDR_DQ5	182	DDR_DQ3	183	DDR_DQ7	184	DDR_DQ1	185	DDR_DQ5	186	DDR_DQ3	187	DDR_DQ7	188	DDR_DQ1	189	DDR_DQ5	190	DDR_DQ3	191	DDR_DQ7	192	DDR_DQ1	193	DDR_DQ5	194	DDR_DQ3	195	DDR_DQ7	196	DDR_DQ1	197	DDR_DQ5	198	DDR_DQ3	199	DDR_DQ7	200	DDR_DQ1	201	DDR_DQ5	202	DDR_DQ3	203	DDR_DQ7	204	DDR_DQ1	205	DDR_DQ5	206	DDR_DQ3	207	DDR_DQ7	208	DDR_DQ1	209	DDR_DQ5	210	DDR_DQ3	211	DDR_DQ7	212	DDR_DQ1	213	DDR_DQ5	214	DDR_DQ3	215	DDR_DQ7	216	DDR_DQ1	217	DDR_DQ5	218	DDR_DQ3	219	DDR_DQ7	220	DDR_DQ1	221	DDR_DQ5	222	DDR_DQ3	223	DDR_DQ7	224	DDR_RESETN	225	NC	226	NC	227	NC	228	NC	229	NC	230	NC	231	NC	232	NC	233	NC	234	NC	235	GPIO0	236	GPIO1	237	GPIO2	238	GPIO3	239	GPIO4	240	GPIO5	241	GPIO6	242	GPIO7	243	VCCIO	244	M80P	245	M80N	246	M81P	247	M81N	248	M82P	249	M82N	250	M83P	251	M83N	252	M84P	253	M84N	254	M85P	255	M85N	256	M86P	257	M86N	258	M87P	259	M87N	260	M88P	261	M88N	262	M89P	263	M89N	264	M90P	265	M90N	266	M91P	267	M91N	268	M92P	269	M92N	270	M93P	271	M93N	272	M94P	273	M94N	274	M95P	275	M95N	276	M96P	277	M96N	278	M97P	279	M97N	280	M98P	281	M98N	282	M99P	283	M99N	284	M100P	285	M100N	286	M101P	287	M101N	288	M102P	289	M102N	290	M103P	291	M103N	292	M104P	293	M104N	294	M105P	295	M105N	296	M106P	297	M106N	298	M107P	299	M107N	300	M108P	301	M108N	302	M109P	303	M109N	304	M110P	305	M110N	306	M111P	307	M111N	308	M112P	309	M112N	310	M113P	311	M113N	312	M114P	313	M114N	314	M115P	315	M115N	316	M116P	317	M116N	318	M117P	319	M117N	320	M118P	321	M118N	322	M119P	323	M119N	324	M120P	325	M120N	326	M121P	327	M121N	328	M122P	329	M122N	330	M123P	331	M123N	332	M124P	333	M124N	334	M125P	335	M125N	336	M126P	337	M126N	338	M127P	339	M127N	340	M128P	341	M128N	342	M129P	343	M129N	344	M130P	345	M130N	346	M131P	347	M131N	348	M132P	349	M132N	350	M133P	351	M133N	352	M134P	353	M134N	354	M135P	355	M135N	356	M136P	357	M136N	358	M137P	359	M137N	360	M138P	361	M138N	362	M139P	363	M139N	364	M140P	365	M140N	366	M141P	367	M141N	368	M142P	369	M142N	370	M143P	371	M143N	372	M144P	373	M144N	374	M145P	375	M145N	376	M146P	377	M146N	378	M147P	379	M147N	380	M148P	381	M148N	382	M149P	383	M149N	384	M150P	385	M150N	386	M151P	387	M151N	388	M152P	389	M152N	390	M153P	391	M153N	392	M154P	393	M154N	394	M155P	395	M155N	396	M156P	397	M156N	398	M157P	399	M157N	400	M158P	401	M158N	402	M159P	403	M159N	404	M160P	405	M160N	406	M161P	407	M161N	408	M162P	409	M162N	410	M163P	411	M163N	412	M164P	413	M164N	414	M165P	415	M165N	416	M166P	417	M166N	418	M167P	419	M167N	420	M168P	421	M168N	422	M169P	423	M169N	424	M170P	425	M170N	426	M171P	427	M171N	428	M172P	429	M172N	430	M173P	431	M173N	432	M174P	433	M174N	434	M175P	435	M175N	436	M176P	437	M176N	438	M177P	439	M177N	440	M178P	441	M178N	442	M179P	443	M179N	444	M180P	445	M180N	446	M181P	447	M181N	448	M182P	449	M182N	450	M183P	451	M183N	452	M184P	453	M184N	454	M185P	455	M185N	456	M186P	457	M186N	458	M187P	459	M187N	460	M188P	461	M188N	462	M189P	463	M189N	464	M190P	465	M190N	466	M191P	467	M191N	468	M192P	469	M192N	470	M193P	471	M193N	472	M194P	473	M194N	474	M195P	475	M195N	476	M196P	477	M196N	478	M197P	479	M197N	480	M198P	481	M198N	482	M199P	483	M199N	484	M200P	485	M200N	486	M201P	487	M201N	488	M202P	489	M202N	490	M203P	491	M203N	492	M204P	493	M204N	494	M205P	495	M205N	496	M206P	497	M206N	498	M207P	499	M207N	500	M208P	501	M208N	502	M209P	503	M209N	504	M210P	505	M210N	506	M211P	507	M211N	508	M212P	509	M212N	510	M213P	511	M213N	512	M214P	513	M214N	514	M215P	515	M215N	516	M216P	517	M216N	518	M217P	519	M217N	520	M218P	521	M218N	522	M219P	523	M219N	524	M220P	525	M220N	526	M221P	527	M221N	528	M222P	529	M222N	530	M223P	531	M223N	532	M224P	533	M224N	534	M225P	535	M225N	536	M226P	537	M226N	538	M227P	539	M227N	540	M228P	541	M228N	542	M229P	543	M229N	544	M230P	545	M230N	546	M231P	547	M231N	548	M232P	549	M232N	550	M233P	551	M233N	552	M234P	553	M234N	554	M235P	555	M235N	556	M236P	557	M236N	558	M237P	559	M237N	560	M238P	561	M238N	562	M239P	563	M239N	564	M240P	565	M240N	566	M241P	567	M241N	568	M242P	569	M242N	570	M243P	571	M243N	572	M244P	573	M244N	574	M245P	575	M245N	576	M246P	577	M246N	578	M247P	579	M247N	580	M248P	581	M248N	582	M249P	583	M249N	584	M250P	585	M250N	586	M251P	587	M251N	588	M252P	589	M252N	590	M253P	591	M253N	592	M254P	593	M254N	594	M255P	595	M255N	596	M256P	597	M256N	598	M257P	599	M257N	600	M258P	601	M258N	602	M259P	603	M259N	604	M260P	605	M260N	606	M261P	607	M261N	608	M262P	609	M262N	610	M263P	611	M263N	612	M264P	613	M264N	614	M265P	615	M265N	616	M266P	617	M266N	618	M267P	619	M267N	620	M268P	621	M268N	622	M269P	623	M269N	624	M270P	625	M270N	626	M271P	627	M271N	628	M272P	629	M272N	630	M273P	631	M273N	632	M274P	633	M274N	634	M275P	635	M275N	636	M276P	637	M276N	638	M277P	639	M277N	640	M278P	641	M278N	642	M279P	643	M279N	644	M280P	645	M280N	646	M281P	647	M281N	648	M282P	649	M282N	650	M283P	651



7.2 Pin Description

Table 7.2.1 QFN128 Pin Description

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
125,126	LA0N LA0P	Analog	I	LVDS Port-A RX Lane-0 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
127,128	LA1N LA1P	Analog	I	LVDS Port-A RX Lane-1 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
1,2	LA2N LA2P	Analog	I	LVDS Port-A RX Lane-2 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
3,4	LACN LACP	Analog	I	LVDS Port-A RX Lane-C Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
5,6	LA3N LA3P	Analog	I	LVDS Port-A RX Lane-3 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
10,11	LB0N LB0P	Analog	I	LVDS Port-B RX Lane-0 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
12,13	LB1N LB1P	Analog	I	LVDS Port-B RX Lane-1 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
14,15	LB2N LB2P	Analog	I	LVDS Port-B RX Lane-2 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
16,17	LBCN LBCP	Analog	I	LVDS Port-B RX Lane-C Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
18,19	LB3N LB3P	Analog	I	LVDS Port-B RX Lane-3 Input LVDS input of polarity swappable differential pairs up to 1.2Gb/s.
35,36,37,38, 39,40,41,42	GPIO0,GPIO1 GPIO2,GPIO3 GPIO4,GPIO5 GPIO6,GPIO7	Analog	I/O	Debug GPIO
59,60	MA0P MA0N	Analog	O/I	MIPI Port-A TX Lane-0 Output and Input MIPI output of polarity swappable differential pairs up to 1.8Gb/s. The low power communication is bi-directional.
61,62	MA1P MA1N	Analog	O	MIPI Port-A TX Lane-1 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
63,64	MACP MACN	Analog	O	MIPI Port-A TX Lane-C Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
65,66	MA2P MA2N	Analog	O	MIPI Port-A TX Lane-2 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.

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PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
67,68	MA3P MA3N	Analog	O	MIPI Port-A TX Lane-3 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
44,45	MB0P MB0N	Analog	O/I	MIPI Port-B TX Lane-0 Output and Input MIPI output of polarity swappable differential pairs up to 1.8Gb/s. The low power communication is bi-directional.
46,47	MB1P MB1N	Analog	O	MIPI Port-B TX Lane-1 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
48,49	MBCP MBCN	Analog	O	MIPI Port-B TX Lane-C Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
50,51	MB2P MB2N	Analog	O	MIPI Port-B TX Lane-2 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
52,53	MB3P MB3N	Analog	O	MIPI Port-B TX Lane-3 Output MIPI output of polarity swappable differential pairs up to 1.8Gb/s.
71	DDR_DQL4	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
72	DDR_DQL6	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
73	DDR_DQL2	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
74	DDR_DQL0	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
75	DDR_DQU3	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
76	DDR_DQU5	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
77	DDR_DQU1	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
78	DDR_DQU7	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
79	DDR_DMU	Analog	O	DDR3 Controller Data Mask Output Output data is masked when DMU is sampled HIGH coincident with that output data during a Write access.
81,80	DDR_DQSL DDR_DQLN	Analog	I/O	DDR3 Controller Input and Output Data Strobe Bi-directional data strobe differential pairs up to 933Mhz.
83,84	DDR_DQSU DDR_DQSN	Analog	I/O	DDR3 Controller Input and Output Data Strobe Bi-directional data strobe differential pairs up to 933Mhz.
85	DDR_DML	Analog	O	DDR3 Controller Data Mask Output Output data is masked when DML is sampled HIGH coincident with that output data during a Write access.
86	DDR_DQU4	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
87	DDR_DQU6	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
88	DDR_DQU2	Analog	I/O	DDR3 Controller Input and Output Data Strobe Bi-directional data strobe differential pairs up to 933Mhz.
89	DDR_DQU0	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.

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PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
90	DDR_DQL3	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
91	DDR_DQL1	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
92	DDR_DQL7	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
93	DDR_DQL5	Analog	I/O	DDR3 Controller Input and Output Data Bi-directional data up to 1866Gbps.
110 109	DDR_CK DDR_CKN	Analog	O	DDR3 Controller CLK Output Differential clock output up to 933MHz.
112 113 114	DDR_RASN DDR_CASN DDR_WEN	Analog	O	DDR3 Controller Command Output
124	DDR_ODT	Analog	O	DDR3 Controller On Die Termination Control Output ODT (registered HIGH) enables termination resistance.
123	DDR_CSN	Analog	O	DDR3 Controller Chip Select Output All commands are masked when CSN is registered high.
100	DDR_CKE	Analog	O	DDR3 Controller Clock Enable Output CKE high activates, and CKE low deactivates.
122 102 115	DDR_BA2 DDR_BA1 DDR_BA0	Analog	O	DDR3 Controller Bank Address Output
103 107 101 118 106 119 105 120 104 121 117 108 116	DDR_A12 DDR_A11 DDR_A10 DDR_A9 DDR_A8 DDR_A7 DDR_A6 DDR_A5 DDR_A4 DDR_A3 DDR_A2 DDR_A1 DDR_A0	Analog	O	DDR3 Controller Address Output
24	DDR_RESETN	Analog	O	DDR3 Controller Asynchronous Reset Output Active low, a 10K resistor pull up to 1.5V is needed with this pin.
7	REXT	Analog	I/O	BandGap External Resistor External 6.04K (1%) resistor for setting internal reference current.
21,22	XTALI XTALO	Analog	I/O	25M Crystal oscillator interface
55	ADDR	Schmitt	I	I2C Device Address Select This pin is configured as I2C address select.
96	RST_N	Schmitt	I	Hardware Reset Input Chip reset signal. Active LOW.
97,98	CSDA CSCL	Schmitt OPD	I/O	I2C Serial Clk and Data Input and Output It serves as 3.3V/1.8V serial port clk and data IO slave for register access.
99	INT	Schmitt OPD	I/O	Interrupt Request Output This pin is interrupt request output. It can be set as Open-drain or CMOS output, when configured as CMOS output.

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PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
				the output high voltage is 1.8V.
8,20	VCC18_RX	PWR	I/O	1.8V RX Power 1.8V power for RX.
56	VCC18_TX	PWR	I/O	1.8V TX Power 1.8V power for TX.
43,58	VCCIO	PWR	I/O	IO Power 1.8V or 3.3V IO power.
70,82,94,111	VCC15_DDR	PWR	I/O	1.5V Power for DDR PHY 1.5V power for DDR PHY.
69,95	VCC18_DDR	PWR	I/O	1.8V Power for DDR PHY 1.8V power for DDR PHY.
9,23,54	VDD	PWR	I/O	1.8V Power 1.8V power for digital block.
57	VCAP12	PWR	I/O	Internal 1.2V Power Output Connect this pin to a bypass capacitor no less than 1uF. When configured as using internal bypass capacitor, please put this pin floating.
25,26,27,28, 29,30,31,32, 33,34	NC	—	—	No Connection
129	#EPAD	—	—	EPAD Connect to VSS on PCB.



8. Function Description

8.1 Function Block Diagram

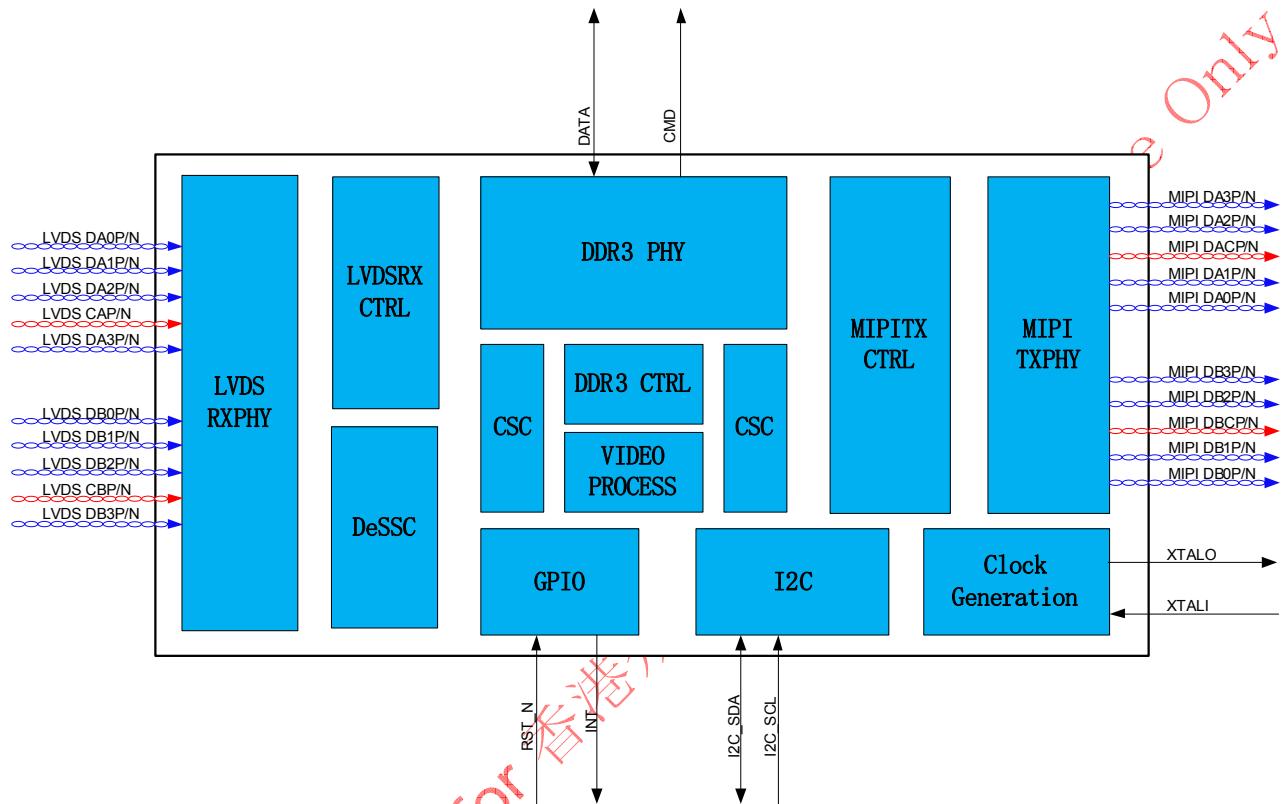


Figure 8.1.1 Function Block Diagram



9. Specification

9.1 Absolute Maximum Conditions

Table 9.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18_DDR, VDD	1.8V Power Supply Voltage	-0.3		2.0	V
VCC15_DDR	1.5V Power Supply Voltage	-0.3		1.6	V
VCCIO	1.8V/3.3V Power Supply Voltage	-0.3		3.68	V
Vi	CMOS Terminal Input Voltage Range	-0.3		2.0	V
Vo	CMOS Terminal Output Voltage Range	-0.3		2.0	V
Ts	Storage Temperature	-55		125	°C
ESD	HBM Electrostatic Discharge Level		4K		V

Notes:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

9.2 Normal Operating Conditions

Table 9.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18_DDR, VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCC15_DDR	1.5V Power Supply Voltage	1.425	1.5	1.575	V
VCC33	3.3V Power Supply Voltage	2.97	3.3	3.63	V
	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCCN	Power Supply Voltage Noise			50	mV
TA	Operating Free-air Temperature	-40	27	85	°C

9.3 DC Characteristics

Table 9.3.1 DC Characteristics

MIPI HS Line Transmitter DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
Vcm	HS Transmit Static Common mode Voltage	150	200	250	mV
Δ Vcm	HS Transmit Static Common mode Voltage Mismatch			5	mV
Vod	HS Transmit Differential Voltage	140	200	270	mV
Δ Vod	HS Transmit Differential Voltage Mismatch			14	mV
Vohhs	HS Transmit Output High Voltage			360	mV
Zos	Single ended output impedance	40	50	62.5	Ω
Δ Zos	Single ended output impedance Mismatch			10	%
MIPI LP Line Receiver DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit

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VIL	Input low voltage			550	mV
VIH	Input high voltage, data rate<1.5Gbps	880			mV
VHYST	Input hysteresis	740			mV

MIPI LP Line Transmitter DC Specifications

Symbol	Parameter	MIN	TYP	MAX	Unit
VOL	Output low-level SE voltage	-50	0	50	mV
VOH	Output high-level SE voltage	1.1	1.2	1.3	V
ZOLP	Single-ended output impedance	110			Ω
Δ ZOLP(01,10)	Single-ended output impedance mismatch driving opposite level			20	%
Δ ZOLP(00,11)	Single-ended output impedance mismatch driving same level			5	%

LVDS Receiver DC Specifications

Symbol	Parameter	MIN	TYP	MAX	Unit
VIDTH	Differential input high voltage threshold			50	mV
VIDTL	Differential input low voltage threshold	-50			mV
VCMRXDC	Input common mode voltage	0	1200	1800	mV
Rterm	Termination Resister	80	100	125	Ω
VIDTH	Differential input high voltage threshold			50	mV

DDR3 Single-Ended DC Specifications for Address and Command output

Symbol	Parameter	MIN	TYP	MAX	Unit
VIH.CA	DC input logic high	vref+0.1		VDD	V
VIL.CA	DC input logic low	VSS		vref-0.1	V
Vref.CA	Reference Voltage for ADD,CMD	0.49*VDD		0.51*VDD	V
Rterm	Termination Resister		50		Ω

DDR3 Single-Ended DC Specifications for DQ output

Symbol	Parameter	MIN	TYP	MAX	Unit
VIH.DQ	DC input logic high	vref+0.1		VDD	V
VIL.DQ	DC input logic low	VSS		vref-0.1	V
Vref.DQ	Reference Voltage for DQ,DM	0.49*VDD		0.51*VDD	V
Ron	Output driver impedance	34			Ω

DDR3 Differential DC Specifications for Clock and Strobe output

Symbol	Parameter	MIN	TYP	MAX	Unit
VIHdiff	Differential input high	0.2			V
VILdiff	Differential input low			-0.2	V
VSEH	Single-ended high level for strobes and clock	vref+0.175			V
VSEL	Single-ended low level for strobes and clock			vref-0.175	V

DDR3 Single-Ended DC Specifications for DQ input

Symbol	Parameter	MIN	TYP	MAX	Unit
VOH	DC output high measurement level	0.8*VDD			mV
VOM	DC output mid measurement level	0.5*VDD			mV
VOL	DC output low measurement level	0.2*VDD		200	mV
Rodt	On Die termination	20			Ω

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9.4 AC Characteristics

Table 9.4.1 AC Characteristics

MIPI HS Line Transmitter DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
$\Delta V_{cmrx}(hf)$	Common mode Voltage variation above 450MHz			15	mVrms
$\Delta V_{cmrx}(lf)$	Common mode Voltage variation between 50-450MHz			25	mVpeak
Rise/Fall Time 20%-80%	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
	Data rate >1.5Gbps	50		0.4UI	ps
MIPI LP Line Transmitter DC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
t_{rlp}, t_{lfp}	Single ended output rise/fall time, 15% to 85%, CL< 70pF			25	ns
t_{reot}	Single ended output rise/fall time, 30% to 85%, CL< 70pF			35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive-OR clock	20			ns
TLP-PER-TX	Period of the LP exclusive-OR clock	90			ns
$\delta V/\delta tSR$	Slew rate @ CLOAD = 0			500	mV/ns
	Slew rate @ CLOAD = 5pF			350	mV/ns
	Slew rate @ CLOAD = 20pF			250	mV/ns
	Slew rate @ CLOAD = 70pF			150	mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30– 0.075*(VO,INST -700)			mV/ns
MIPI LP Line Receiver AC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
LVDS Receiver AC Specifications					
Symbol	Parameter	MIN	TYP	MAX	Unit
CLK	Output clk cycle	6.25	Tc	37	ns
T0	Input data position0	-0.15	0	0.15	ns
T1	Input data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Input data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Input data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Input data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Input data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Input data position6	6Tc/7-0.15		6Tc/7+0.15	ns
DDR3 Single-Ended AC Specifications for Address and Command output					
Symbol	Parameter	MIN	TYP	MAX	Unit
VIH.CA	AC input logic high	vref+0.175			V
VIL.CA	AC input logic low			vref-0.175	V
Vref.CA	Reference Voltage for ADD,CMD	0.49*VDD		0.51*VDD	V
Rterm	Termination Resister		50		Ω

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Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Single-Ended AC Specifications for DQ output					
Symbol	Parameter	MIN	TYP	MAX	Unit
VIH.DQ	AC input logic high	vref+0.175			V
VIL.DQ	AC input logic low			vref-0.175	V
Rterm	Termination Resister		50		Ω
Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Differential AC Specifications for Clock and Strobe output					
Symbol	Parameter	MIN	TYP	MAX	Unit
VIHdiff	Differential input high	2*(VIH-Vref)			V
VILdiff	Differential input low			2*(VIL+Vref)	V
VIX.CK	Differential Output Cross Point Voltage relative to VDD/2 for CK	-175		175	mV
VIX.DQS	Differential Output Cross Point Voltage relative to VDD/2 for DQS	-150		150	V
Vovershoot	Amplitude allowed for overshoot area			0.4	V
Vundershoot	Amplitude allowed for undershoot area			0.4	V
DDR3 Single-Ended AC Specifications for DQ input					
Symbol	Parameter	MIN	TYP	MAX	Unit
VOH	AC output high measurement level	VTT+0.1*VDDQ			mV
VOL	AC output low measurement level			VTT-0.1*VDDQ	mV
DDR3 Differential AC Specifications for DQS input					
Symbol	Parameter	MIN	TYP	MAX	Unit
VOHdiff	AC differential output high measurement level	0.2*VDDQ			mV
VOLdiff	AC differential output low measurement level			-0.2*VDDQ	mV

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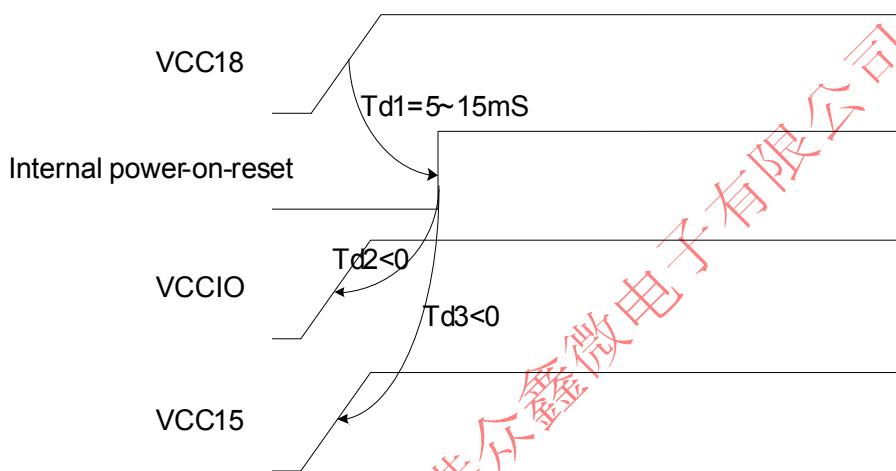


9.5 Power Consumption

Table 9.5.1 Dual-Port LVDS to MIPI Power Consumption

Symbol	Test Condition	Power Consumption	Unit
I _{VCC18}		TBD	mA
I _{VCC15}		TBD	mA
I _{VCCIO}		TBD	mA

9.6 Power-up and Reset Sequence



Note: Internal power-on-reset is generated by VCC18, VCCIO and VCC15 should be stable when Internal power-on-reset is high.

Figure 9.6.1 Power-up Sequence



10. Package Information

10.1 ePad Enhancement

The LT2911R is packaged in QFN128 package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

10.2 Package Dimensions

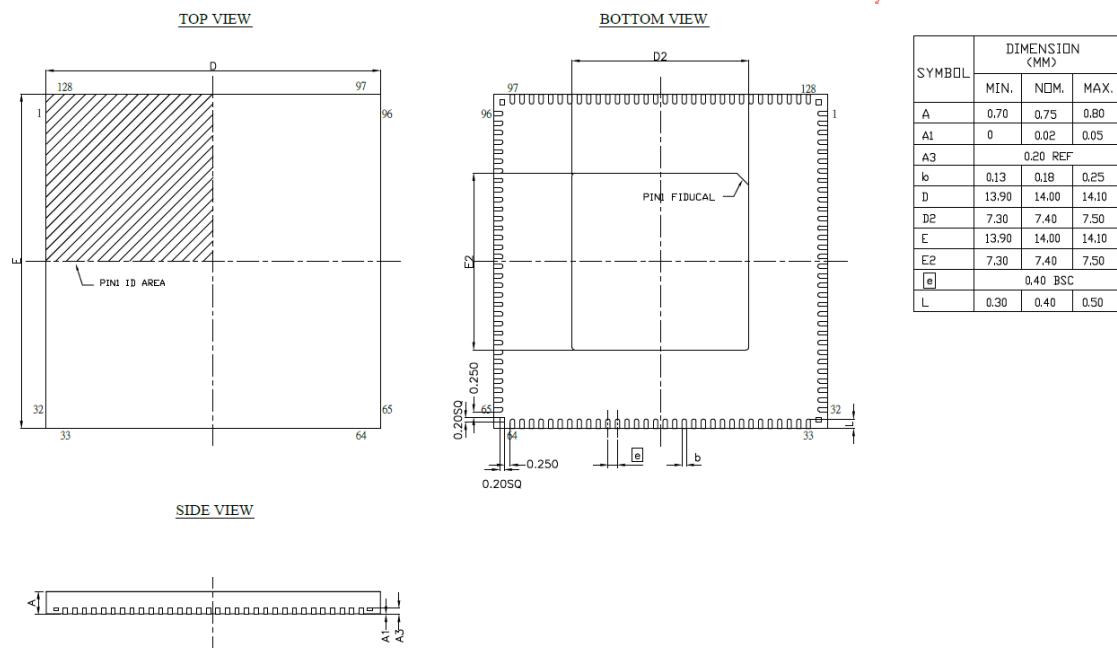


Figure 10.2.1 QFN128 Package Dimensions



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