Boost and Inverting Switching Regulator for CCD Bias

FEATURES

- **Generates 15V at 45mA, –8V at 90mA from a Li-Ion Cell**
- **Output Disconnect**
- **Sequencing: Positive Output Reaches Regulation Before Negative Channel Begins Switching**
- **Internal Schottky Diodes**
- **2MHz Constant Switching Frequency**
- **Requires Only One Resistor per Channel to Set Output Voltages**
- V_{IN} Range: 2.3V to 16V
- Output Voltage Up to 28V
- Short-Circuit Robust
- Capacitor Programmable Soft-Start
- Separate V_{BAT} Pin Allows Separate Sources for Power and Control Circuitry
- Available in 10-Lead (3mm × 3mm) DFN Package

APPLICATIONS

- CCD Bias
- TFT LCD Bias
- OLED Bias
- ±Rail Generation for Op Amps

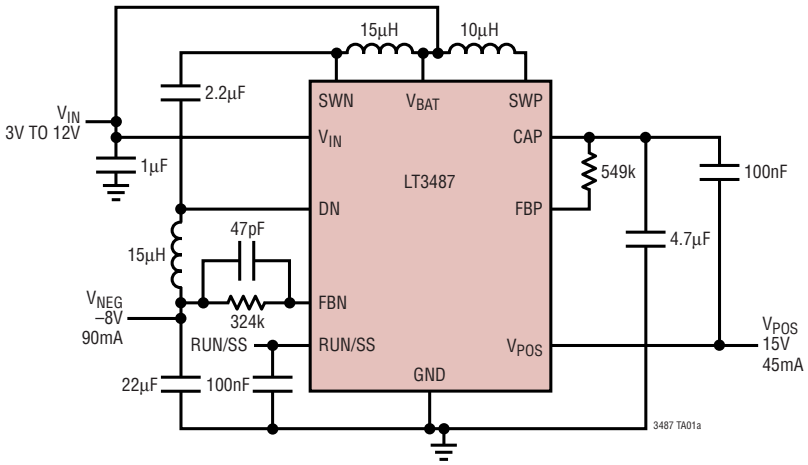
DESCRIPTION

The LT®3487 dual channel switching regulator generates positive and negative outputs for biasing CCD imagers. The device delivers up to –8V at 90mA and 15V at 45mA from a lithium-ion cell, providing bias for many popular CCD imagers. The boost regulator incorporates output disconnect technology to eliminate the DC current path from V_{IN} to the output load that is present in standard boost configurations. The 2MHz switching frequency allows CCD solutions using tiny, low profile capacitors and inductors and generates low noise outputs that are easy to filter. Schottky diodes are internal and the output voltages are set with one resistor per channel, reducing the external component count.

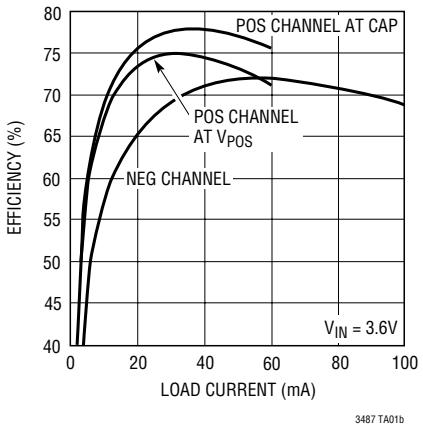
Intelligent soft-start allows sequential soft-start of the two channels with a single capacitor. The soft-start is sequenced such that the output ramp of the negative channel begins after the ramp of the positive channel. Internal sequencing circuitry also disables the negative channel until the positive channel has reached 87% of its final value, ensuring that the sum of the two outputs is always positive.

The LT3487 is available in a 10-pin 3mm × 3mm DFN package.

TYPICAL APPLICATION



Conversion Efficiency

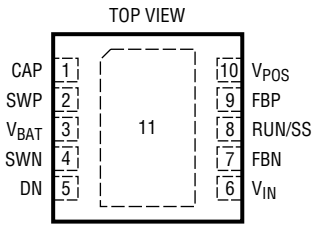


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 16V
V_{BAT} Voltage 16V
SWP, SWN Voltage 32V
CAP, V_{POS} 30V
DN Voltage ..... –32V
RUN/SS Voltage 8V
FBP Voltage 6V
FBN Voltage ..... –0.2V to 6V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 43°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE CONNECTED TO PCB

ORDER PART NUMBER	DD PART MARKING
LT3487EDD	LBXB

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{BAT} = 3.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range			2.3		16	V
Quiescent Current	RUN/SS = 3V, Not Switching RUN/SS = 0V			3.7 5.3	5 8	mA µA
RUN/SS Voltage Threshold (Full Current)	(Note 3)				1.6	V
RUN/SS Voltage Threshold (Shutdown)		●	100	160		mV
RUN/SS Pin Current	RUN/SS = 0V (Note 4)		1	1.4	2	µA
FBP (Positive Channel) Pin Voltage		●	1.19	1.23	1.27	V
FBN (Negative Channel) Pin Voltage		●	–7	3	12	mV
FBP Pin Voltage Line Regulation				0.007		%/V
FBN Pin Voltage Line Regulation				0.001		mV/V
FBP Pin Bias Current		●	24.4	25	25.6	µA
FBN Pin Bias Current		●	24.4	25	25.6	µA
FBP Threshold (Percent of Final Value) to Start Negative Channel				87	90	%
Switching Frequency			1.85	2	2.15	MHz
Maximum Duty Cycle		●	87	93		%
Positive Channel Switch Current Limit	(Note 5)	●	750	920		mA
Negative Channel Switch Current Limit	(Note 5)	●	900	1090		mA
Positive Channel V_{CESAT}	I_{SWP} = 400mA			280		mV
Negative Channel V_{CESAT}	I_{SWN} = 600mA			340		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, V_{BAT} = 3.6V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Schottky DP Forward Drop	I_{SWP} = 400mA			1045		mV
Schottky DN Forward Drop	I_{SWN} = 600mA			980		mV
Disconnect PNP V_{CE}	I_{VPOS} = 50mA			205		mV
Disconnect Current Limit	V_{CAP} = 15V, V_{POS} = 0V		100	155		mA
$V_{CAP} – V_{BAT}$ to Disconnect	V_{BAT} = 3.6V, V_{POS} = 0V, I_{CAP} < 100µA			1.2	1.6	V
Disconnect Leakage	V_{BAT} = 3.6V, CAP = 3.6V, V_{POS} = 0V			0.1	1.0	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3487E is guaranteed to meet specified performance from 0°C to 85°C. Specifications over the –40°C to 85°C operating range are assured by design, characterization and correlation with statistical process controls.

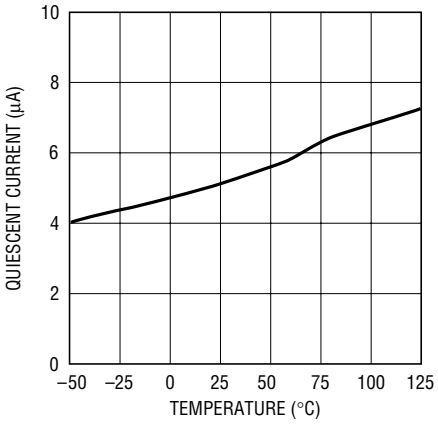
Note 3: Guaranteed by design, not directly tested.

Note 4: Current flows out of pin.

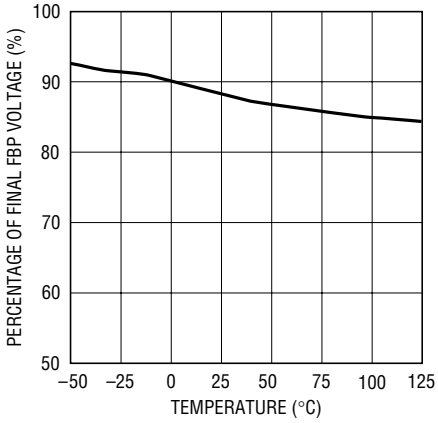
Note 5: Current limit guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

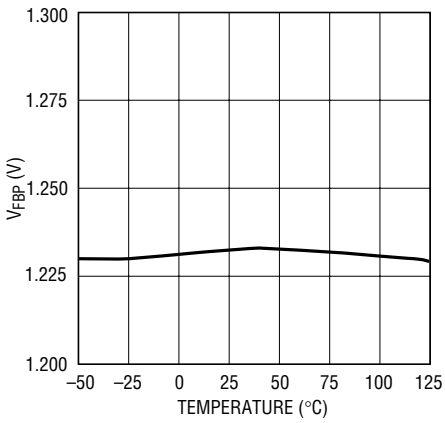
Shutdown Quiescent Current



Positive Output to Enable Inverter

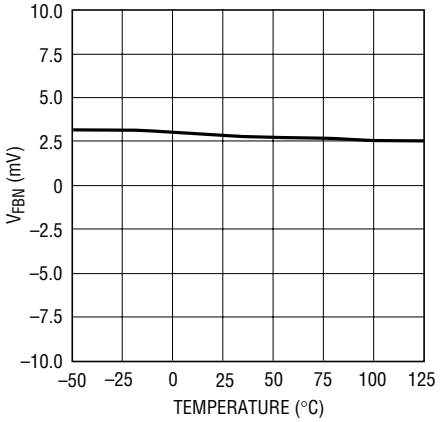


FBP Voltage



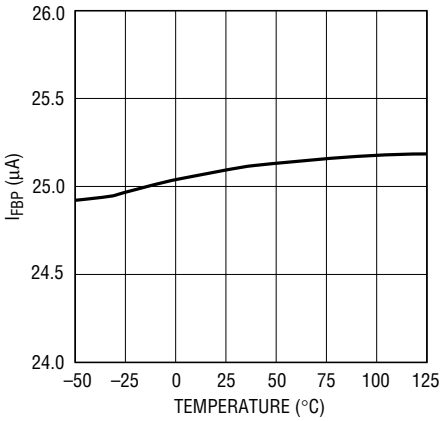
TYPICAL PERFORMANCE CHARACTERISTICS

FBN Voltage



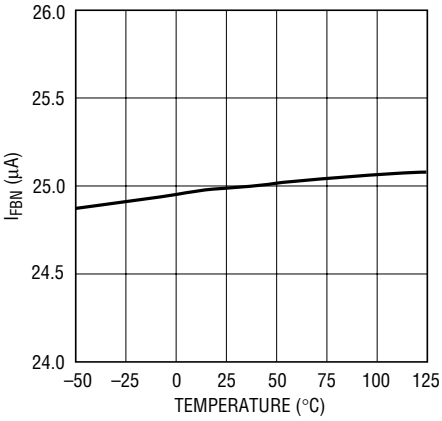
3487 G04

FBP Bias Current



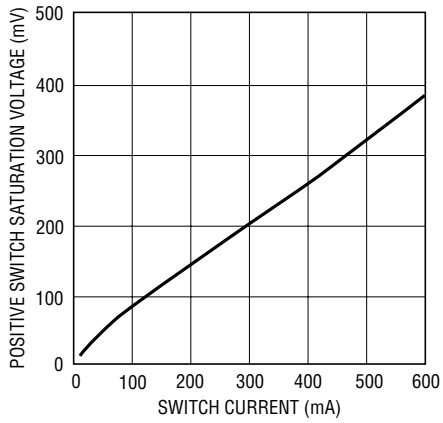
3487 G05

FBN Bias Current



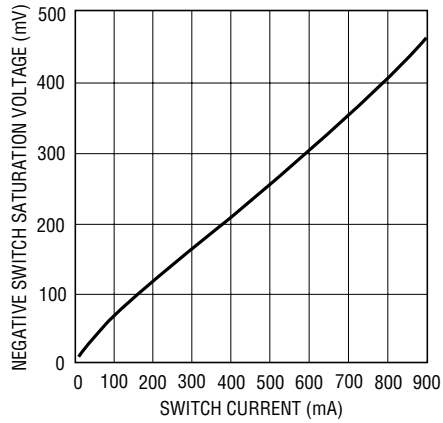
3487 G06

Positive Channel Switch $V_{CE(SAT)}$



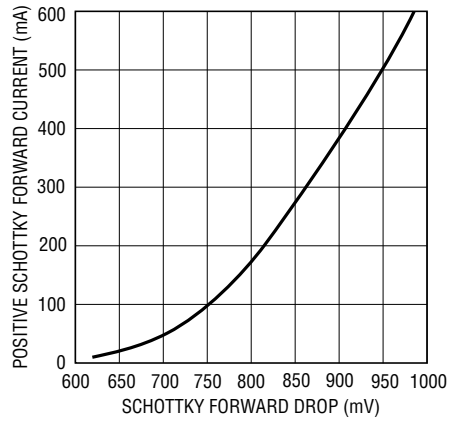
3487 G07

Negative Channel Switch $V_{CE(SAT)}$



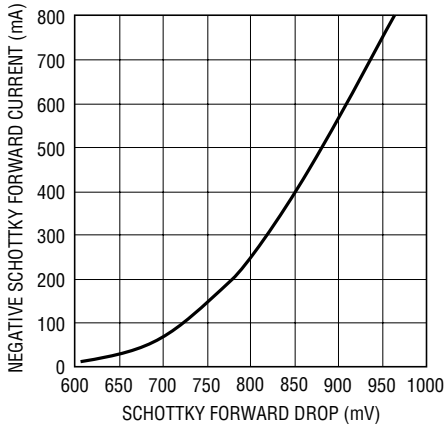
3487 G08

Positive Channel Schottky I-V Characteristic



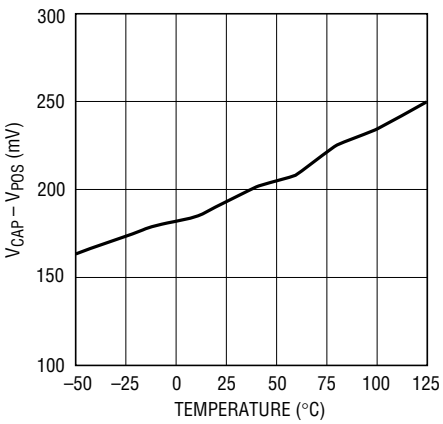
3487 G09

Negative Channel Schottky I-V Characteristic



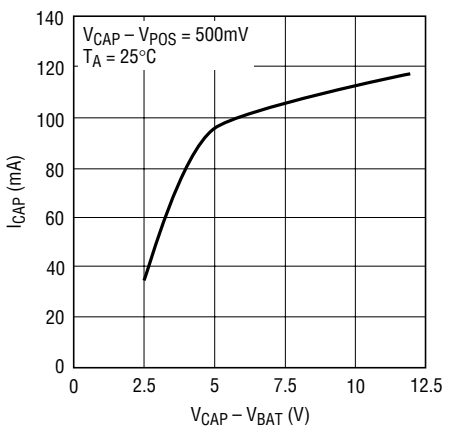
3487 G10

Output Disconnect Voltage Drop (50mA Load)



3487 G11

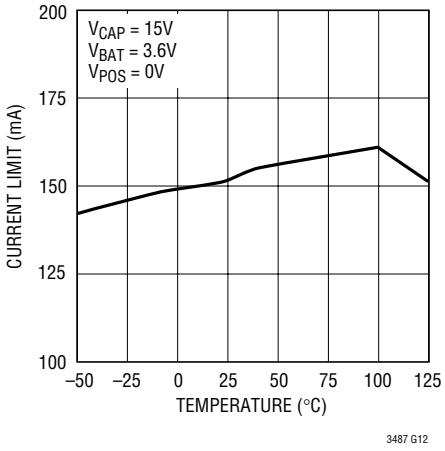
Maximum Disconnect Current



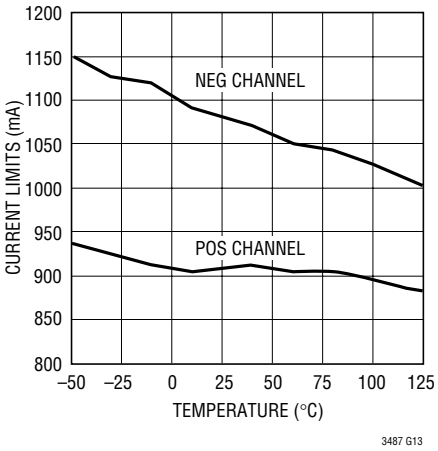
3487 G20

TYPICAL PERFORMANCE CHARACTERISTICS

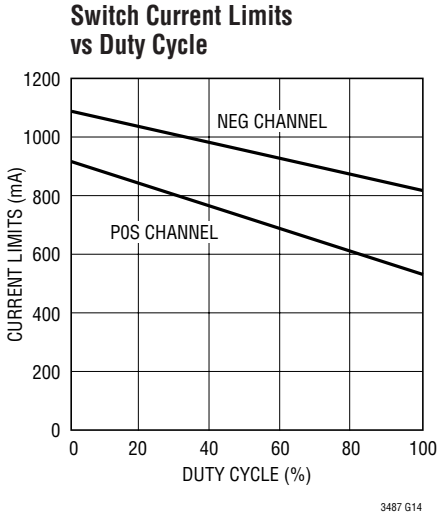
Output Disconnect Current Limit



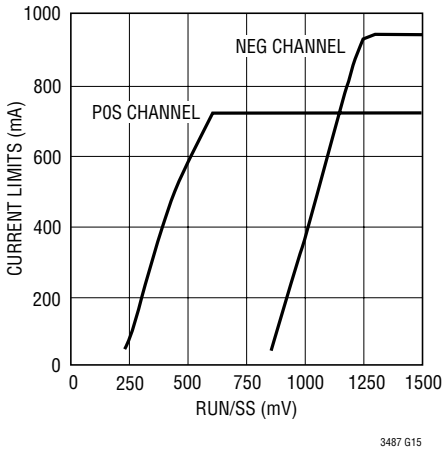
Switch Current Limits



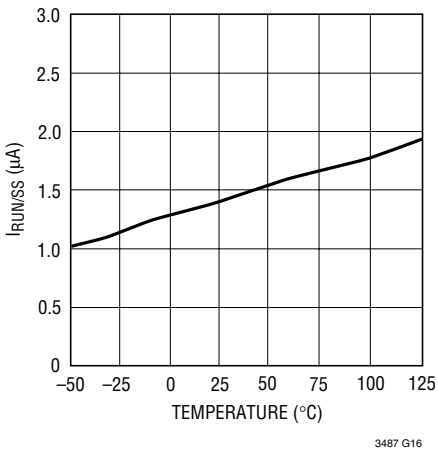
Switch Current Limits vs Duty Cycle



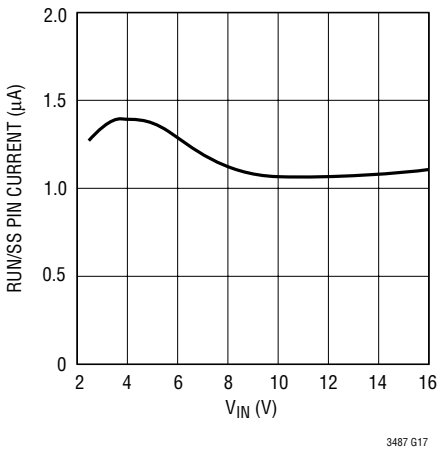
Switch Current Limits vs RUN/SS Voltage (at 55% Duty Cycle)



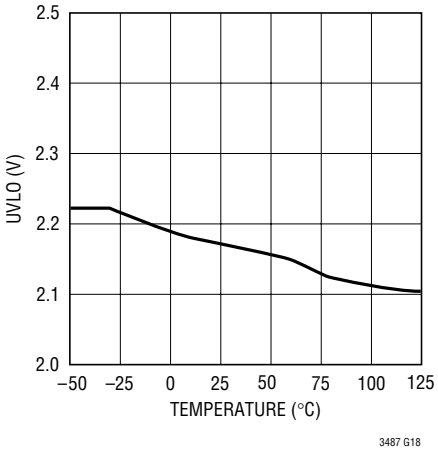
RUN/SS Pin Current in Shutdown



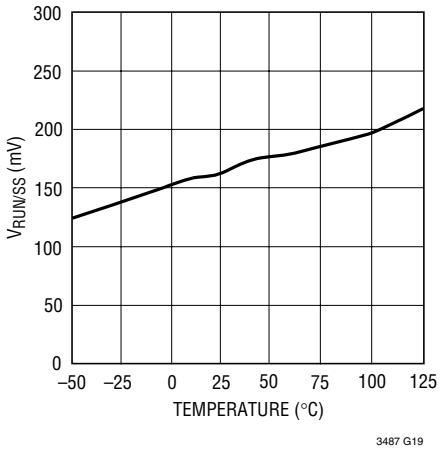
RUN/SS Pin Current vs V_{IN} in Shutdown



UVLO Voltage



RUN/SS Shutdown Threshold



PIN FUNCTIONS

CAP (Pin 1): Disconnect-PNP Emitter and Positive Schottky Cathode. Acts as an intermediate positive (boost) output. Connect boost output capacitor to this pin.

SWP (Pin 2): Switch Pin and Schottky Anode for Positive Channel. Connect boost inductor to this pin.

V_{BAT} (Pin 3): Battery Voltage. Connect this pin to the supply voltage for the boost inductor. The disconnect drive current is returned to this pin. The disconnect operates until CAP falls to 1.2V above V_{BAT}.

SWN (Pin 4): Switch Pin for Negative (Inverter) Channel. Connect inverter input inductor and flying capacitor here.

DN (Pin 5): Anode of Internal Schottky for Inverter. Connect inverter output inductor and flying capacitor here.

V_{IN} (Pin 6): Input Supply Pin. V_{IN} is used to power the control circuitry of the LT3487. This pin must be locally bypassed with an X5R or X7R type ceramic capacitor.

FBN (Pin 7): Feedback Pin for Inverter. Connect feedback resistor R2 from this pin to V_{NEG}. Choose R2 according to:

$$R2 = -\frac{V_{NEG}}{25\mu A}$$

Pin voltage = 0V when regulated.

RUN/SS (Pin 8): Run/Soft-Start Pin. Connect to an open-drain transistor. The transistor must sink 1.4µA from RUN/SS. Pull RUN/SS below 100mV to shut down the chip. Connect a capacitor from RUN/SS to ground to program soft-start functionality. The soft-start will slowly bring the boost channel into regulation and then slowly bring up the inverter. RUN/SS must be above 1.6V to allow both channels to reach full current. If soft-start is not required, this pin can be driven with a logic signal, but the RUN/SS voltage must remain below V_{IN}.

FBP (Pin 9): Feedback Pin for Boost. Connect boost feedback resistor R1 from FBP to CAP. Choose R1 according to:

$$R1 = \frac{V_{POS} - 1.23}{25\mu A}$$

Pin voltage = 1.23V when regulated.

V_{POS} (Pin 10): Output Pin for Boost Channel. V_{POS} is the collector of the output disconnect PNP. Connect the boost load to V_{POS}. Connect capacitor C5 between CAP and V_{POS} for stability.

Exposed Pad (Pin 11): GND. Tie directly to ground plane through multiple vias under the package for optimum thermal performance.

BLOCK DIAGRAM

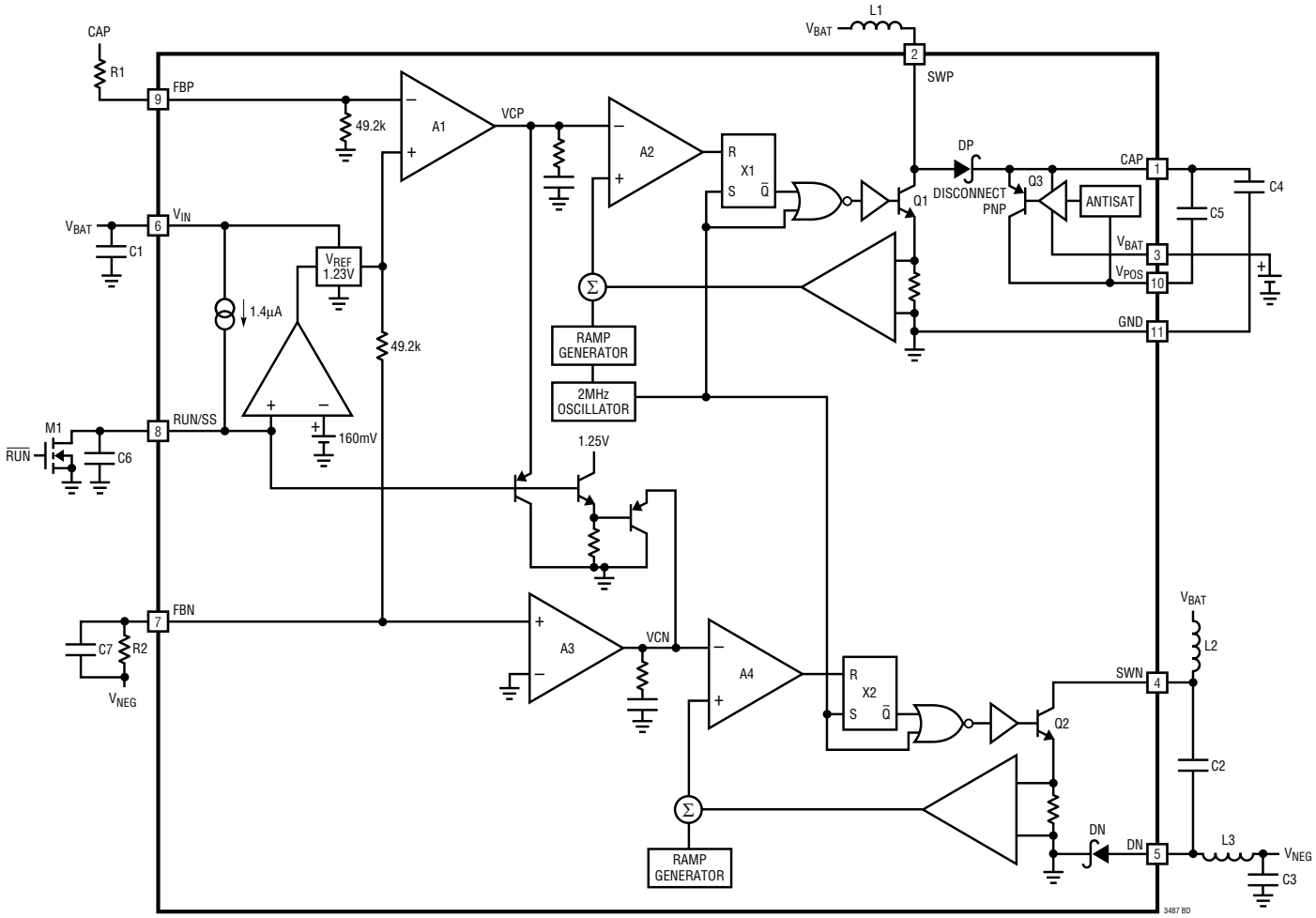


Figure 1. Block Diagram

APPLICATIONS INFORMATION

Operation

The LT3487 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. Operation can be best understood by referring to the Block Diagram in Figure 1. At the start of each oscillator cycle, the SR latch X1 is set, which turns on the power switch Q1. A voltage proportional to the switch current is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A2. When this voltage exceeds the level at the negative input of A2, the SR latch X1 is reset, turning off the power switch Q1. The level at the negative input of A2 is set by the error amplifier A1, and is simply an amplified version of the difference between the feedback voltage and the reference voltage of 1.23V. In this manner, the error amplifier sets the correct peak current level to keep the output in regulation. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. The second channel is an inverting converter. The basic operation is the same as the positive channel. The SR latch X2 is also set at the start of each oscillator cycle. The power switch Q2 is turned on at the same time as Q1. Q2 turns off based on its own feedback loop, which consists of error amplifier A3 and PWM comparator A4. The reference voltage of this negative channel is ground. Voltage clamps on V_{CP} and V_{CN} (not shown) enforce current limit. Switching waveforms with typical load conditions are shown in Figure 2.

The PNP Q3 is used as an output disconnect pass transistor. Q3 disconnects the load from the input during shutdown. The anti-sat driver keeps Q3 at the edge of saturation as long as CAP is typically 1.2V and worst-case 1.6V (cold) above the V_{BAT} voltage. The drive current for the output disconnect PNP is returned to the V_{BAT} pin. This allows the pass transistor to turn off when the CAP voltage falls to less than 1.2V above V_{BAT}. The V_{BAT} pin allows applications in which the power (inductors L1 and L2) and internal control circuitry (V_{IN} pin) are powered from different sources.

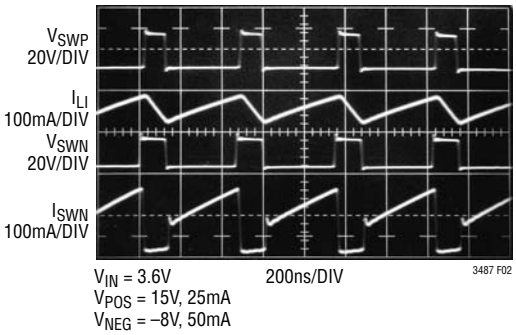


Figure 2. Switching Waveforms

Inductor Selection

A 10µH inductor is recommended for the LT3487 boost channel. The inverting channel can use uncoupled 15µH inductors, or coupled 10µH inductors. Small size and high efficiency are the major concerns for most LT3487 applications. Inductors with low core losses and small DCR (copper wire resistance) at 2MHz are good choices for LT3487 applications. The inductor DCR should be on the order of half of the switch on-resistance for its channel. Some inductors in this category with small size are listed in Table 1.

Table 1. Recommended Inductors

PART NUMBER	INDUCTANCE (µH)	DCR (Ω)	CURRENT RATING (mA)	MANUFACTURER
DB318C-A997AS-100M	10	0.18	580	Toko www. tokoam.com
CDRH3D18-100	10	0.205	900	Sumida www.sumida.com
CDRH2D18HP-100	10	0.245	850	
CDRH3D23-100	10	0.117	850	
CDRH2D18/HP-150	15	0.345	700	
CDRH3D18-150	15	0.301	750	
CDRH3D23-150	15	0.191	700	

Capacitor Selection

The small size of ceramic capacitors makes them suitable for LT3487 applications. X5R and X7R types of ceramic capacitors are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 1µF input capacitor is sufficient for most LT3487 applications. The output capacitors required for stability depend on the application. For the typical Li-Ion to +15V, –8V application, the positive channel requires a 4.7µF output capacitor and the negative channel requires at least 10µF of capacitance.

APPLICATIONS INFORMATION

Table 2. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	PHONE	URL
Taiyo Yuden	(408) 573-4150	www.t-yuden.com
Murata	(814) 237-1431	www.murata.com
Kemet	(408) 986-0424	www.kemet.com

Inrush Current

The LT3487 uses internal Schottky diodes. When a supply voltage is abruptly applied to the V_{IN} pin, the voltage difference between V_{IN} and V_{CAP} generates inrush current flowing from the input through the inductor L1 and the internal Schottky diode DP to charge the boost output capacitor C4. For the inverting channel, there is a similar inrush current flowing from the input through the inductor L2 path, charging the flying capacitor C2 and returning through the internal Schottky diode DN. The maximum current the Schottky diodes in the LT3487 can sustain is 2A. The selection of inductor and capacitor values should ensure that the peak inrush current is below 2A. The peak inrush current can be calculated as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \bullet \omega} \bullet e^{-\frac{\alpha}{\omega} \bullet \arctan\left(\frac{\omega}{\alpha}\right)} \bullet \mathrm{SIN}\left[\arctan\left(\frac{\omega}{\alpha}\right)\right]$$

$$\alpha = \frac{r + 1.5}{2 \bullet L}$$

$$\omega = \sqrt{\frac{1}{L \bullet C} - \frac{r}{4 \bullet L^2}}$$

where L is the inductance, r is the resistance of the inductor and C is the output capacitance. For low DCR inductors, which is usually the case for this application, the peak inrush current can be simplified as follows:

$$I_P = \frac{V_{IN} - 0.6}{L \bullet \omega} \bullet e^{\left(-\frac{\alpha}{\omega} \bullet \frac{\pi}{2}\right)}$$

Table 3 gives inrush peak currents for some component selections. Note that inrush current is not a concern if the input voltage rises slowly.

Table 3. Inrush Peak Current

V_{IN} (V)	R (Ω)	L (µH)	C (µF)	I_P (A)
5	0.18	10	4.7	1.44
5	0.235	15	2.2	1.06
3.6	0.18	10	4.7	0.979
3.6	0.245	10	4.7	0.958
3.6	0.345	15	2.2	0.704

External Diode Selection

As stated previously, the LT3487 has internal Schottky diodes. The Schottky diode, DP, is sufficient for most step-up applications. However, for high current inverter applications, a properly selected external Schottky diode in parallel with DN can improve efficiency. For external diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes rated for higher current usually have lower forward voltage drops and larger capacitance, which can cause significant switching losses at a 2MHz switching frequency. Some recommended Schottky diodes are listed in Table 4.

Table 4. Recommended Schottky Diodes

PART NUMBER	FORWARD CURRENT (mA)	FORWARD VOLTAGE DROP (V)	DIODE CAPACITANCE (pF at 10V)	MANUFACTURER
PMEG2010AEB	1000	0.51	7.5	Philips www.semiconductors.philips.com
CMDSH2-3	200	0.49	15	Central Semiconductor www.centralsemi.com
RSX051VA-30	500	0.35	30	ROHM www.rohm.com
ZHCS400	400	0.425	18	Zetex www.zetex.com

APPLICATIONS INFORMATION

Setting the Output Voltages

The LT3487 has an accurate internal feedback resistor that is trimmed to set the feedback currents to 25µA for each channel. Only one resistor is needed to set the output voltage for each channel. The output voltage can be set according to the following formulas:

$$R1 = \left(\frac{V_{POS} - 1.23}{25\mu A} \right)$$

$$R2 = \frac{-V_{NEG}}{25\mu A}$$

In order to maintain accuracy, high precision resistors are preferred (1% is recommended).

Soft-Start

The LT3487 has a single soft-start control for both channels. The RUN/SS pin is fed by a 1.4µA current source. The soft-start ramp can be programmed by connecting a capacitor from the RUN/SS pin to ground. An open-drain transistor should be used to pull the pin low to shut down the LT3487. Once the transistor stops sinking the 1.4µA, the capacitor begins to charge. The chip starts up when the RUN/SS pin charges to 160mV. The V_{CP} node voltage follows the RUN/SS voltage as it continues to ramp up to ensure slow start-up on the positive channel. The V_{CN} node follows the ramp voltage, down a V_{BE}. This ensures that the negative channel starts up after the positive, but still has a slow ramping output to avoid large start-up currents.

Start Sequencing

The LT3487 also has internal sequencing circuitry that inhibits the negative channel from operating until the feedback voltage of the boost channel reaches about 1.1V (87% of the final voltage), ensuring that the sum of the two outputs is always positive.

There are two ways in which the negative channel may start up, depending on the size of the soft-start capacitor. If there is no soft-start capacitor, or a very small capacitor, then the negative channel will start up when the positive output reaches 87% of its final value. If a large enough soft-start capacitor is used, then the RUN/SS voltage will continue to clamp the negative channel past the point where the positive channel is in regulation. Figure 3 shows the start-up sequencing without soft-start, with a small soft-start capacitor, and a large soft-start capacitor.

Output Disconnect

The output disconnect uses a PNP transistor with circuitry that varies the base current such that the transistor is consistently at the edge of saturation, thus yielding the best compromise between $V_{CE(SAT)}$ and low quiescent current. To remain stable, this circuit requires a bypass capacitor connected between the V_{POS} pin and the CAP pin or between the V_{POS} pin and ground. A ceramic capacitor with a value of at least 0.1µF is a good choice. Figure 4 shows that the PNP can support load currents of 50mA with a V_{CE} less than 210mV. The disconnect transistor is current limited to provide a maximum of 155mA in short circuit.

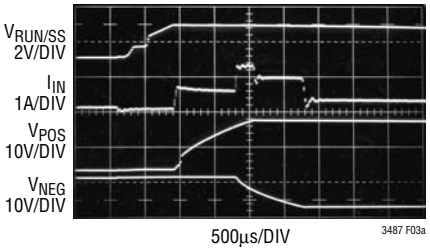


Figure 3a. $V_{RUN/SS}$, V_{POS}, V_{NEG}, I_{IN} with No Soft-Start Capacitor

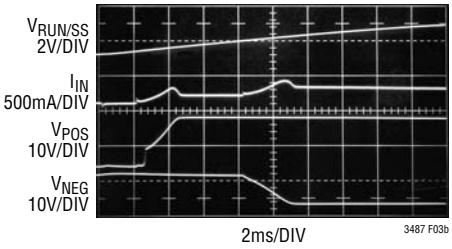


Figure 3b. $V_{RUN/SS}$, V_{POS}, V_{NEG}, I_{IN} with a 10nF Soft-Start Capacitor

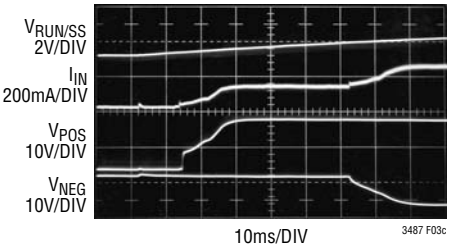


Figure 3c. V_{RUN}/SS, V_{POS}, V_{NEG}, I_{IN} with a 100nF Soft-Start Capacitor

APPLICATIONS INFORMATION

Choosing a Feedback Node

The positive channel feedback resistor, R1, may be connected to the V_{POS} pin or to the CAP pin (see Figure 5). Regulating the V_{POS} pin eliminates the output offset resulting from the voltage drop across the output disconnect. However, in the case of a short-circuit fault at the V_{POS} pin, the LT3487 will switch continuously because the FBP pin is low. While operating in this open-loop condition, the rising voltage at the CAP pin is limited only by the current limit of the output disconnect. Given worst-case parameters this voltage may reach 18V in a Li-Ion application. Care must be taken in high V_{IN} applications when regulating from the V_{POS} pin. When the short-circuit is removed, the V_{POS} pin will bounce up to the voltage on the CAP pin, potentially exceeding the programmed output voltage until the capacitor voltages fall back into regulation. While this is harmless to the LT3487, this should be considered in the context of the external circuitry if short-circuit events are expected. Regulating the CAP pin ensures that the voltage on the V_{POS} pin never exceeds the set output voltage after a short-circuit event. However, this setup does not compensate for the voltage drop across the output disconnect, resulting in an output voltage that is slightly lower than the voltage set by the feedback resistor. This voltage drop (V_{DISC}) can be accounted for when using the CAP pin as the feedback node by setting the output voltage according to the following formula (using V_{DISC} from Figure 4):

$$R1 = \frac{V_{POS} + V_{DISC} - 1.23}{25\mu A}$$

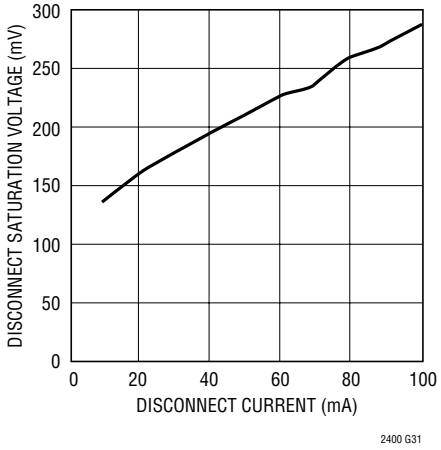


Figure 4. V_{CE} vs I of Output Disconnect

V_{BAT}

The V_{BAT} pin is a new innovation in the LT3487 that allows output disconnect operation in a wide range of applications. The V_{BAT} pin allows the part to stay on until CAP is less than 1.2V above V_{BAT}. This ensures that the positive bias doesn't fall before the negative bias discharges. In some applications it may be useful to power the inductors from a different source than V_{IN}. In this case, connect V_{BAT} to the source powering the inductors to allow proper operation of the disconnect. For example, in an automotive system there may already be a buck regulator producing 3.3V from a 12V battery. The LT3487 enables the user to power V_{IN} from the 3.3V rail, but power the V_{BAT} pin

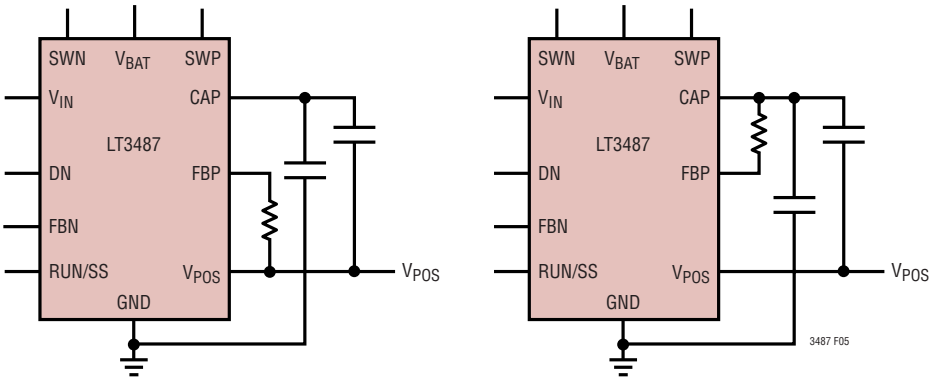


Figure 5. Feedback Connection Using the V_{POS} and CAP Pins

APPLICATIONS INFORMATION

and the inductors directly from the battery for higher efficiency. When the part goes into shutdown, the output load is isolated from the 12V source as soon as the CAP node falls to below V_{BAT} plus 1.2V (13.2V in this case). The V_{BAT} pin is also useful in a system using a 2V supply (such as a 2-cell alkaline battery), below the operating range of the LT3487. A boost converter designed for low voltage operation can provide 3.3V for the LT3487 V_{IN} pin, while the inductors and V_{BAT} can still be powered from the 2V supply. In shutdown, the 3.3V supply will turn off, but the output disconnect will still decouple the output load as soon as CAP falls below 3.2V .

Board Layout Consideration

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signals of the SWP and SWN pins have rise and fall times of a few ns. Minimize the length and area of all traces connected to the SWP and SWN pins and always use a ground plane under the switching regulator to minimize interplane coupling. Recommended component placement is shown in Figure 6.

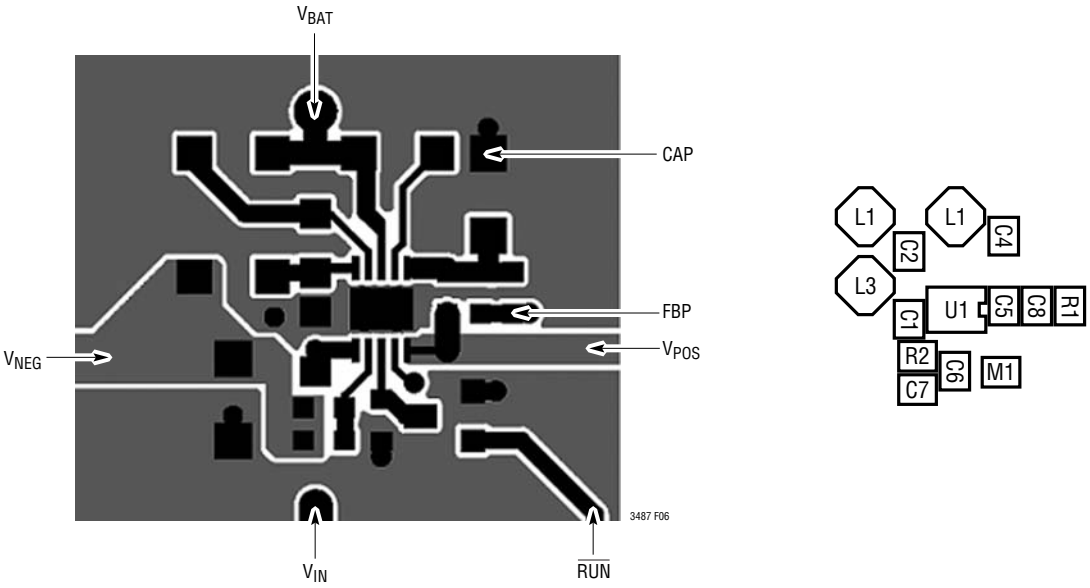
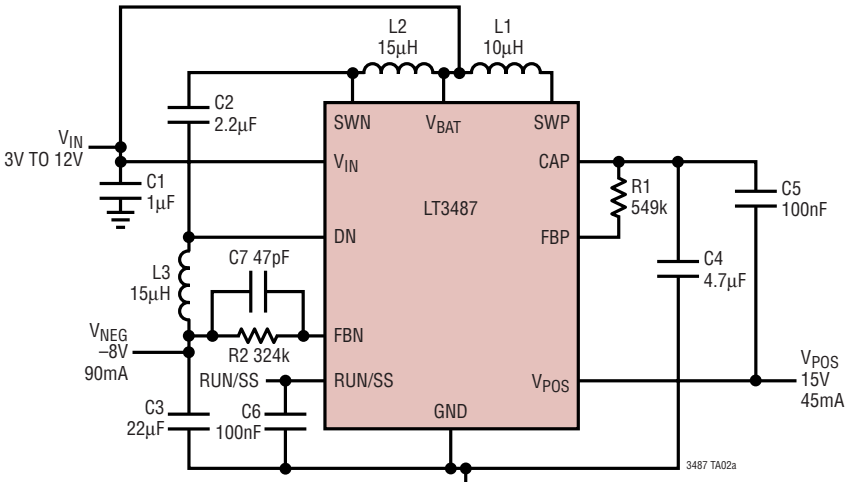


Figure 6. Recommended Component Placement

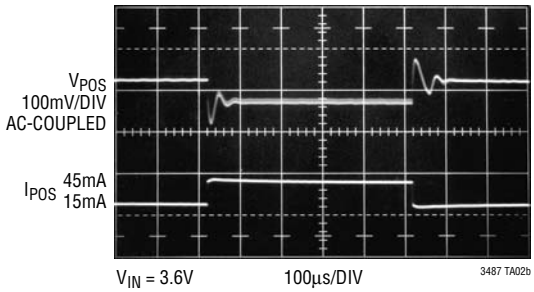
TYPICAL APPLICATION

+15V and –8V Boost and Inverting CCD Bias

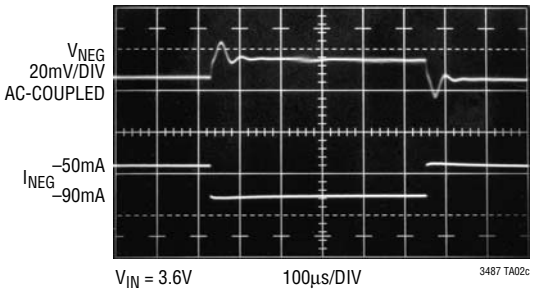


C1: TAIYO YUDEN EMK212BJ105MG
C2: TAIYO YUDEN TMK212BJ225MG
C3: TAIYO YUDEN TMK325BJ226MM
C4: TAIYO YUDEN TMK316BJ475ML-TR
L1: TOKO DB318C-A997AS-100M
L2, L3: SUMIDA CDRH2D18/HP-150NC

V_{POS} Load Step Response

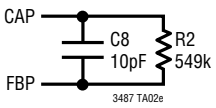


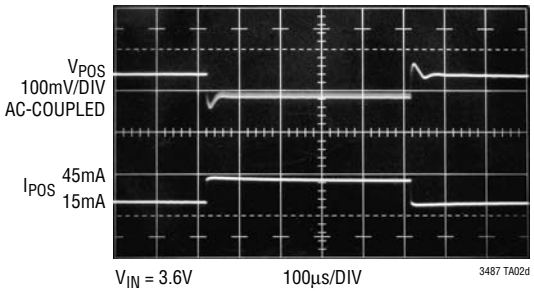
V_{NEG} Load Step Response



The positive channel's response is stable, but slightly underdamped. A phase lead capacitor (C8) can be added to provide more ideal phase margin.

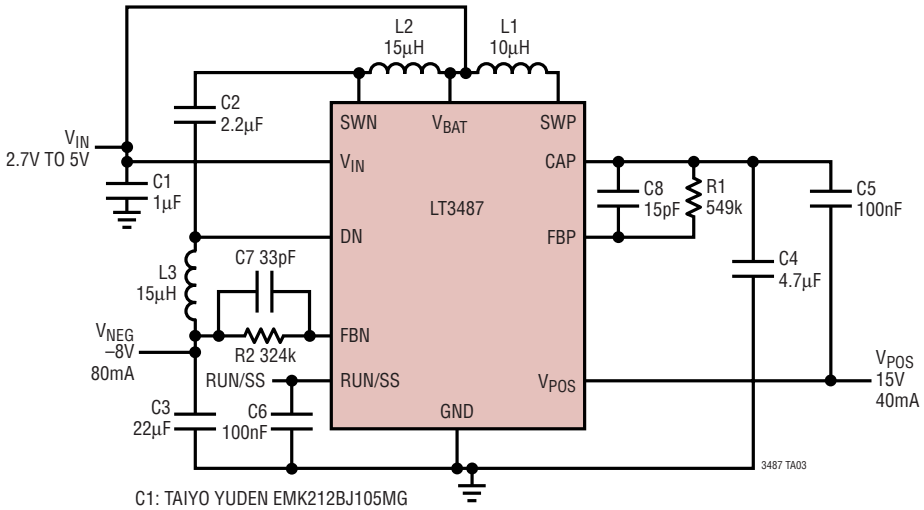
V_{POS} Load Step Response (with Phase Lead Capacitor)





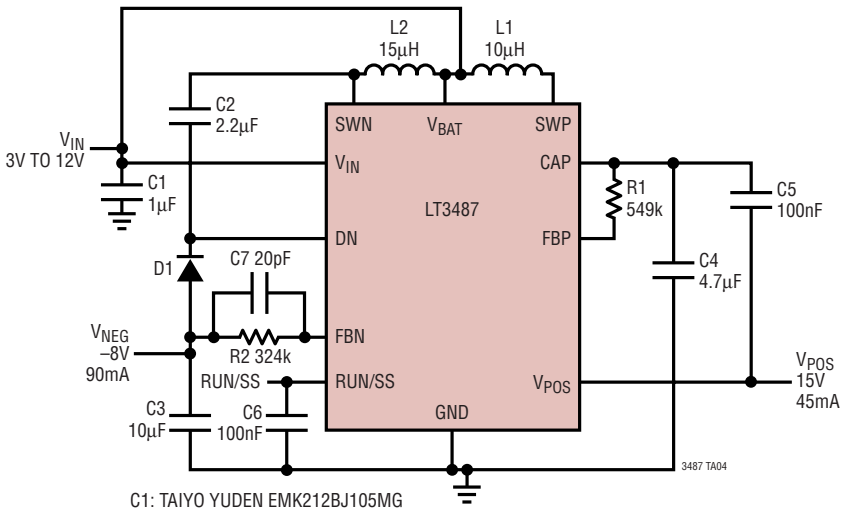
TYPICAL APPLICATIONS

+15V and –8V Low V_{IN} CCD Bias



C1: TAIYO YUDEN EMK212BJ105MG
C2: TAIYO YUDEN EMK212BJ225MD-TR
C3: TAIYO YUDEN TMK325BJ226MM
C4: TAIYO YUDEN TMK316BJ475ML-TR
L1: TOKO DB318C-A997AS-100M
L2, L3: SUMIDA CDRH2D18/HP-150NC

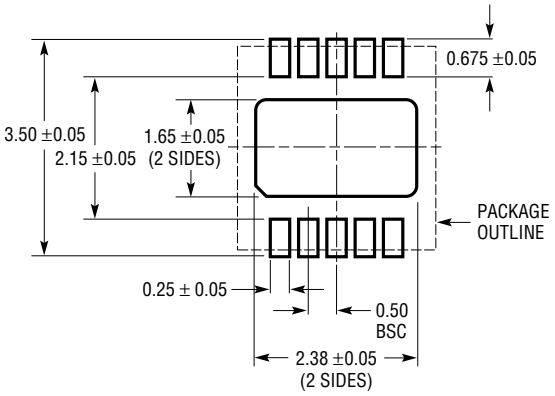
+15V and –8V Boost and Charge Pump CCD Bias



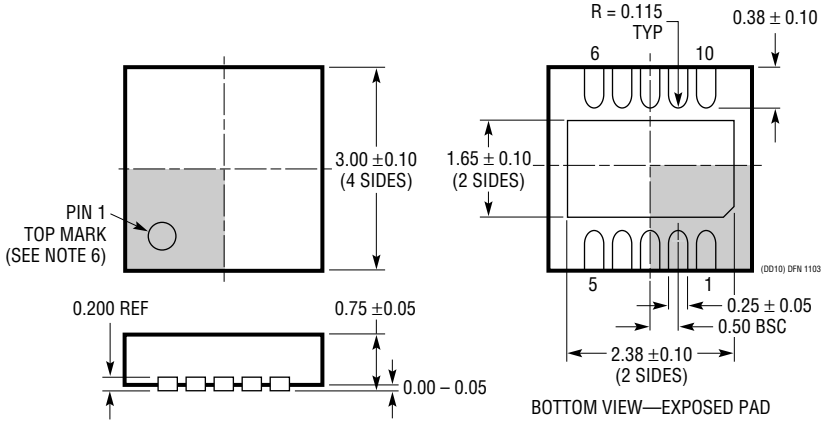
C1: TAIYO YUDEN EMK212BJ105MG
C2: TAIYO YUDEN TMK212BJ225MG
C3: TAIYO YUDEN EMK316BJ106ML
C4: TAIYO YUDEN TMK316BJ475ML-TR
D1: PHILIPS PMEG2010AEB
L1: TOKO DB318C-A997AS-100M
L2, L3: SUMIDA CDRH2D18/HP-150NC

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

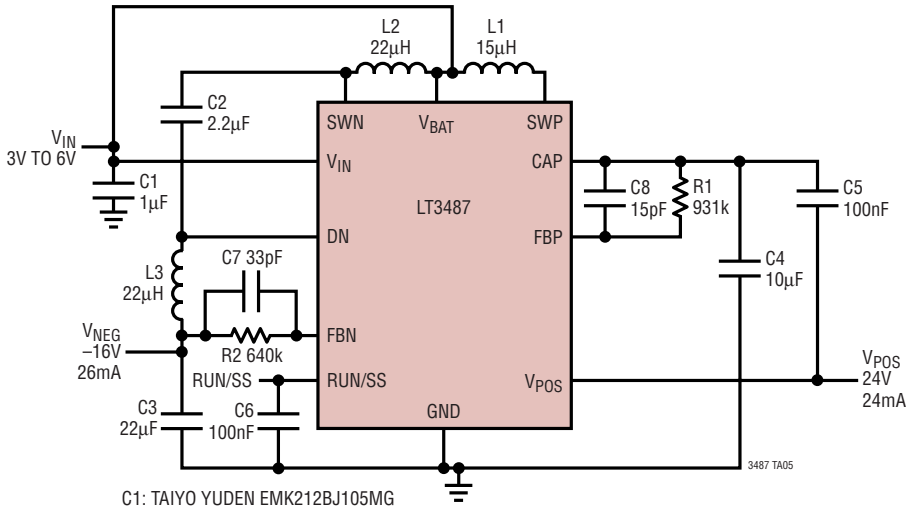


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

+24V and –16V LCD Bias



C1: TAIYO YUDEN EMK212BJ105MG
C2: TAIYO YUDEN TMK212BJ225MG
C3: TAIYO YUDEN TMK325BJ226MM
C4: TAIYO YUDEN TMK316BJ106KL-T
L1: SUMIDA CDRH2D18/HP-150NC
L2, L3: TOKO D53LC-A915AY-220M

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1944/LT1944-1	Dual Output 350mA/100mA I_{SW}, Constant Off-Time, High Efficiency DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, 10-Lead MS Package
LT1945	Dual Output, Boost/Inverter, 350mA I_{SW}, Constant Off-Time, High Efficiency DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MS Package
LT1947	Triple Output, 3MHz, High Efficiency DC/DC Converter	V_{IN}: 2.6V to 8V, $V_{OUT(MAX)}$ = ±34V, I_Q = 9.5mA, I_{SD} < 1µA, 10-Lead MS Package
LTC®3450	Triple Output, 550kHz, High Efficiency DC/DC Converter	V_{IN}: 1.4V to 4.6V, $V_{OUT(MAX)}$ = ±15V, I_Q = 75µA, I_{SD} < 2µA, DFN Package
LT3463/LT3463A	Dual Output, Boost/Inverter, 250mA I_{SW}, Constant Off-Time, High Efficiency DC/DC Converter with Integrated Schottkys	V_{IN}: 2.2V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.8mA, I_{SD} < 1µA, DFN Package
LT3471	Dual Output, Boost/Inverter, 1.3A I_{SW}, 1.2MHz, High Efficiency DC/DC Converter	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} < 1µA, DFN Package
LT3472/LT3472A	Dual Output, Boost/Inverter, 350mA/400mA I_{SW}, 1.2MHz, High Efficiency DC/DC Converter with Integrated Schottkys	V_{IN}: 2.3V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} < 1µA, DFN Package

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