1kHz-3GHz High Signal Level Down-Converting Mixer

FEATURES

- **Broadband RF, LO and IF Operation**
- **High Input IP3: +21dBm at 900MHz**
  +17dBm at 1900MHz
- **Typical Conversion Gain: 1dB at 1900MHz**
- **SSB Noise Figure: 11dB at 900MHz**
  14dB at 1900MHz
- **Integrated LO Buffer: Insensitive to LO Drive Level**
- **Single-Ended or Differential LO Signal**
- **High LO-RF Isolation**
- Enable Function
- 4.5V to 5.25V Supply Voltage Range
- 4mm × 4mm QFN Package

DESCRIPTION

The LT®5512 is a broadband mixer IC optimized for high linearity downconverter applications including cable and wireless infrastructure. The IC includes a differential LO buffer amplifier driving a double-balanced mixer. An integrated RF buffer amplifier improves LO-RF isolation and eliminates the need for precision external bias resistors.

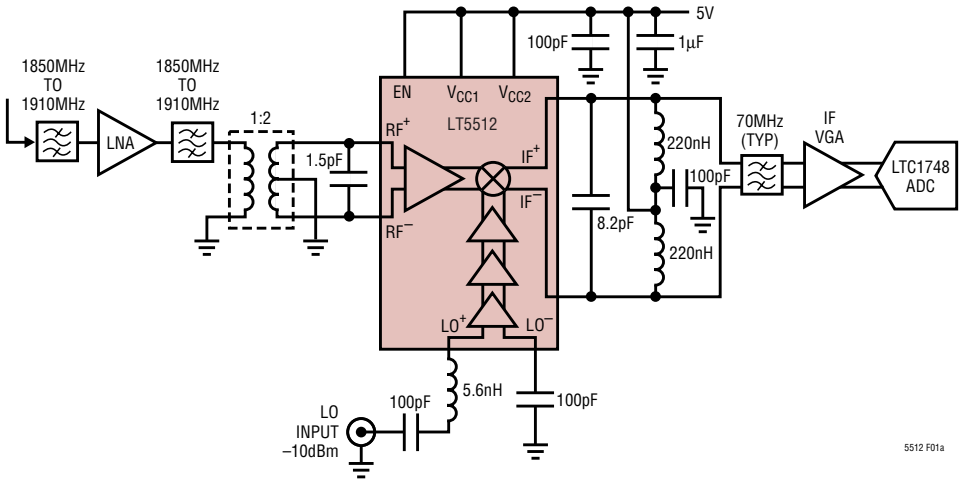
The LT5512 is a high-linearity alternative to passive diode mixers. Unlike passive mixers, which have conversion loss and require high LO drive levels, the LT5512 delivers conversion gain and requires significantly lower LO drive levels.

APPLICATIONS

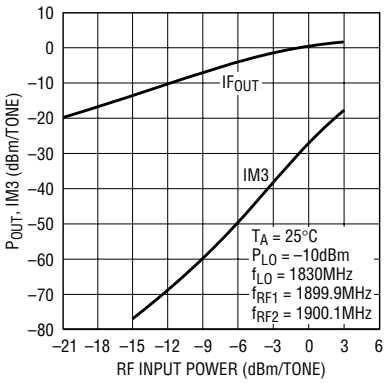
- Cellular/PCS/UMTS Infrastructure
- CATV Downlink Infrastructure
- High Linearity Mixer Applications
- ISM Band Receivers

TYPICAL APPLICATION

High Signal-Level Downmixer for Wireless Infastructure



Output IF Power and Output IM3 vs RF Input Power (Two Input Tones)

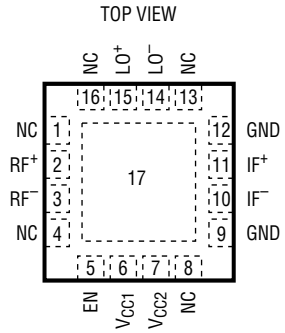


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 5.5V
Enable Voltage ..... –0.3V to V_{CC} + 0.3V
LO^+ to LO^- Differential Voltage ..... ±1.5V
..... (+6dBm equivalent)
RF^+ to RF^- Differential Voltage ..... ±0.7V
..... (+10dBm equivalent)
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–65°C to 125°C
Junction Temperature (T_J) ..... 125°C

PACKAGE/ORDER INFORMATION



UF PACKAGE
16-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD IS GROUND (PIN 17)
(MUST BE SOLDERED TO PCB)

ORDER PART NUMBER
LT5512EUF
PART MARKING
5512

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Input Frequency Range[2]	Requires Appropriate Matching		0.001 to 3000		MHz
LO Input Frequency Range[2]	Requires Appropriate Matching		0.001 to 3000		MHz
IF Output Frequency Range[2]	Requires Appropriate Matching		0.001 to 2000		MHz

Downmixer Application: (Test Circuit Shown in Figure 2) V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, P_{RF} = –10dBm (–10dBm/tone for two-tone IIP3 tests, Δf = 200kHz), f_{LO} = f_{RF} – 170MHz, P_{LO} = –10dBm, IF output measured at 170MHz, unless otherwise noted. (Notes 2, 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	f_{RF} = 900MHz f_{RF} = 1900MHz	 –1	0 1		dB dB
Conversion Gain vs Temperature	T_A = –40°C to 85°C		–0.011		dB/°C
Input 3rd Order Intercept	f_{RF} = 900MHz f_{RF} = 1900MHz		21 17		dBm dBm
Single-Sideband Noise Figure	f_{RF} = 900MHz f_{RF} = 1900MHz		11 14		dB dB
LO to RF Leakage	f_{LO} = 730MHz f_{LO} = 1730MHz		–60 –53		dBm dBm
LO to IF Leakage	f_{LO} = 730MHz and 1730MHz		–46		dBm
RF to LO Isolation	f_{RF} = 900MHz f_{RF} = 1900MHz		57 50		dB dB
2RF-2LO Output Spurious Product (f_{RF} = f_{LO} + $f_{IF/2}$)	900MHz: f_{RF} = 815MHz at –12dBm 1900MHz: f_{RF} = 1815MHz at –12dBm		–66 –59		dBc dBc
3RF-3LO Output Spurious Product (f_{RF} = f_{LO} + $f_{IF/3}$)	900MHz: f_{RF} = 786.67MHz at –12dBm 1900MHz: f_{RF} = 1786.67MHz at –12dBm		–83 –58		dBc dBc
Input 1dB Compression	f_{RF} = 900MHz f_{RF} = 1900MHz		10.1 6.2		dBm dBm

ELECTRICAL CHARACTERISTICS

1230MHz Cable Infrastructure Downmixer Application: (Test Circuit Shown in Figure 3) V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, RF input = 1230MHz at –10dBm, LO input swept from 1500MHz to 2100MHz, P_{LO} = –10dBm, IF output measured from 270MHz to 870MHz, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	f_{LO} = 1800MHz, f_{IF} = 570MHz		2.8		dB
Input 3rd Order Intercept	2-Tone RF Input, –10dBm/Tone, Δf = 1MHz, f_{LO} = 1800MHz, f_{IF} = 570MHz		17.9		dBm
LO to RF Leakage			–56		dBm
LO to IF Leakage			–40		dBm
RF to LO Isolation			51		dB
2RF – LO Output Spurious Product	f_{IF} = 570MHz, P_{RF} = –18dBm, f_{LO} = 1800MHz		–60		dBc
Single-Sideband Noise Figure	f_{LO} = 1800MHz, f_{IF} = 570MHz		13.3		dB

DC ELECTRICAL CHARACTERISTICS

(Test Circuit Shown in Figure 2) V_{CC} = 5V_{DC}, EN = High, T_A = 25°C (Note 3), unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Enable (EN) Low = Off, High = On					
Turn On Time			3		µs
Turn Off Time			13		µs
Input Current	V_{ENABLE} = 5V_{DC}		50		µA
Enable = High (On)		3			V_{DC}
Enable = Low (Off)				0.3	V_{DC}
Power Supply Requirements (V_{CC})					
Supply Voltage		4.50		5.25	V_{DC}
Supply Current			57	74	mA
Shutdown Current	EN = Low			100	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

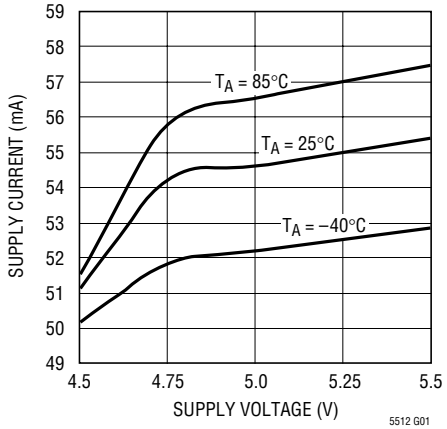
Note 2: External components on the final test circuit are optimized for operation at f_{RF} = 1900MHz, f_{LO} = 1730MHz and f_{IF} = 170MHz (Figure 2).

Note 3: Specifications over the –40°C to 85°C temperature range are assured by design, characterization and correlation with statistical process controls.

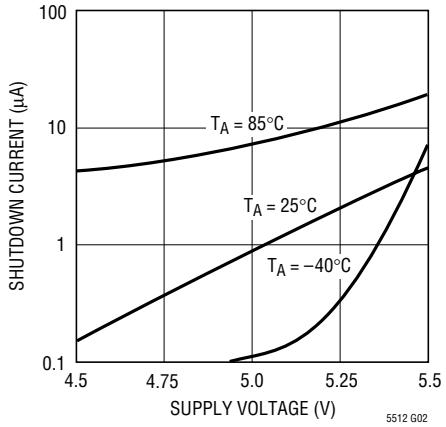
TYPICAL PERFORMANCE CHARACTERISTICS

(Test Circuit Shown in Figure 2)

Supply Current vs Supply Voltage



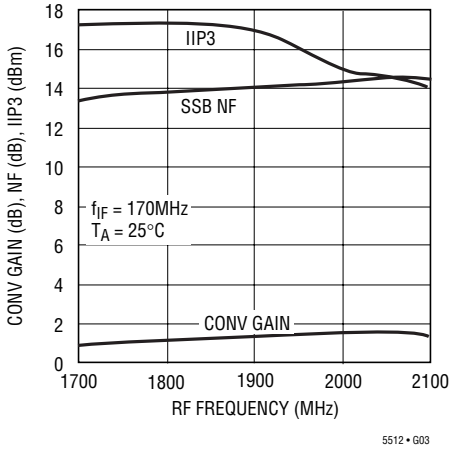
Shutdown Current vs Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (1900MHz Downmixer Application)

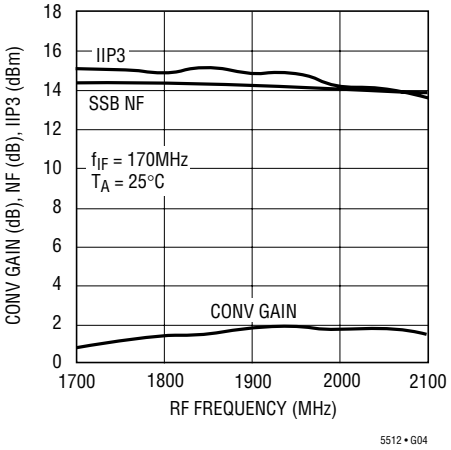
V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, 1900MHz RF input matching, RF input = 1900MHz at –10dBm, LO input = 1730MHz at –10dBm, IF output measured at 170MHz, unless otherwise noted. (Test circuit shown in Figure 2).

Conv Gain, IIP3 and SSB NF vs RF Frequency (Low-Side LO)



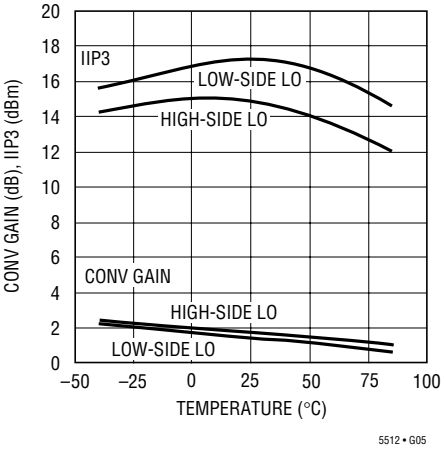
5512 • G03

Conv Gain, IIP3 and SSB NF vs RF Frequency (High-Side LO)



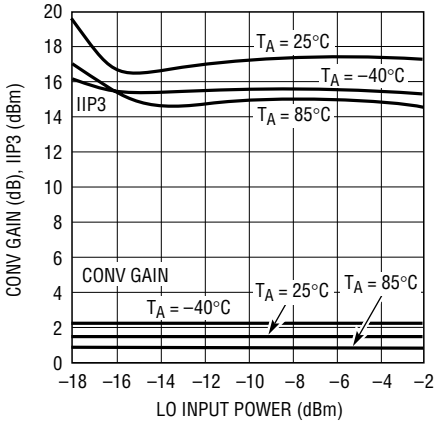
5512 • G04

Conv Gain and IIP3 vs Temperature RF = 1900MHz, IF = 170MHz



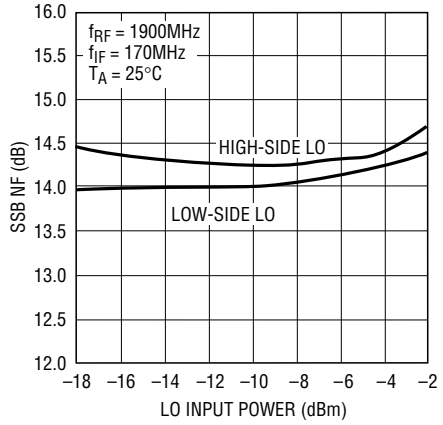
5512 • G05

Conv Gain and IIP3 vs LO Input Power



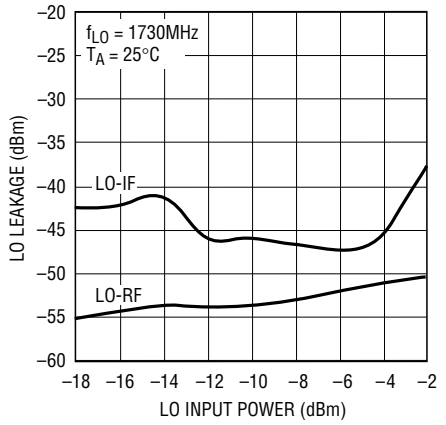
5512 • G06

SSB Noise Figure vs LO Input Power



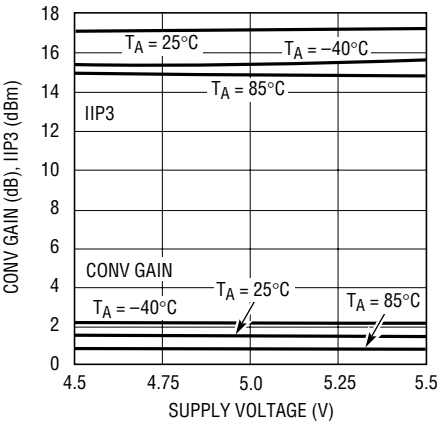
5512 • G07

LO-IF and LO-RF Leakage vs LO Input Power



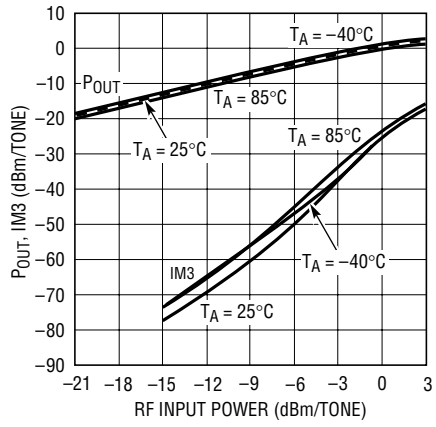
5512 • G08

Conv Gain and IIP3 vs Supply Voltage



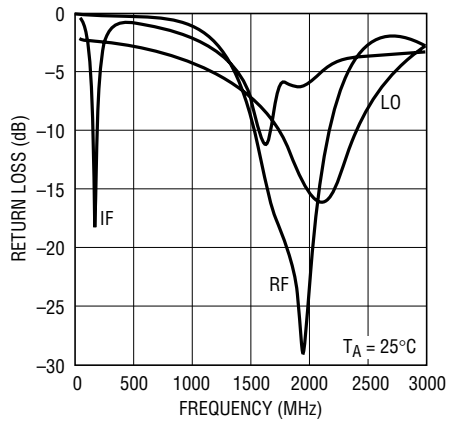
5512 • G09

Output IF Power and Output IM3 vs RF Input Power (Two Input Tones)



5512 G10

RF, LO and IF Port Return Loss vs Frequency

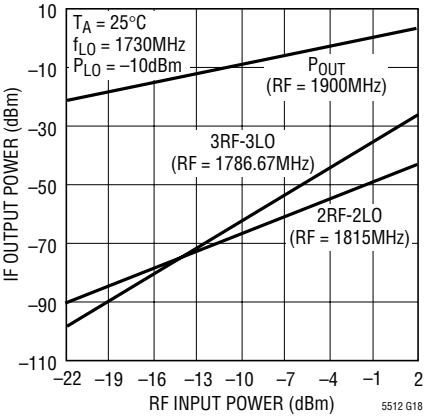


5512 G11

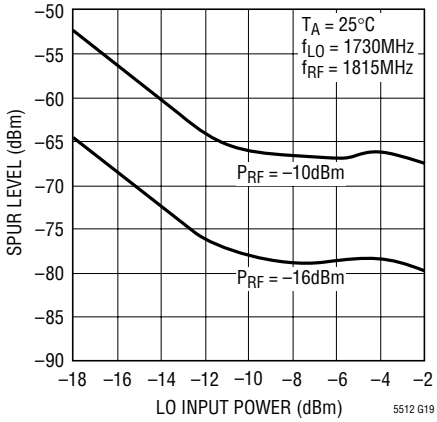
TYPICAL PERFORMANCE CHARACTERISTICS (1900MHz Downmixer Application, continued)

V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, 1900MHz RF input matching, RF input = 1900MHz at –10dBm, LO input = 1730MHz at –10dBm, IF output measured at 170MHz, unless otherwise noted. (Test circuit shown in Figure 2).

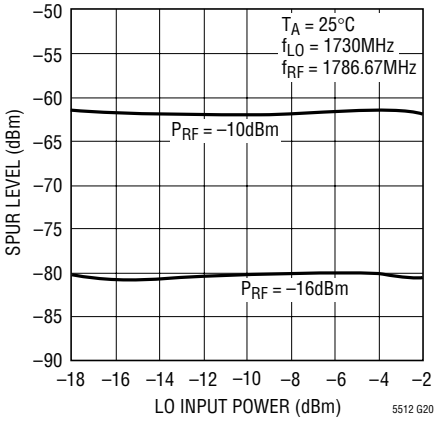
IF Output Power, 2RF-2LO and 3RF-3LO vs RF Input Power



2RF-2LO (Half-IF) Spur Level vs LO Input Power

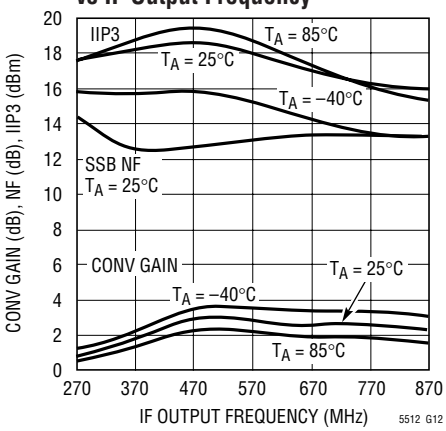


3RF-3LO Spur Level vs LO Input Power

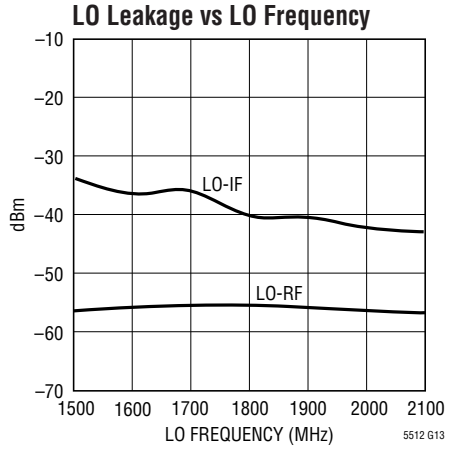


(1230MHz Cable Infrastructure Downmixer Application) V_{CC} = 5V_{DC}, EN = High, T_A = 25°C, RF input = 1230MHz at –10dBm, LO input swept from = 1500MHz to 2100MHz, P_{LO} = –10dBm, IF output measured from 270MHz to 870MHz, unless otherwise noted. (Test circuit shown in Figure 3.)

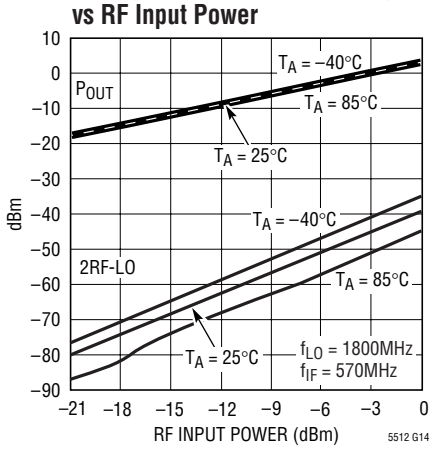
Conv Gain, IIP3 and SSB NF vs IF Output Frequency



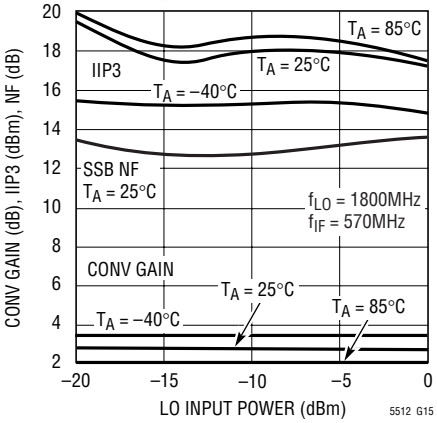
LO Leakage vs LO Frequency



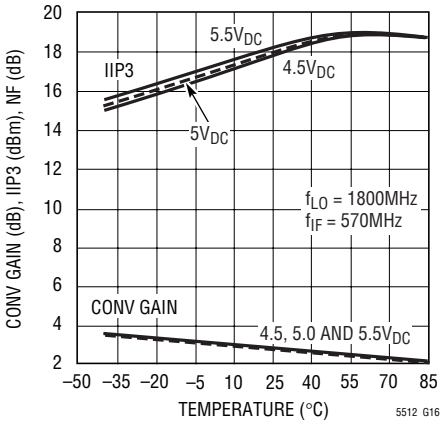
IF Output Power and 2RF-LO Spur vs RF Input Power



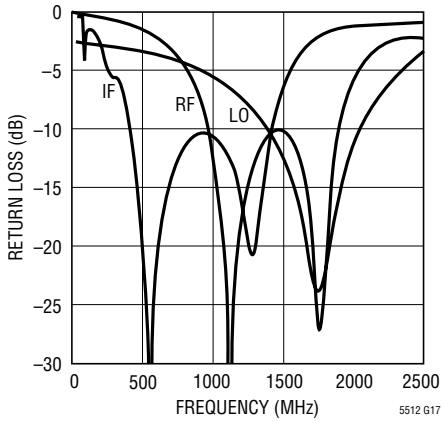
Conv Gain, IIP3 and SSB NF vs LO Input Power



Conv Gain and IIP3 vs Temperature



RF, LO and IF Port Return Losses vs Frequency



PIN FUNCTIONS

NC (Pins 1, 4, 8, 13, 16): Not connected internally. These pins should be grounded on the circuit board for improved LO to RF and LO to IF isolation.

RF⁺, RF⁻ (Pins 2, 3): Differential Inputs for the RF Signal. These pins must be driven with a differential signal. Each pin must be connected to a DC ground capable of sinking 15mA (30mA total). This DC bias return can be accomplished through the center-tap of a balun, or with shunt inductors. An impedance transformation is required to match the RF input to 50Ω (or 75Ω).

EN (Pin 5): Enable Pin. When the input voltage is higher than 3V, the mixer circuits supplied through Pins 6, 7, 10, and 11 are enabled. When the input voltage is less than 0.3V, all circuits are disabled. Typical enable pin input current is 50μA for EN = 5V and 0μA when EN = 0V.

V_{CC1} (Pin 6): Power Supply Pin for the LO Buffer Circuits. Typical current consumption is 22mA. This pin should be externally connected to the other V_{CC} pins, and decoupled with 100pF and 0.01μF capacitors.

V_{CC2} (Pin 7): Power Supply Pin for the Bias Circuits. Typical current consumption is 4mA. This pin should be externally connected to the other V_{CC} pins, and decoupled with 100pF and 0.01μF capacitors.

GND (Pins 9 and 12): Ground. These pins are internally connected to the backside ground for better isolation. They should be connected to RF ground on the circuit board, although they are not intended to replace the primary grounding through the backside contact of the package.

IF⁻, IF⁺ (Pins 10, 11): Differential Outputs for the IF Signal. An impedance transformation may be required to match the outputs. These pins must be connected to V_{CC} through impedance matching inductors, RF chokes or a transformer center-tap.

LO⁻, LO⁺ (Pins 14, 15): Differential Inputs for the Local Oscillator Signal. They can also be driven single-ended by connecting one to an RF ground through a DC blocking capacitor. These pins are internally biased to 2V; thus, DC blocking capacitors are required. An impedance transformation is required to match the LO input to 50Ω (or 75Ω).

GROUND (Pin 17) (Backside Contact): Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

BLOCK DIAGRAM

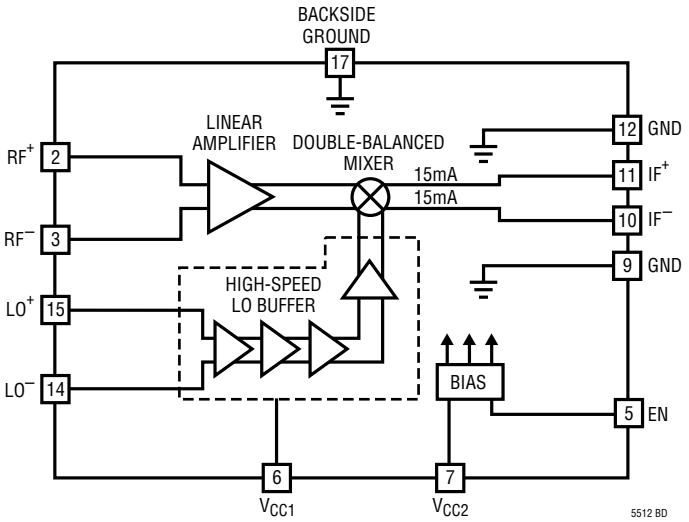
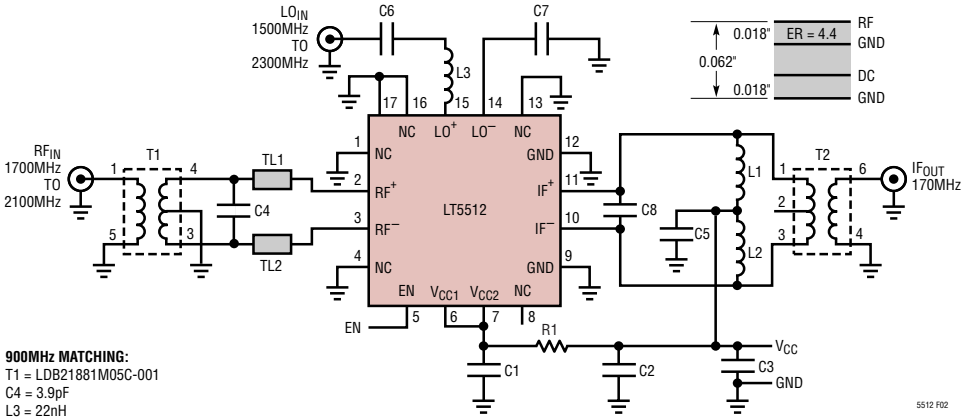


Figure 1.

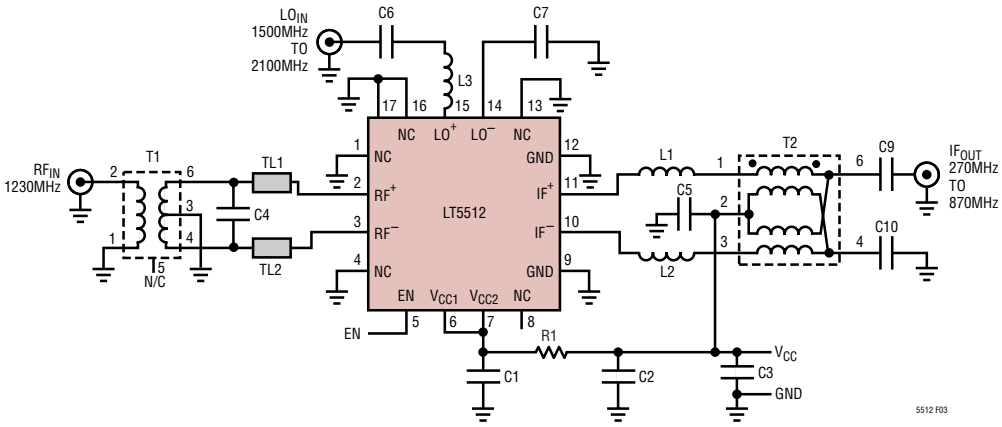
TEST CIRCUITS



900MHz MATCHING:
T1 = LDB21881M05C-001
C4 = 3.9pF
L3 = 22nH

REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C1, C5, C6, C7	100pF	0402	Murata GRP1555C1H101J	L1, L2	47nH	0402	Coilcraft 0402CS-47NX
C2	0.01µF	0402	Murata GRP155R71C103K	L3	5.6nH	0402	Toko LL1005-FH5N6
C3	1.0µF	0603	Taiyo Yuden LMK107F105ZA	R1	10	0402	
C4	1.5pF	0402	Murata GRP1555C1H1R5C	T1	2:1		Murata LDB211G9010C-001
C8	6.8pF	0402	Murata GRP1555C1H6R8D	T2	8:1		Mini-Circuits TC8-1
				TL1, TL2	Z_0 = 72Ω	θ = 8.1°	(W = 0.4mm, L = 2mm)

Figure 2. Test Schematic for 1900MHz Downconverter (PCS/UMTS Applications)



REF DES	VALUE	SIZE	PART NUMBER	REF DES	VALUE	SIZE	PART NUMBER
C1, C5, C6, C7, C9, C10	100pF	0402	Murata GRP1555C1H101J	L1, L2	12nH	0402	Toko LL1005-FH12N
				L3	8.2nH	0402	Toko LL1005-FH8N2
C2	0.01µF	0402	Murata GRP155R71C103K	R1	10	0402	
C3	1.0µF	0603	Taiyo Yuden LMK107F105ZA	T1	1:1		Murata LDB311G2705C-428
C4	2.7pF	0402	Murata GRP1555C1H2R7C	T2	4:1		M/A-COM ETC1.6-4-2-3
				TL1, TL2	Z_0 = 72Ω	θ = 5.4°	(W = 0.4mm, L = 2.0mm)

Figure 3. Test Schematic for 1230MHz Downconverter (Cable Infrastructure Downlink Transmitter Applications)

APPLICATIONS INFORMATION

The LT5512 consists of a double-balanced mixer, RF buffer amplifier, high-speed limiting LO buffer, and bias/enable circuits. The RF, LO and IF ports are differential. All three ports can be matched from 1kHz to 3GHz, although the IC has been optimized for downconverter applications where the RF and LO input signals are high frequency and the IF output frequency ranges from 1kHz up to 2GHz. Low side or high side LO injection can be used.

RF Input Port

The RF input buffer has been designed to simplify impedance matching while improving LO-RF isolation and noise figure. A simplified schematic is shown in Figure 4 with the associated external impedance matching elements for a 1.9GHz application. Each RF input requires a low resistance DC return to ground capable of sinking 15mA. This can be accomplished with the center-tap of a balun as shown in Figure 4, or bias chokes connected from Pins 2 and 3 to ground.

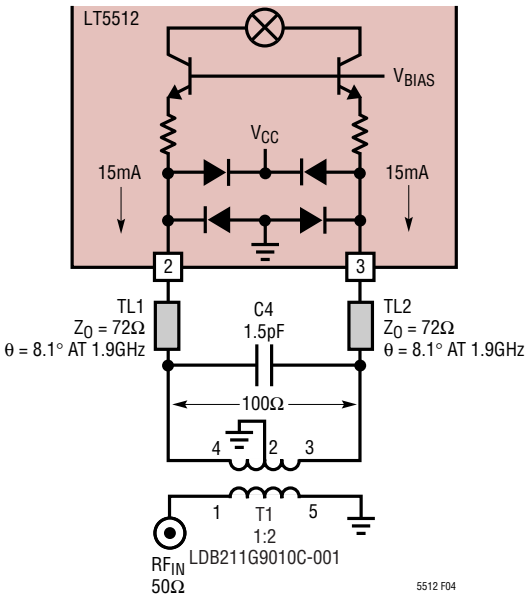


Figure 4. RF Input with External Matching for a 1.9GHz Application

Table 1 lists the differential input impedance and differential reflection coefficient between Pins 2 and 3 for several common RF frequencies. As shown in Figures 4 and 5, low-pass impedance matching is used to transform the differential input impedance up to the desired value for the balun input. The following example shows how to design the low-pass impedance transformation network for the RF input.

From Table 1, the differential input impedance at 1900MHz is 20.6 + j22.8. As shown in Figure 5, the 22.8Ω reactance is split, with one half on each side of the 20.6Ω load resistor. The matching network will consist of additional inductance in series with the internal inductance and a capacitor in parallel with the desired 100Ω source impedance. The capacitance (C4) and inductance are calculated as follows.

$n = R_S/R_L = 100/20.6 = 4.85$

$Q = \sqrt{n-1} = 1.963$

$X_C = R_S/Q = 100/1.963 = 50.9\Omega$

$C4 = 1/(\omega Xc) = 1.6pF$ (use 1.5pF)

$X_L = (R_L \bullet Q) = (20.6 \bullet 1.963) = 40.4\Omega$

$X_{EXT} = X_L - X_{INT} = 40.4 - 22.8 = 17.6\Omega$

$L_{EXT} = (X_{EXT}/\omega) = 1.47nH$

The external inductance is split in half (0.74nH), with each half connected between the pin and the shunt capacitor, as shown in Figure 5. The inductance is implemented with short (2mm) high-impedance printed transmission lines, which yield a compact board layout. Finally, the 2:1balun transforms the 100Ω differential impedance down to a 50Ω single-ended input for the RF signal.

Table 1. RF Input Differential Impedance

Frequency (MHz)	Differential Input Impedance	Differential S11	
		Mag	Angle
10	18.2 + j0.14	0.467	179.6
44	18.0 + j0.26	0.470	178.6
240	18.1 + j2.8	0.471	172.6
450	18.1 + j5.2	0.473	166.3
950	18.7 + j11.3	0.479	150.8
1900	20.6 + j22.8	0.503	124.3
2150	21.4 + j26.5	0.512	116.9
2450	22.5 + j30.5	0.522	109.2
2700	24.1 + j34.7	0.530	101.7

APPLICATIONS INFORMATION

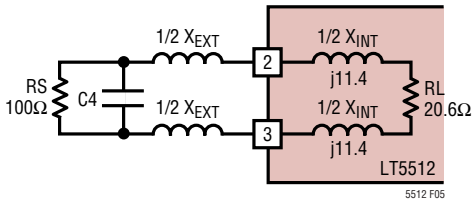


Figure 5. 1.9GHz RF Input Matching

It is also possible to eliminate the RF balun and drive the RF inputs differentially. In this case, inductors from Pins 2 and 3 to ground would be required to bias the input stage. The value of the inductors should be high enough to avoid reducing the input impedance at the frequency of interest.

LO Input Port

The LO buffer amplifier consists of high-speed limiting differential amplifiers, designed to drive the mixer quad for high linearity. The LO+ and LO– pins are designed for differential or single-ended drive. An external balun is optional. Both LO pins are internally biased to $2V_{DC}$.

The LO input has been designed for simple impedance matching for frequencies up to 3GHz. A simplified schematic is shown in Figure 6 with the associated external impedance matching. The matching technique is similar to that described earlier for the RF port, except the match is not nearly as critical. Table 2 lists the differential input impedance and differential reflection coefficient between the LO+ and LO– pins (Pin 15 to Pin 14). As shown, the real part of the series impedance is close to 100Ω. Series inductors (L3, L4) are used to tune out the capacitive portion of the differential impedance.

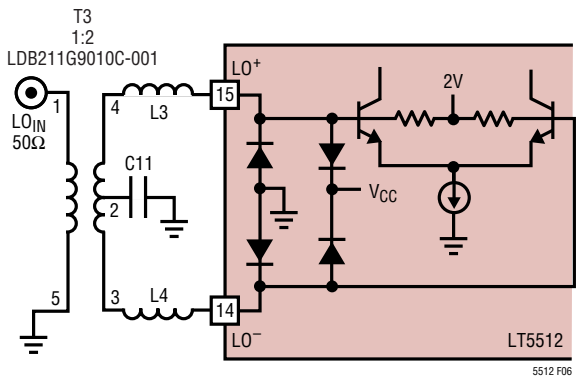


Figure 6. LO Input with External Matching Elements

Table 2. LO Input Differential Impedance

Frequency (MHz)	Differential Input Impedance	Differential S11	
		Mag	Angle
750	263 – j172	0.766	–10.2
1000	213 – j178	0.760	–13.4
1250	175 – j173	0.752	–16.6
1500	146 – j164	0.743	–19.8
1750	125 – j153	0.733	–22.8
2000	108 – j142	0.722	–25.8
2250	95 – j131	0.709	–28.9
2500	86 – j122	0.695	–31.8
2750	78 – j113	0.68	–34.6

Single-ended LO drive can be used if a differential LO source is not available, or the added expense of a LO balun is undesirable. In this case, one LO input is AC-coupled to ground through a 100pf DC blocking capacitor as shown in Figure 7. The other input is matched to 50Ω using a series inductor and a second DC blocking capacitor. The LT5512 is characterized and production tested with single-ended LO drive.

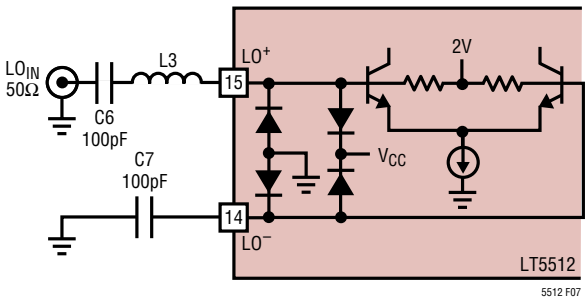


Figure 7. Single-Ended LO Input Matching

The differential port impedance listed in Table 2 can be used to compute the value of the series matching inductor, L3. Alternatively, Figure 8 shows measured LO input return loss for various values of L3.

APPLICATIONS INFORMATION

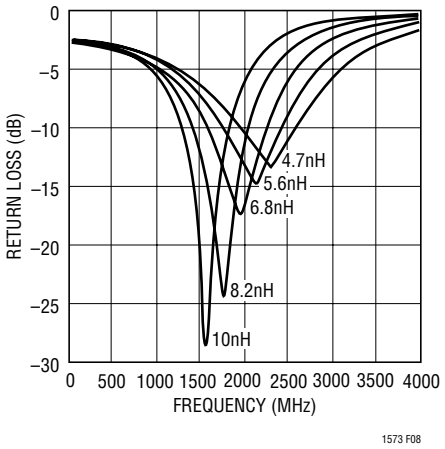


Figure 8. Single-Ended LO Port Return Loss vs Frequency for Various Values of L3

IF Output Port

The IF outputs, IF+ and IF–, are internally connected to the collectors of the mixer switching transistors as shown in Figure 9. These differential outputs should be combined externally through an RF balun or 180° hybrid to achieve optimum performance. Both pins must be biased at the supply voltage, which can be applied through matching inductors (see Figure 2), or through the center-tap of an output transformer (see Figure 3). These pins are protected with ESD diodes; the diodes allow peak AC signal swing up to 1.3V above V_{CC}.

As shown in Table 3, the IF output differential impedance is approximately 390Ω in parallel with 0.44pF. A simple band-pass IF matching network suitable for wireless applications is shown in Figure 9. Here, L1, L2 and C8 set the desired IF output frequency. The 390Ω differential output can then be applied directly to a differential filter, or an 8:1 balun for impedance transformation down to 50Ω. To achieve maximum linearity, C8 should be located as close as possible to the IF+/IF– pins. Even small amounts of inductance in series with C8 (such as through a via) can significantly degrade IIP3. For high IF frequencies, the value of C8 should be reduced by the value of internal capacitance (see Table 3).This matching network is simple and offers good selectivity for narrow band IF applications.

An alternative matching network for a broadband CATV IF (270MHz to 870MHz) is shown in Figure 3. Here, a low-pass impedance transformer consisting of the internal capacitance, with L1 and L2, transforms the 371Ω output resistance at 870MHz to 200Ω. A 4:1 balun then completes the match down to 50Ω. Supply voltage is applied through the center-tap of the transformer.

Table 3. IF Output Differential Impedance (Parallel Equivalent)

Frequency	Differential Output	Differential S11	
(MHz)	Impedance	Mag	Angle
10	396 II – j10k	0.766	0
70	394 II – j5445	0.775	–1.1
170	393 II – j2112	0.774	–2.8
240	392 II – j1507	0.773	–3.9
450	387 II – j798	0.772	–7.3
750	377 II – j478	0.768	–12.2
860	371 II – j416	0.766	–14.0
1000	363 II – j359	0.762	–16.2
1250	363 II – j295	0.764	–19.6
1500	346 II – j244	0.756	–23.6
1900	317 II – j192	0.743	–29.9

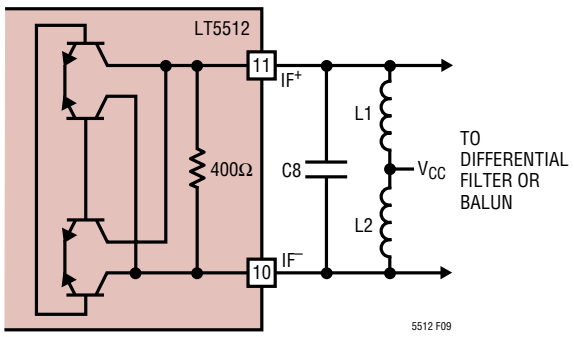
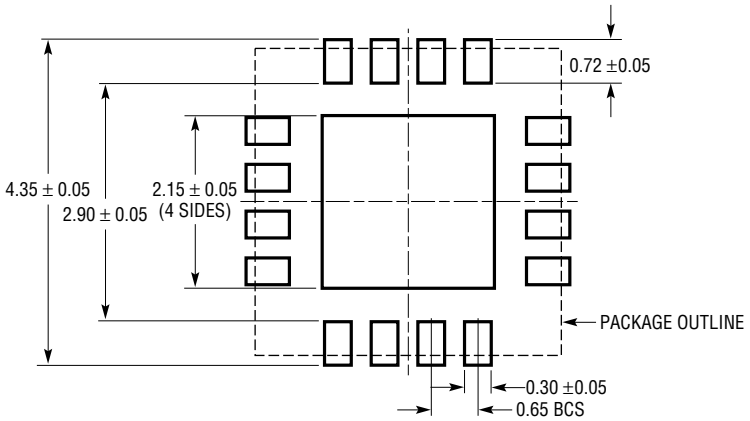


Figure 9. IF Output Equivalent Circuit with Band-Pass Matching Elements

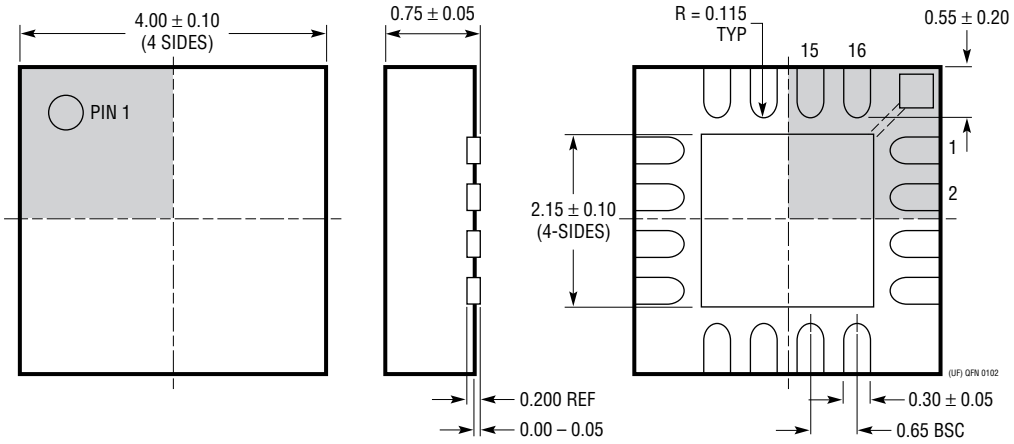
PACKAGE DESCRIPTION

UF16 Package
16-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1692)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGC)
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
4. EXPOSED PAD SHALL BE SOLDER PLATED

APPLICATIONS INFORMATION

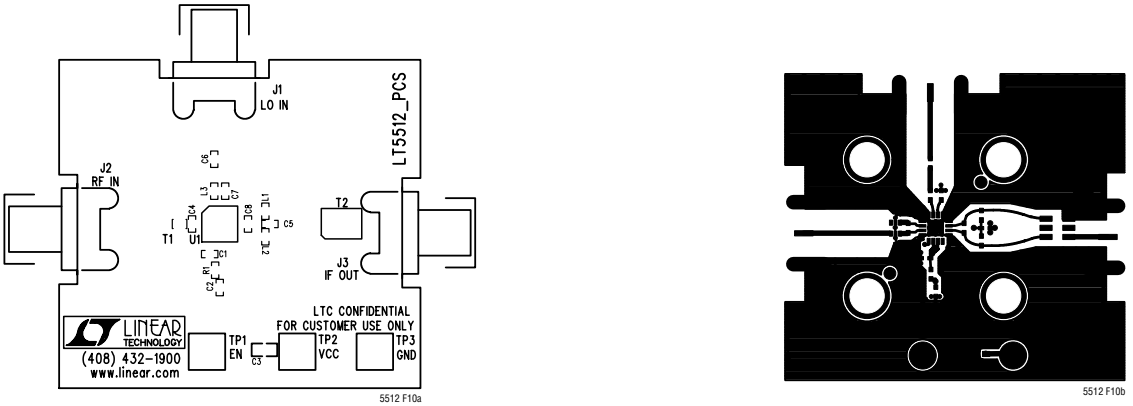


Figure 10. 1900MHz Evaluation Board Layout

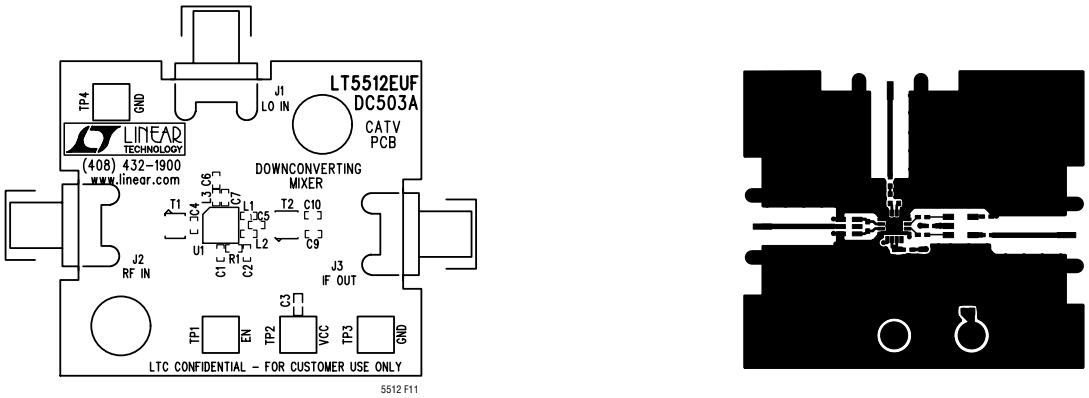


Figure 11. 1230MHz Cable Infrastructure Evaluation Board Layout (Wide Output Range Down-Converting Mixer for Downlink Transmitter)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT5502	400MHz Quadrature Demodulator with RSSI	1.8V to 5.25V Supply, 70MHz to 400MHz IF, 84dB Limiting Gain, 90db RSSI Range
LT5504	800MHz to 2.7GHz RF Measuring Receiver	80dB Dynamic Range, Temperature Compensated, 2.7V to 5.5V Supply
LTC5505	300MHz to 3.5GHz RF Power Detector	>40dB Dynamic Range, Temperature Compensated, 2.7V to 6V Supply
LT5506	500MHz Quadrature IF Demodulator with VGA	1.8V to 5.25V Supply, 40MHz to 500MHz IF, –4dB to 57dB Linear Power Gain
LTC5507	100kHz to 1GHz RF Power Detector	48dB Dynamic Range, Temperature Compensated, 2.7V to 6V Supply
LTC5508	300MHz to 7GHz RF Power Detector	44dB Dynamic Range, Temperature Compensated, SC70 Package
LTC5509	300MHz to 3GHz RF Power Detector	36dB Dynamic Range, SC70 Package
LT5511	High Signal Level Up Converting Mixer	RF Output to 3GHz, 17dBm IIP3, Integrated LO Buffer
LT5515	1.5GHz to 2.5GHz Direct Conversion Quadrature Demodulator	20dBm IIP3, Integrated LO Quadrature Generator
LT5516	0.8GHz to 1.5GHz Direct Conversion Quadrature Demodulator	21.5dBm IIP3, Integrated LO Quadrature Generator
LT5522	600MHz to 2.7GHz Down Converting Mixer	25dBm IIP3, 50Ω Single-Ended RF and LO Ports
LTC5532	300MHz to 7GHz Precision RF Power Detector	Precision V_{OUT} Offset Control, Adjustable Gain and Offset Voltage

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