



LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT6211C

HDMI1.4 to Dual-port LVDS with Audio

Datasheet



1. Features

● HDMI1.4 Receiver

- Compliant with the HDMI 1.4 specification with TMDS data rates up to 3.4Gbps per channel
- Support HDCP 1.4
- Adaptive receiver Equalization for PCB, cable and connector losses

● Single/Dual-Port LVDS Transmitter

- Compatible with VESA and JEIDA standard
- 1/2 Configurable Port
- 1 clock lane and 4 configurable data lanes per port
- Data Lane and Polarity Swapping
- Support Maximum Data Rate 1.2Gb/s/lane
- Output Color Depth supports 6-bit and 8-bit
- Video stream copy mode for each dual-port
- Side-by-side 3D support

● Miscellaneous

- 3.3V/1.2V Supply Power
- Internal CSC support conversions between YCbCr 4:4:4 and RGB, and between YCbCr 4:2:2 and YCbCr 4:4:4
- Support SPDIF and 2-channel IIS audio output

- Support 100KHz and 400KHz I2C slave
- Power from phone or adapter mode selection
- Integrated Microprocessor
- Embedded EDID shadow.
- Temperature Range: -40°C ~ +85°C
- ESD 4kV HBM

2. Description

The LT6211C is a high performance HDMI1.4 to LVDS chip for VR/Display application.

For LVDS output, LT6211C can be configured as single-port or dual-port. For 2D video stream, the same video stream can be mapped to two separated panel, for 3D video format, left side data can be sent to one panel, and right side data can be sent to another panel.

This package is BGA144 7mmx7mm. It operate from -40°C to +85°C.

3. Applications

- Docking Station
- Display
- VR

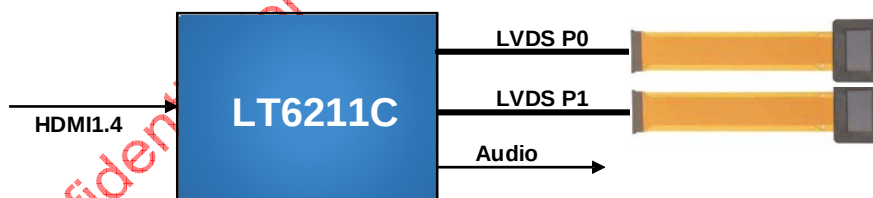


Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT6211C	-40°C to +85°C	QFN64 (7.5*7.5)	Tray

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5. Revision History

Version	Owner	Content	Date
R1.0	XF CH	Initial data sheet creation	03/09/2017
R1.1	N W	Update package information	03/28/2017
R1.2	Terry	Update pin and package information	05/23/2017
R1.3	Terry	Update about LVDS Transmitter AC Specifications information	06/13/2017
R1.4	Terry	Update about pin and features information	07/11/2017
	N W	Update package information	11/14/2018
R1.5	PP J	Update Figure 6.1.1	07/17/2019



6. Pinning Information

6.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with $100\Omega \pm 10\%$ differential impedance. Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

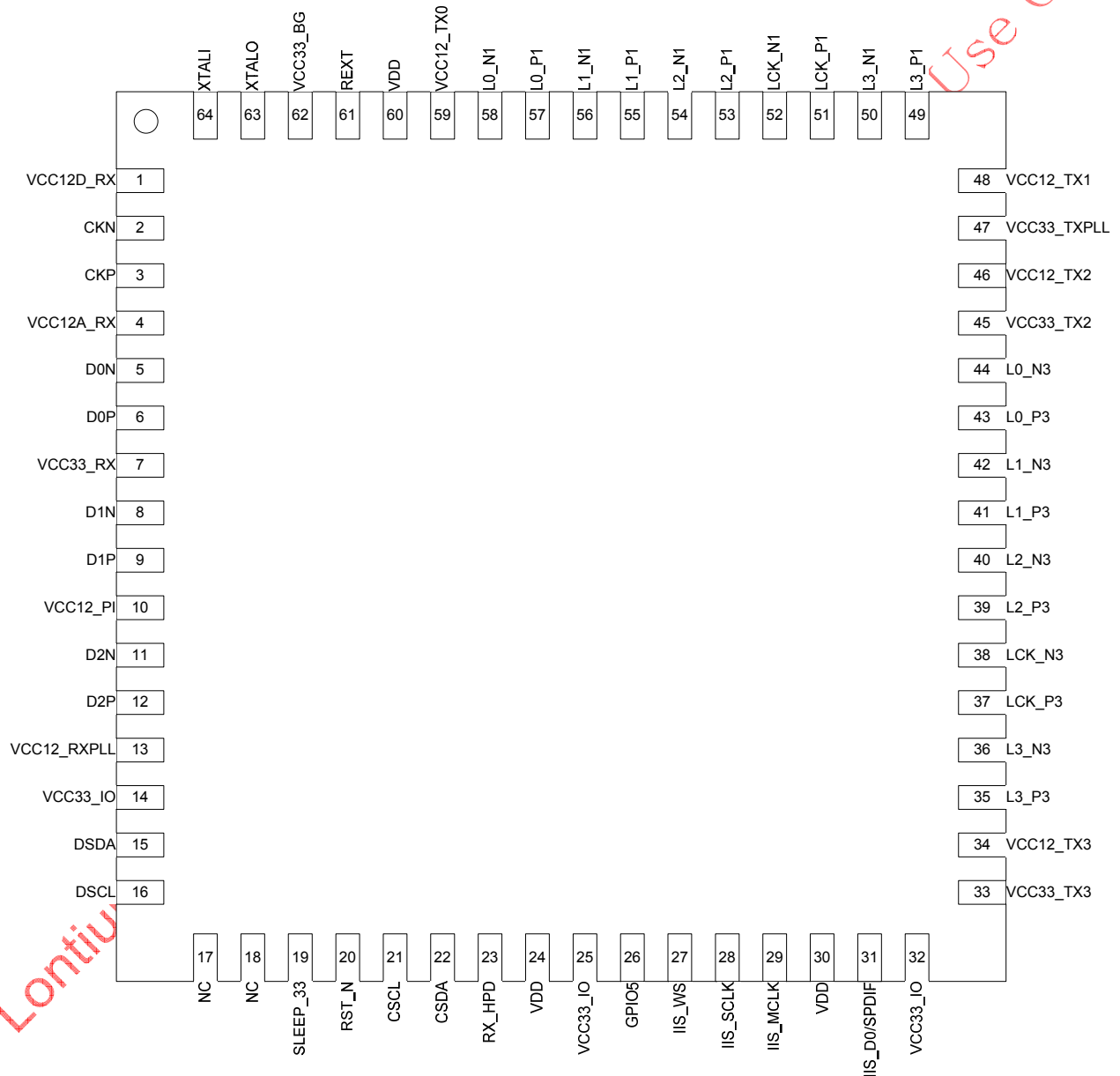


Figure 6.1.1 LT6211C (QFN64) Pin Assignment (Top View)

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To minimize the power supply noise floor, at least one 0.1 μ F and one 0.01 μ F decoupling capacitors recommended to be installed near all the LT6211C power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized.

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6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
65	VSS	PG	I/O	Ground(EPAD)
14,25,32	VCC33_IO	PG	I/O	3.3V IO Power
62	VCC33_BG	PG	I/O	3.3V Power for BG
7	VCC33_RX	PG	I/O	3.3V Power for RX
45	VCC33_TX2	PG	I/O	3.3V Power for LVDS TX Port2
33	VCC33_TX3	PG	I/O	3.3V Power for LVDS TX Port3
47	VCC33_TXPLL	PG	I/O	3.3V Power for TXPLL
24,30,60	VDD	PG	I/O	1.2V Core Power
10	VCC12_PI	PG	I/O	1.2V Power for PI
13	VCC12_RXPLL	PG	I/O	1.2V Power for RXPLL
4	VCC12A_RX	PG	I/O	1.2V Power for RX Analog Part
1	VCC12D_RX	PG	I/O	1.2V Power for RX Digital Part
59	VCC12_TX0	PG	I/O	1.2V Power for LVDS TX Port0
48	VCC12_TX1	PG	I/O	1.2V Power for LVDS TX Port1
46	VCC12_TX2	PG	I/O	1.2V Power for LVDS TX Port2
34	VCC12_TX3	PG	I/O	1.2V Power for LVDS TX Port3
11	D2N	Analog	I	RX Data Channel Lane-2 Negative Input Maximum data rate is 3.4Gbps.
12	D2P	Analog	I	RX Data Channel Lane-2 Positive Input Maximum data rate is 3.4Gbps.
8	D1N	Analog	I	RX Data Channel Lane-1 Negative Input Maximum data rate is 3.4Gbps.
9	D1P	Analog	I	RX Data Channel Lane-1 Positive Input Maximum data rate is 3.4Gbps.
5	D0N	Analog	I	RX Data Channel Lane-0 Negative Input Maximum data rate is 3.4Gbps.
6	D0P	Analog	I	RX Data Channel Lane-0 Positive Input Maximum data rate is 3.4Gbps.
2	CKN	Analog	I	RX Clock Channel Negative Input Maximum clock rate is 340MHz.
3	CKP	Analog	I	RX Clock Channel Positive Input Maximum clock rate is 340MHz.
17	NC	Analog	I/O	Connect 100k Ohm to GND
18	NC	Analog	I/P	Connect 100k Ohm to GND
64	XTALI	Analog	I/O	XTAI for Debug
63	XTALO	Analog	I/O	XTAO for Debug
57	L0_P1	Analog	O	LVDS TX Port1/Lane0 Channel Positive Input Maximum data rate is 1.2Gbps.
58	L0_N1	Analog	O	LVDS TX Port1/Lane0 Channel Negative Input Maximum data rate is 1.2Gbps.
55	L1_P1	Analog	O	LVDS TX Port1/Lane1 Channel Positive Input Maximum data rate is 1.2Gbps.
56	L1_N1	Analog	O	LVDS TX Port1/Lane1 Channel Negative Input Maximum data rate is 1.2Gbps.
53	L2_P1	Analog	O	LVDS TX Port1/Lane2 Channel Positive Input

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Pin#	Pin Name	I/O Type	I/O Dir	Description
				Maximum data rate is 1.2Gbps.
54	L2_N1	Analog	O	LVDS TX Port1/Lane2 Channel Negative Input Maximum data rate is 1.2Gbps.
51	LCK_P1	Analog	O	LVDS TX Port1/Clock Channel Positive Input Maximum Frequency is 171MHz.
52	LCK_N1	Analog	O	LVDS TX Port1/Clock Channel Negative Input Maximum Frequency is 171MHz.
49	L3_P1	Analog	O	LVDS TX Port1/Lane3 Channel Positive Input Maximum data rate is 1.2Gbps.
50	L3_N1	Analog	O	LVDS TX Port1/Lane3 Channel Negative Input Maximum data rate is 1.2Gbps.
43	L0_P3	Analog	O	LVDS TX Port3/Lane0 Channel Positive Input Maximum data rate is 1.2Gbps.
44	L0_N3	Analog	O	LVDS TX Port3/Lane0 Channel Negative Input Maximum data rate is 1.2Gbps.
41	L1_P3	Analog	O	LVDS TX Port3/Lane1 Channel Positive Input Maximum data rate is 1.2Gbps.
42	L1_N3	Analog	O	LVDS TX Port3/Lane1 Channel Negative Input Maximum data rate is 1.2Gbps.
39	L2_P3	Analog	O	LVDS TX Port3/Lane2 Channel Positive Input Maximum data rate is 1.2Gbps.
40	L2_N3	Analog	O	LVDS TX Port3/Lane2 Channel Negative Input Maximum data rate is 1.2Gbps.
37	LCK_P3	Analog	O	LVDS TX Port3/Clock Channel Positive Input Maximum Frequency is 171MHz.
38	LCK_N3	Analog	O	LVDS TX Port3/Clock Channel Negative Input Maximum Frequency is 171MHz.
35	L3_P3	Analog	O	LVDS TX Port3/Lane3 Channel Positive Input Maximum data rate is 1.2Gbps.
36	L3_N3	Analog	O	LVDS TX Port3/Lane3 Channel Negative Input Maximum data rate is 1.2Gbps.
15	DSDA	Schmitt, OD	I/O	Slave I2C SDA Signal For EDID
16	D_SCL	Schmitt, OD	I	Slave I2C SCL Signal For EDID
23	RX_HPD	OD	O	Hot Plug Signal
28	IIS_SCLK	LVTTL	I/O	SCLK of IIS
31	IIS_D0/SPDIF	LVTTL	I/O	D0/SPDIF of IIS
26	GPIO5	LVTTL	I/O	GPIO
27	IIS_WS	LVTTL	I/O	WS of IIS
20	RSTN	Schmitt	I	External Reset Signal, Low is Reset.
29	IIS_MCLK	LVTTL	I/O	MCLK of IIS
19	SLEEP_33	Schmitt	I	External Sleep Mode Control Signal
22	CSDA	Schmitt, OD	I/O	Slave I2C SDA Signal For Program Register
21	CSCL	Schmitt, OD	I	Slave I2C SCL Signal For Program Register
61	REXT	Analog	O	External 7.68Kohm Resistor For BG

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7. Function Description

7.1 Function Block Diagram

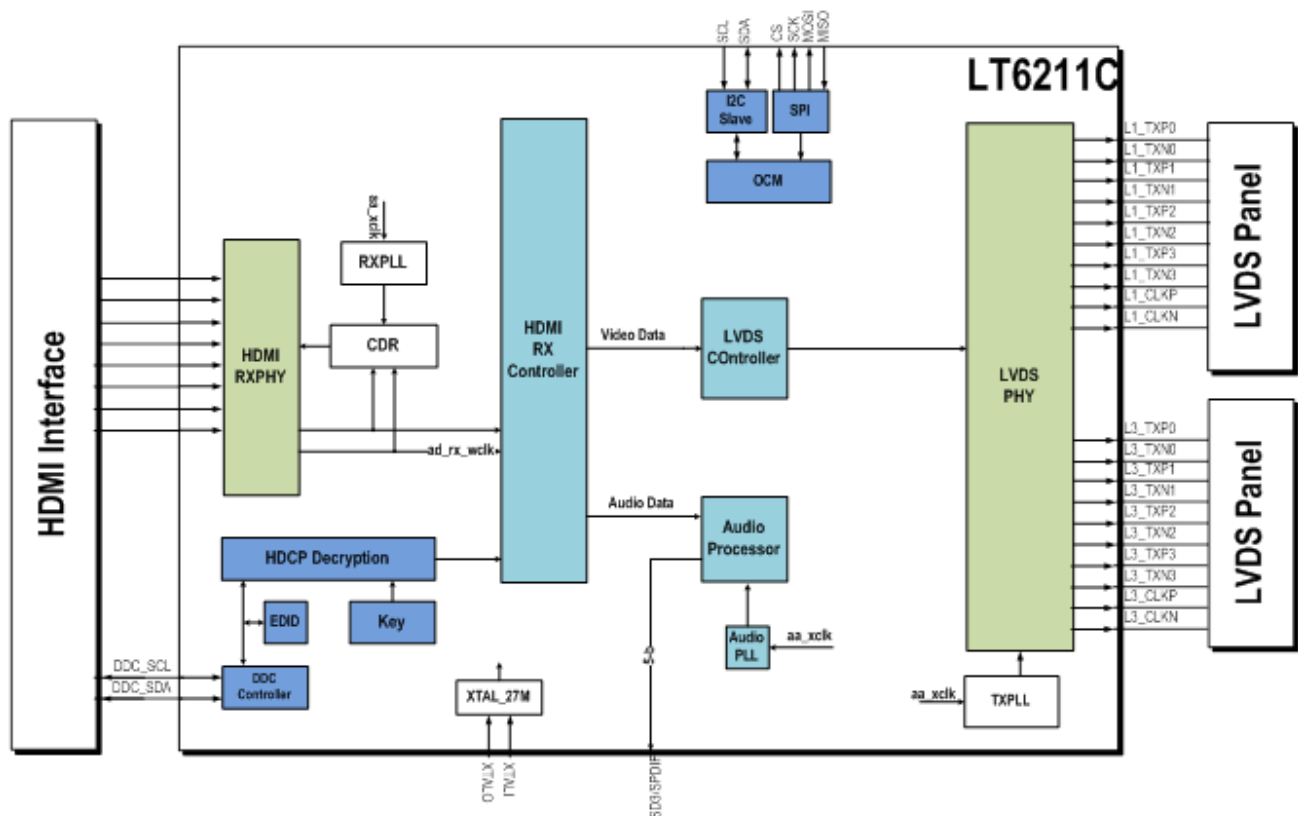


Figure 7.1.1 Function Block Diagram



8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VC C33_BG, VCC33_TXPLL VCC33_RX	3.3V Power Supply Voltage	-0.3		3.63	V
VDD,VCC12_TX0,VCC12_TX 1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VC C12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	-0.3		1.32	V
V _I	CMOS Terminal Input Voltage Range	-0.3		3.63	V
V _O	CMOS Terminal Output Voltage Range	-0.3		3.63	V
T _s	Storage Temperature	-40		125	°C
ESD	HBM Elastostatic Discharge Level		4000		V

Notes:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VC C33_BG, VCC33_TXPLL, VCC33_RX	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VDD,VCC12_TX0,VCC12_TX 1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VC C12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	1.08		1.32	V
VCC _N	Power Supply Voltage Noise			50	mV
T _A	Operating Free-air Temperature	-40	27	85	°C

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

TMDS RX DC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
V _{diff}	Differential input voltage level	150		1200	mV
V _{cm}	Input common mode voltage	AVCC- 400		AVCC- 37.5	mV

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Rterm	Single-ended termination resistance	45	50	55	Ω
LVDS Transmitter DC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
Voh	Output voltage high			1475	mV
Vol	Output voltage low	925			mV
Vod	Output differential voltage	250		400	mV
Vos	Output offset voltage	1125		1275	mV

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

TMDS RX AC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
Vs	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_intra_skew	Intra-pair skew at sink connector			0.15T+112	ps
T_inter_skew	Inter-pair skew at sink connector			0.2Tch aractor +1.78	ns
Tjitter	TMDS clock jitter			0.3Tbit	ps
LVDS Transmitter AC Specifications					
Symbol	Parameter	Min	Typ	Max	Unit
D-Clock	Clock duty cycle	45		55	%
T_intra_skew	Intra-pair skew			50	ps
T_inter_skew	Inter-pair skew			100	ps
Trise	Vod rise time, 20% to 80%	300		500	ps
Tfall	Vod fall time, 20% to 80%	300		500	ps

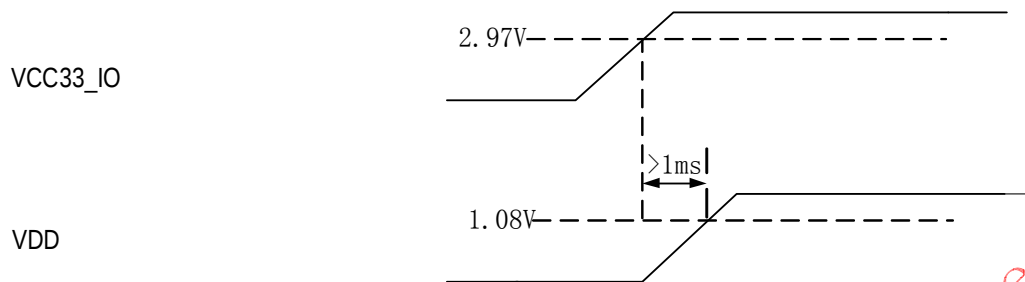
8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
4Kx2K@30Hz	80	350	mA
1080P	TBD	TBD	mA



8.6 Power-up and Reset Sequence



Note: 1.2V power should be set up at least 1ms later than 3.3V power, the reset signal should be released after 1.2V power is ready.

Figure 8.6.1 Power-up and Reset Sequence



9. Package Information

The LT6211C is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

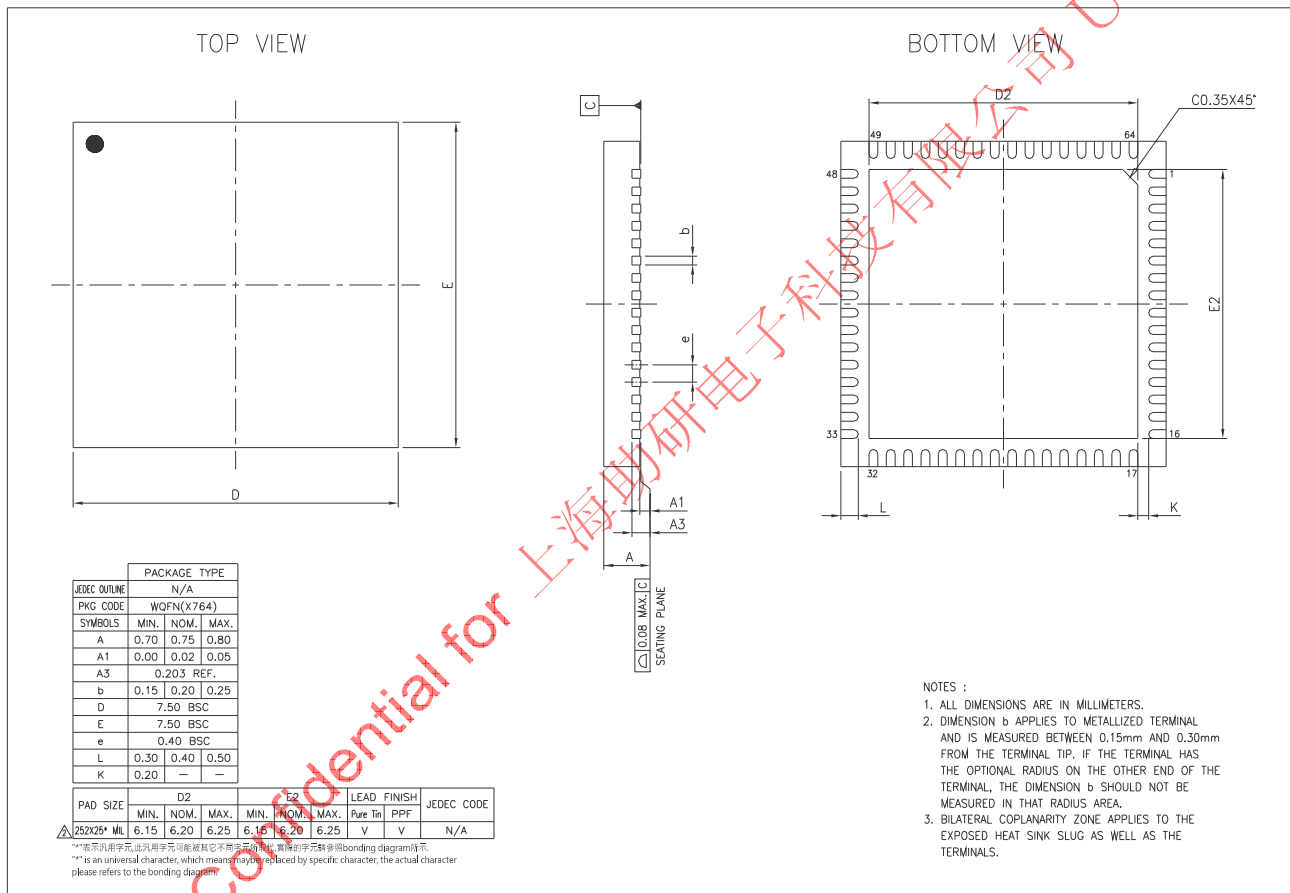


Figure 9.1 Package Dimensions



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