LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT7911D

Type-C to Dual-port MIPI DSI/CSI with Audio

Datasheet

1. Features

- **Type-C**
  - Compliant with VESA DisplayPort Alt Mode on USB Type-C Standard version1.0
  - Compliant with USB Power Delivery Rev.2.0
  - Compatible with USB Type-C V1.1
  - Compliant with HDMI 1.4b Alt Mode on USB Type-C specification V1.0
  - Built-in CC controller for plug and orientation detection
  - Dual-port CC for charger and normal communication.
- **DP/eDP Receiver**
  - Compliant with DisplayPort Specification 1.2 for 1.62Gbps, 2.7Gbps ,5.4Gbps
  - Compliant with DisplayPort Specification version 1.2 and Embedded DisplayPort (eDP) Specification version 1.4
  - Support DisplayPort 1, 2，4 lanes
  - Support HDCP 1.3
  - Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
  - Fast and full Link Training for embedded DisplayPort system
  - Adaptive DisplayPort Receiver Equalization for PCB, cable and connector losses
  - Support AUX and IIC for firmware updating
- **Single/Dual-Port MIPI® DSI/CSI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2& DSI1.02 &CSI-2 1.0
  - 1 Clock Lane, and 1~4 Configurable Data Lanes per port
  - 1/2 configurable port
  - 80Mb/s~1.5Gb/s per data lane
  - Data lane and polarity swapping
  - Maximum 64pixels overlap for each half
  - Both non-burst and burst video mode supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2,20-bit YCbCr4:2:2,24-bit YCbCr 4:2:2, 12-bit YCbCr4:2:0Video Format
  - Video stream copy mode for each single/dual-port
  - Side-by-side 3D support
  - Port swap
- **Miscellaneous**
  - 3.3V/1.2V Supply Power
  - Internal CSC support conversions between YCbCr 4:4:4 and RGB, and between YCbCr 4:2:2 and YCbCr 4:4:4
  - Support SPDIF and 2-channel IIS audio output
  - Support 100KHz and 400KHz I2C slave
  - Power from phone or adapter mode selection
  - Integrated Microprocessor
  - Embedded EDID shadow.
  - Temperature Range: -40°C ~ +85°C
  - ESD 4kV HBM
  - Package:QFN64 7.5x7.5

2. Description

The LT7911D is a high performance Type-C to MIPI®DSI/CSI chip for VR/Smart phone/Display application.

For DP1.2 input, LT7911D can be configured as 1,2,4 lane, also support lane swap function. Adaptive equalization makes it suitable for long cable application and the maximum bandwidth is up to 21.6Gbps.

For MIPI®DSI/CSI output, LT7911D features configurable single-port or dual-port MIPI®DSI/CSI with 1 high-speed clock lane and 1~4 high-speed data lanes operating at maximum 1.5Gb/s/lane, which can support a total bandwidth of up to 12Gbps. LT7911D supports Burst mode DSI video data transferring, also support flexible video data mapping path.

For 2D video stream, the same video stream can be mapped to two separated panel, for 3D video format, left side data can be sent to one panel, and right side data can be sent to another panel.

With sophisticated MCU and the Embedded Flash, LT7911D support EDID buffer, DP/eDP input detection and determine to enter into power saving mode automatically. When the receiver of LT7911D locks the input signal, MCU can read the recovered timing parameters by MSA registers to match the ASSR. The DPCD registers are accessible via system I2C when debugging the full link training. Once the fast link training used, system time will save at least 400ms.

3. Applications

- Mobile system
- VR

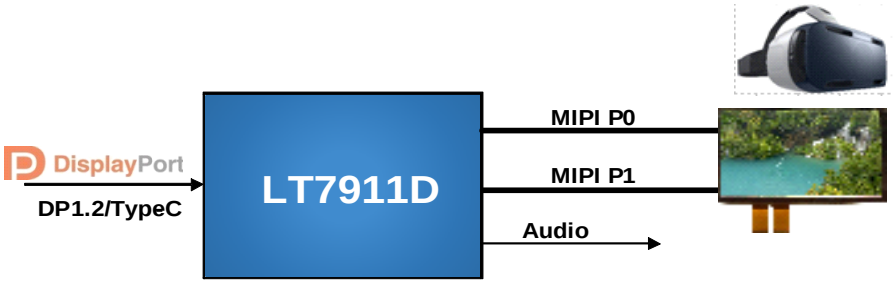

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT7911D	-40℃ to+85℃	QFN64 (7.5*7.5)	Tray

5. Revision History

Version	Owner	Content	Date
R1.0	Terry	Initial datasheet creation	11/15/2017
R1.1	Terry	Update about feature information	04/27/2018
R1.2	Terry	Update about feature and electrical characteristics information	08/16/2018
	N Wang	Update package information	11/15/2018

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6. Pinning Information

6.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance. Maximum trace length mismatch should be less than 5mil and keep total trace length to a minimum for all differential traces. Routing differential pairs on the top or bottom layer with no vias as on signal path is highly recommended.

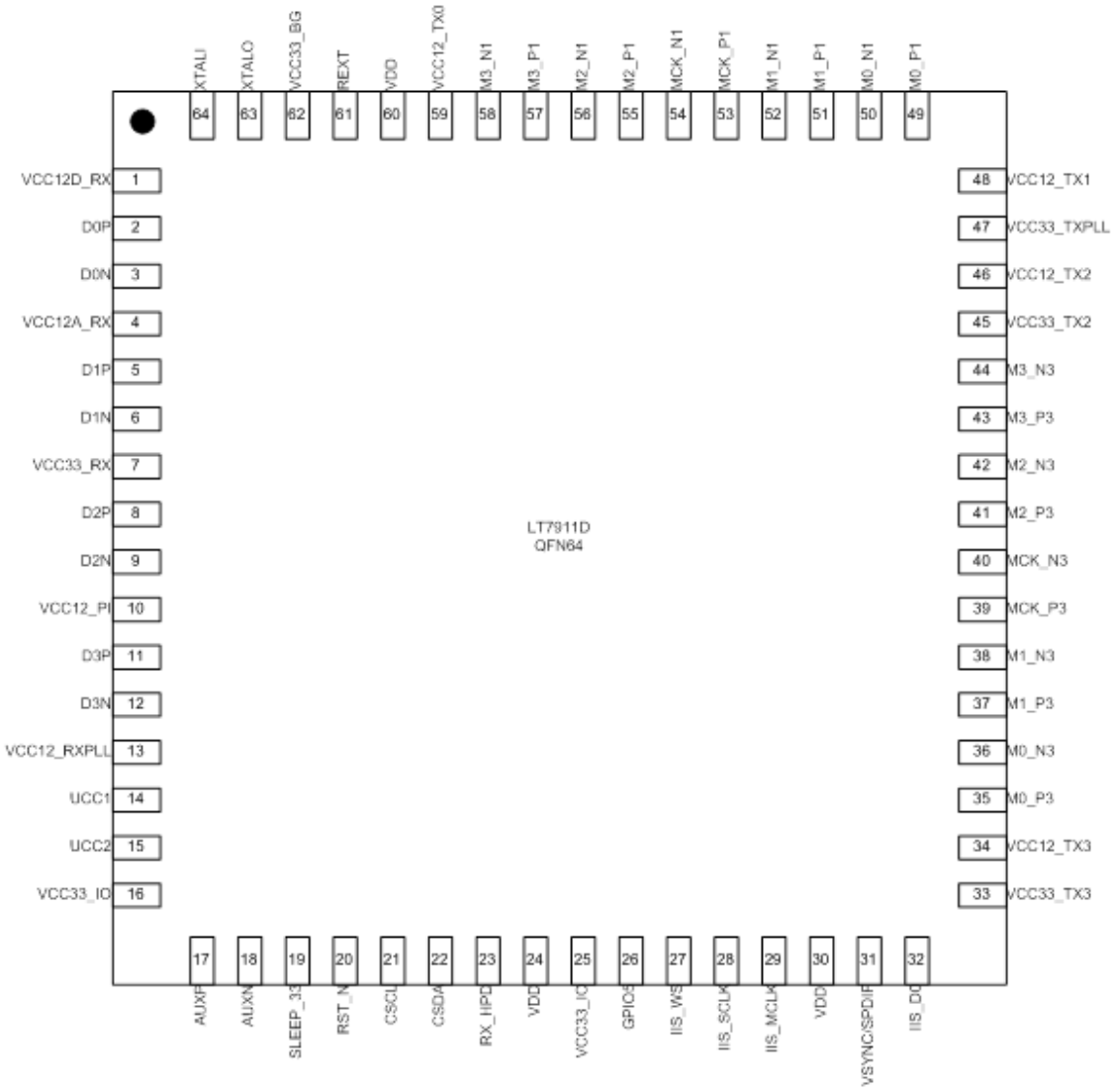


Figure 6.1.1 LT7911D Pin Assignment (Top View)

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitors recommended to be installed near all the LT7911D power pins. To avoid large current loops and trace inductance, thetrace length between decoupling capacitor and device power inputs pins must be minimized.

6.2 Pin Description

Table 6.2.1 Pin Description

Pin#	Pin Name	I/O Type	I/O Dir	Description
65	VSS	PG	I/O	Ground(EPAD)
16,25	VCC33_IO	PG	I/O	3.3V IO Power
62	VCC33_BG	PG	I/O	3.3V Power for BG
7	VCC33_RX	PG	I/O	3.3V Power for RX
45	VCC33_TX2	PG	I/O	3.3V Power for MIPI TX Port2
33	VCC33_TX3	PG	I/O	3.3V Power for MIPI TX Port3
47	VCC33_TXPLL	PG	I/O	3.3V Power for TXPLL
24,30,60	VDD	PG	I/O	1.2V Core Power
10	VCC12_PI	PG	I/O	1.2V Power for PI
13	VCC12_RXPLL	PG	I/O	1.2V Power for RXPLL
4	VCC12A_RX	PG	I/O	1.2V Power for RX Analog Part
1	VCC12D_RX	PG	I/O	1.2V Power for RX Digital Part
59	VCC12_TX0	PG	I/O	1.2V Power for MIPI TX Port0
48	VCC12_TX1	PG	I/O	1.2V Power for MIPI TX Port1
46	VCC12_TX2	PG	I/O	1.2V Power for MIPI TX Port2
34	VCC12_TX3	PG	I/O	1.2V Power for MIPI TX Port3
11	D3P	Analog	I	RX Data Channel Lane-3 Positive Input Maximum data rate is 5.4Gbps.
12	D3N	Analog	I	RX Data Channel Lane-3 Negative Input Maximum data rate is 5.4Gbps.
8	D2P	Analog	I	RX Data Channel Lane-2 Positive Input Maximum data rate is 5.4Gbps.
9	D2N	Analog	I	RX Data Channel Lane-2 Negative Input Maximum data rate is 5.4Gbps.
5	D1P	Analog	I	RX Data Channel Lane-1 Positive Input Maximum data rate is 5.4Gbps.
6	D1N	Analog	I	RX Data Channel Lane-1 Negative Input Maximum data rate is 5.4Gbps.
2	D0P	Analog	I	RX Data Channel Lane-0 Positive Input Maximum data rate is 5.4Gbps.
3	D0N	Analog	I	RX Data Channel Lane-0 Negative Input Maximum data rate is 5.4Gbps.
17	AUXP	Analog	I/O	AUX Positive Input
18	AUXN	Analog	I/O	AUX Negative Input
64	XTALI	Analog	I/O	XTAI for Debug
63	XTALO	Analog	I/O	XTAO for Debug
57	M3_P1	Analog	O	MIPI TX Port1/Lane3 Channel Positive Input Maximum data rate is 1.5Gbps.
58	M3_N1	Analog	O	MIPI TX Port1/Lane3 Channel Negative Input Maximum data rate is 1.5Gbps.
55	M2_P1	Analog	O	MIPI TX Port1/Lane2 Channel Positive Input Maximum data rate is 1.5Gbps.
56	M2_N1	Analog	O	MIPI TX Port1/Lane2 Channel Negative Input Maximum data rate is 1.5Gbps.
53	MCK_P1	Analog	O	MIPI TX Port1/Clock Channel Positive Input

Pin#	Pin Name	I/O Type	I/O Dir	Description
				Maximum Frequency is 750MHz.
54	MCK_N1	**Analog**	**O**	**MIPI TX Port1/Clock Channel Negative Input** Maximum Frequency is 750MHz.
51	M1_P1	**Analog**	**O**	**MIPI TX Port1/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
52	M1_N1	**Analog**	**O**	**MIPI TX Port1/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
49	M0_P1	**Analog**	**O**	**MIPI TX Port1/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
50	M0_N1	**Analog**	**O**	**MIPI TX Port1/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
43	M3_P3	**Analog**	**O**	**MIPI TX Port3/Lane3 Channel Positive Input** Maximum data rate is 1.5Gbps.
44	M3_N3	**Analog**	**O**	**MIPI TX Port3/Lane3 Channel Negative Input** Maximum data rate is 1.5Gbps.
41	M2_P3	**Analog**	**O**	**MIPI TX Port3/Lane2 Channel Positive Input** Maximum data rate is 1.5Gbps.
42	M2_N3	**Analog**	**O**	**MIPI TX Port3/Lane2 Channel Negative Input** Maximum data rate is 1.5Gbps.
39	MCK_P3	**Analog**	**O**	**MIPI TX Port3/Clock Channel Positive Input** Maximum Frequency is 750MHz.
40	MCK_N3	**Analog**	**O**	**MIPI TX Port3/Clock Channel Negative Input** Maximum Frequency is 750MHz.
37	M1_P3	**Analog**	**O**	**MIPI TX Port3/Lane1 Channel Positive Input** Maximum data rate is 1.5Gbps.
38	M1_N3	**Analog**	**O**	**MIPI TX Port3/Lane1 Channel Negative Input** Maximum data rate is 1.5Gbps.
35	M0_P3	**Analog**	**O**	**MIPI TX Port3/Lane0 Channel Positive Input** Maximum data rate is 1.5Gbps.
36	M0_N3	**Analog**	**O**	**MIPI TX Port3/Lane0 Channel Negative Input** Maximum data rate is 1.5Gbps.
14	UCC1	**Analog**	**I/O**	**CC1 Connected with Source**
15	UCC2	**Analog**	**I/O**	**CC2 Connected with Source**
23	RX_HPD	**OD**	**O**	**Hot Plug Signal**
28	IIS_SCLK	**LVTTL**	**I/O**	**SCLK of IIS**
31	VSYNC/SPDIF	**LVTTL**	**I/O**	**VSYNC Output or SPDIF of IIS**
32	IIS_D0	**LVTTL**	**I/O**	**D0 of IIS**
26	GPIO5	**LVTTL**	**I/O**	**GPIO**
27	IIS_WS	**LVTTL**	**I/O**	**WS of IIS**
20	RSTN	**Schmitt**	**I**	**External Reset Signal, Low is Reset.**
29	IIS_MCLK	**LVTTL**	**I/O**	**MCLK of IIS**
19	SLEEP_33	**Schmitt**	**I**	**External Sleep Mode Control Signal**
22	CSDA	**Schmitt, OD**	**I/O**	**Slave I2C SDA Signal For Program Register**
21	CSCL	**Schmitt, OD**	**I**	**Slave I2C SCL Signal For Program Register**
61	REXT	**Analog**	**O**	**External 7.68Kohm Resistor For BG**

7. Function Description

7.1 Function Block Diagram

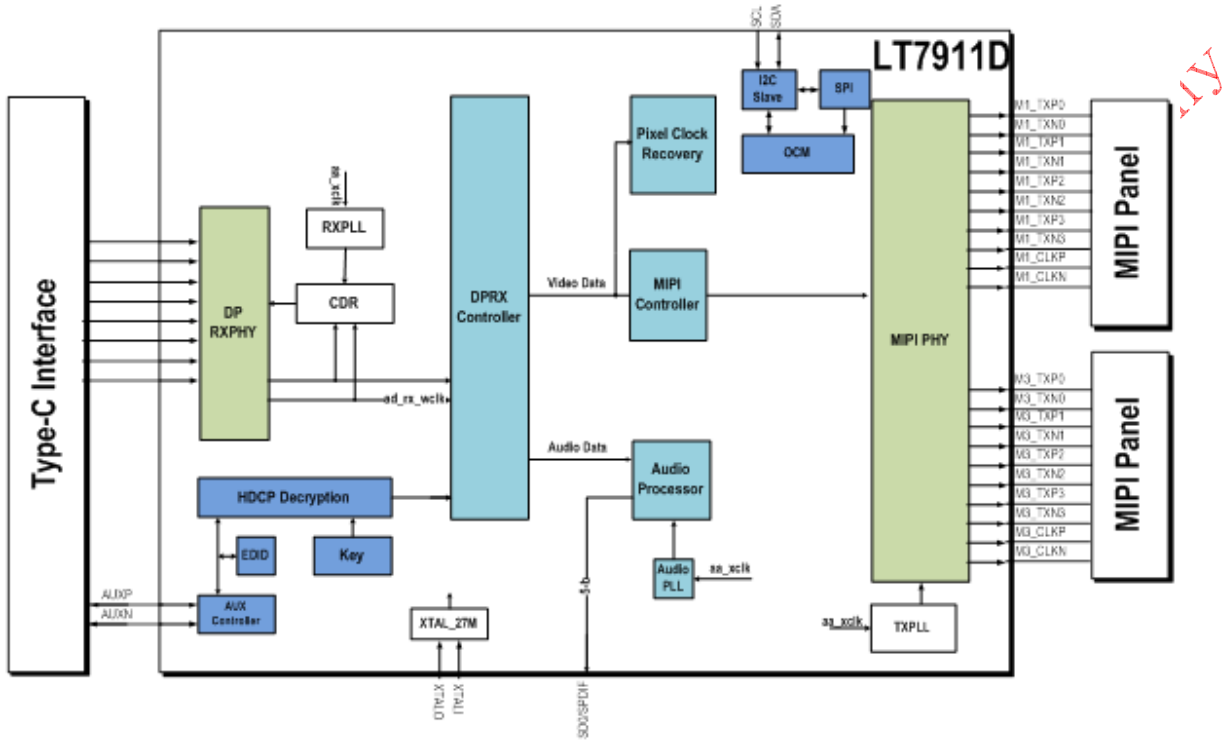


Figure 7.1.1 Function Block Diagram

8. Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL VCC33_RX	3.3V Power Supply Voltage	-0.3		3.63	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	-0.3		1.32	V
V_I	CMOS Terminal Input Voltage Range	-0.3		3.63	V
V_O	CMOS Terminal Output Voltage Range	-0.3		3.63	V
T_S	Storage Temperature	-40		125	℃
ESD	HBM Elastrostatic Discharge Level		4000		V

Notes:
1.Permanent device damage may occur if absolute maximum conditions are exceeded.
2.Function operation should be restricted to the conditions described under Normal Operating Conditions.

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
VCC33_IO, VCC33_TX2,VCC33_TX3,VCC33_BG, VCC33_TXPLL, VCC33_RX	3.3V Power Supply Voltage	2.97	3.3	3.63	V
VDD,VCC12_TX0,VCC12_TX1, VCC12_TX2,VCC12_TX3, VCC12A_RX,VCC12D_RX,VCC12_PI,VCC12_RXPLL	1.2V Power Supply Voltage	1.08		1.32	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

TMDS RX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{IDIFF}	Differential input voltage level	150		1200	mV
V_{ICM}	Input common mode voltage	VCC33		VCC33	mV

		_RX-700		_RX-37.5	
R_{TERM}	Single-ended termination resistance	45	50	55	Ω
MIPI HS Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{CM}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS transmit output high voltage			360	mV
Z_{OS}	Single ended output impedance	40	50	62.5	Ω
MIPI LP Line TX DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Output low-level SE voltage	-50	0	50	mV
V_{OH}	Output high-level SE voltage	1.1	1.2	1.3	V
Z_{OLP}	Single-ended output impedance	110			Ω

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

TMDS RX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
V_S	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_{INTRA_SKEW}	Intra-pair skew at sink connector			$0.15T_{bit}+112$	ps
T_{INTER_SKEW}	Inter-pair skew at sink connector			$0.2T_{character}+1.78$	ns
T_{JITTER}	TMDS clock jitter			$0.3T_{bit}$	ps
MIPI HS Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
$\Delta V_{CMTX(HF)}$	Common mode Voltage variation above 450MHz			15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common mode Voltage variation between 50-450MHz			25	mV_{PEAK}
t_R and t_F (rise/fall time, 20%-80%)	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
MIPI LP Line TX AC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
T_{RLP}/T_{FLP}	Single ended output rise/fall time,15% to 85%, C_L< 70pF			25	ns
T_{REOT}	Single ended output rise/fall time,30% to 85%, C_L< 70pF			35	ns
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	20			ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90			ns

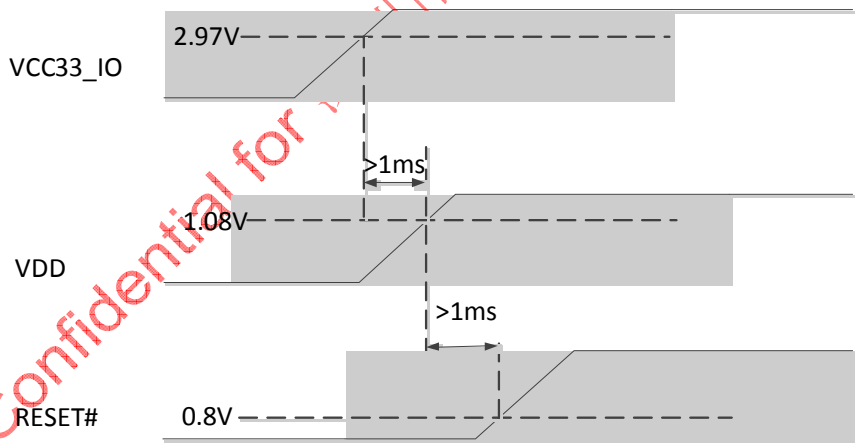
δ V/δtSR	Slew rate @ CLOAD = 0			500	mV/ns
	Slew rate @ CLOAD = 5pF			350	mV/ns
	Slew rate @ CLOAD = 20pF			250	mV/ns
	Slew rate @ CLOAD = 70pF			150	mV/ns
	Slew rate @ CLOAD = 0 to 70pF(falling edge only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF(rising edge only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF(rising edge only)	30–0.075*(VO,INST-700)			mV/ns

8.5 Power Consumption

Table 8.5.1 Power Consumption

Condition	Supply Current(3.3V)	Supply Current(1.2V)	Unit
5.4G_4lane, TX 2port	42	400	mA
2.7G_4lane, TX 2port	34	350	mA

8.6 Power-up and Reset Sequence



Note:
（1）1.2V power should be set up at least 1ms later than 3.3V power, the internal reset signal should be released after 1.2V power is ready.
（2）External RESET# signal should be set up at least 1ms later than 1.2V.

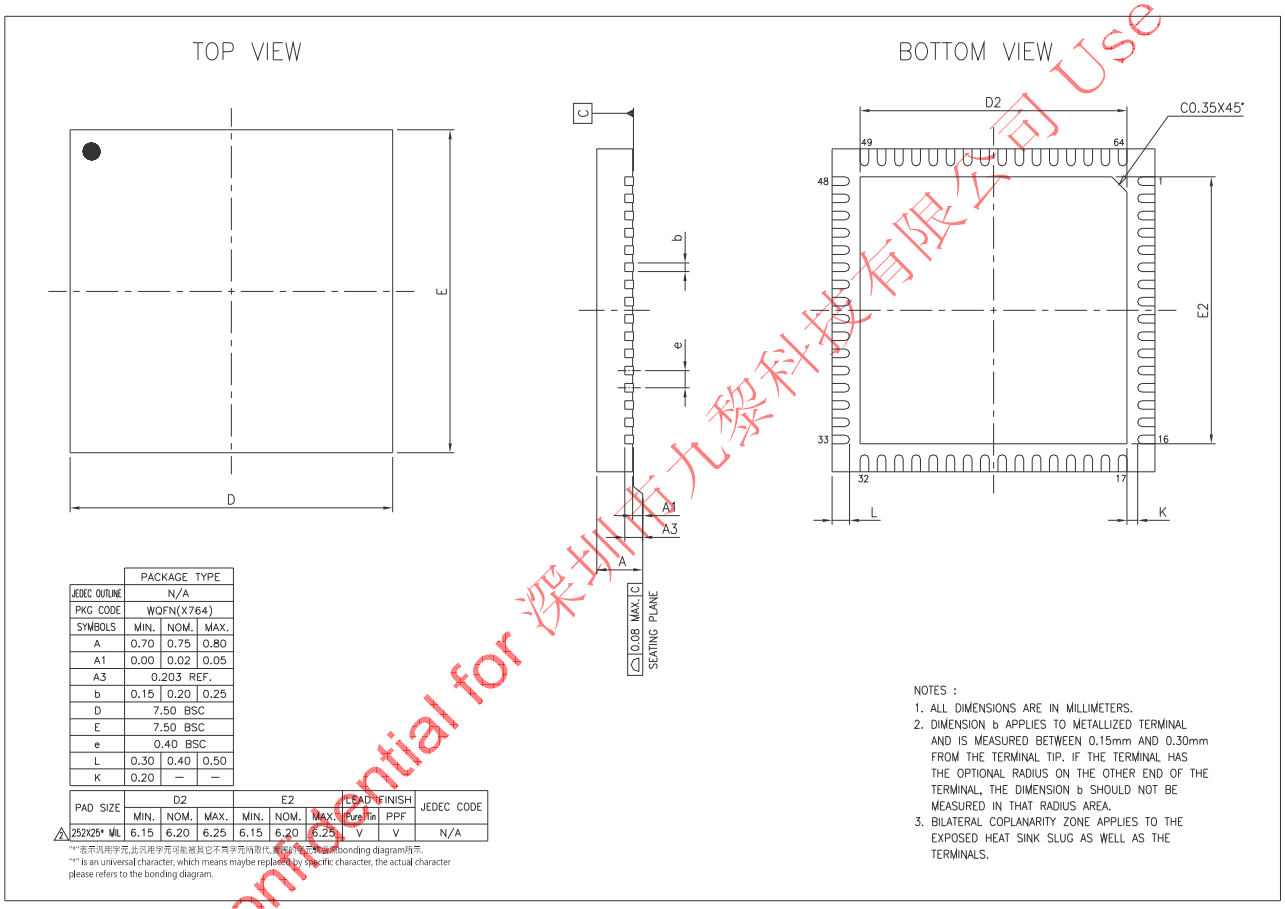
Figure 8.6.1 Power-up and Reset Sequence

9. Package Information

The LT7911D is packaged in a 64-lead QFN package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠ 252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

"*"表示讯用字元,此讯用字元可能被其它不同字元码取代,实际请依bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 9.1 Package Dimensions

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