LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT8511EX HDMI/DP-VGA/YPbPr Converter

Data Sheet

We produce mixed-signal products for a better digital world!

Table of Contents

1. Revision History

Version	Owner	Content	Date
Preliminary	Rends	Initial datasheet creation	03/17/2014
Preliminary	NWang	Update package information	03/20/2014
1.0	XH.Guo	Update power consumption	05/12/2014
1.1	Dsren	Update pin description	06/05/2014
1.2	FChen	Add dual-mode feature	06/09/2014
1.3	Dsren	Update VGA output RGB name and order for compliant with LT8511	06/10/2014
1.4	N.Wang	Check package information	07/14/2014
1.5	N.Wang	Add package die pad information	11/11/2014

.2. General Description

LT8511EX is a low cost high performance single port HDMI and dual-mode Displayport receiver which is compliant with HDMI 1.4. The RX can receive 4Kx2K(1080p 8/10/12bit deep color, up to 3.4GHz data ratio) input. Besides it supports analog video-output(VGA or YPbPr) up to 4Kx2K, 1920x1200, and 1080p with three high resolution DACs. The chip integrates dual-mode receiver front end with equalizer, HDMI core and HDCP engine in a single chip.

2.1 Features

- On-chip HDMI and dual-mode DP receiver with Equalizer, supports 4Kx2K, 1920x1200 and 1080p 8/10/12bit deep color, up to 3.4GHz data ratio.
- On chip receiver core which is compliant with HDMI1.4 specification.
- On chip HDCP engine which is compliant with HDCP1.4 spec.
- HDCP key stored in MCU for BOM cost reduction.
- Supports analog video output (VGA or YPbPr) up to 4Kx2K, 1920x1200, and 1080p with three on chip DAC.
- On-chip audio decoder which supports 2-channel IIS and SPDIF audio outputs.
- Support audio soft mute.
- On chip YCC422 to YCC444 conversion.
- On chip YCC to RGB and RGB to YCC conversion in ITU-R BT.601 and 709 color space.
- Support separate sync output and SOG/SOY.
- Flexible interrupt registers with interrupt pin.
- Link on and Valid DE detection.
- The LT8511EX is offered in 64-pin QFN package, and operates over -40°C to +85°C temperature range

2.2 LT8511EX Pin Diagram

64 pin QFN package, it is named as LT8511EX. Pin diagram is shown as figure1a.

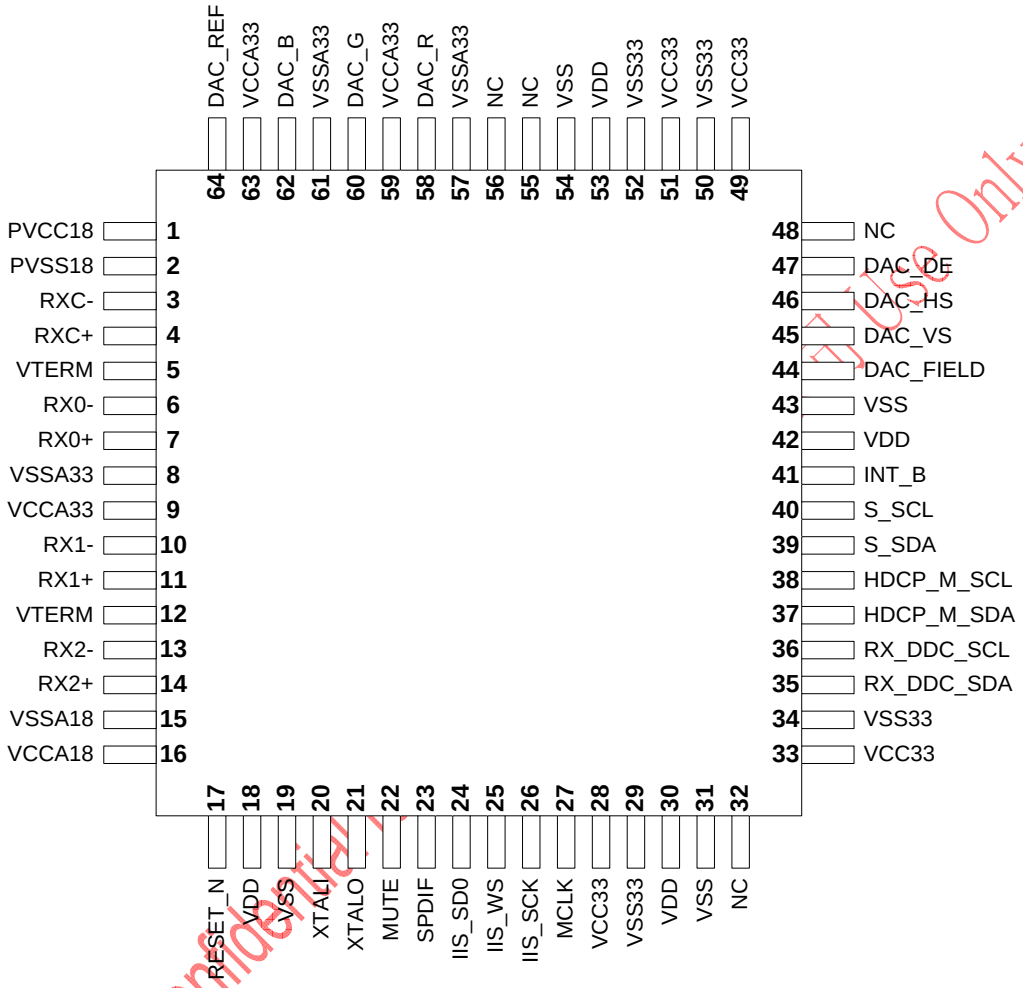


Figure 1a: LT8511EX Pin Diagram

2.3 Functional Description

The LT8511EX provides a complete solution for converting HDMI to analog VGA/YPbPr.

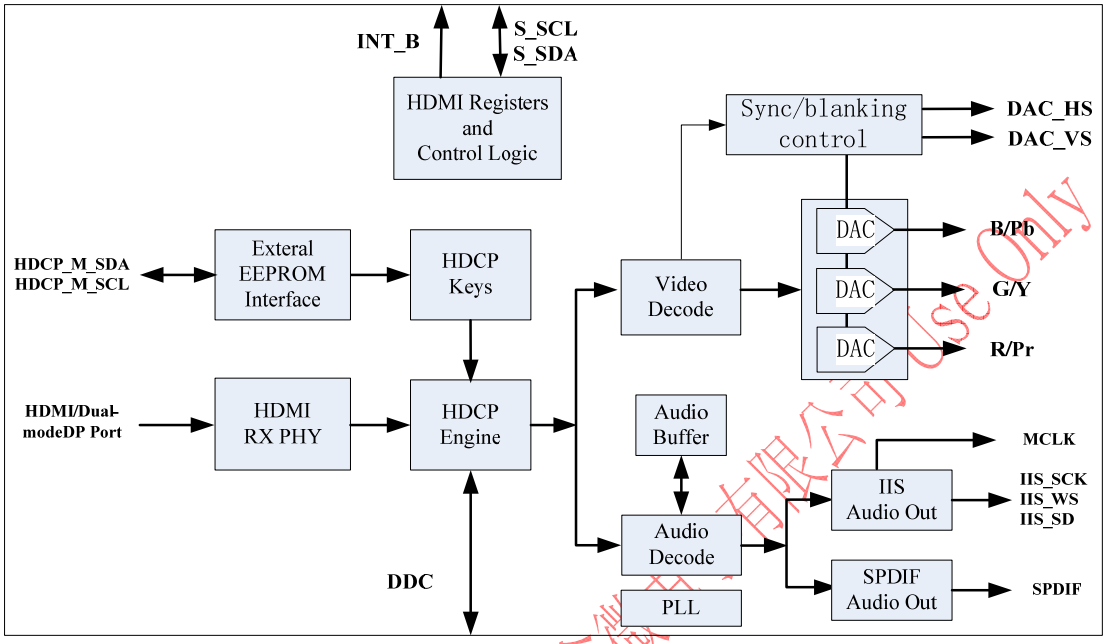


Figure 2: Function Block Diagram

Figure 2 shows the functional blocks of the chip. HDMI or dual-mode data is received by RX PHY, then decoded by HDCP engine. The decoded data flow is sliced to video and audio data channels. Video channel transfers RGB signal or YCbCr signal according to the type of the display device. A PLL provides an audio clock refer to crystal oscillator, and output audio signal is synchronized with video frame by TMDS clock.

2.3.1 HDMI/Dual-mode DP RX PHY

The receiver PHY can support HDMI or dual-mode DP signals, which meets more consumer requirement. And the receiver has built-in equalizer which enables the port to receiver HDMI or dual-mode DP signals through longer cable, and ensures the signal can be recovered better. The receiver is compliant with HDMI 1.4. The receiver front-end can be programmed so the termination voltage is set different from 3.3V for better DP signal detection. The front-end and entire receiver support video resolution up to 4Kx2K , 1920x1200 and 1080p.

The chip also integrates RX/TX side on-die-terminations (ODTs), and employs the ODT management circuitry for cost-efficient system design and enhanced performance.

2.3.2 HDCP Engine

The LT8511EX includes HDCP 1.4(High - Bandwidth Digital Content Protection) circuitry with internal memory to store a unique HDCP device key. The HDCP protocol ensures protection from unauthorized duplication of copyrighted media content.

The LT8511EX employs a HDCP decryption engine. It contains the decryption logic for all HDMI data (audio, video, and control). Hardware - implemented HDCP authentication and decryption for audio and video reduce external micro - controller overhead. HDCP

decryption and authentication is performed automatically following device initialization. Pre‐programmed HDCP keys and Key Selector Vectors(KSV) are stored in embedded ROM for the decryption process, also provide highest level of security.

2.3.3 Video Decoder

Video data is decoded to RGB or YCbCr format through data decoder according to register set for different application. Output video data supports both separated sync and SOG. When Sync-On-Green mode, it outputs video data stream to three 10-bit DACs, and the sync signal is composite into the G channel at the DAC by the sync/blanking control module.

2.3.4 Audio Decode

Audio data is extracted and decoded from HDMI data stream. The decoded audio data is buffered in an on-chip FIFO. An on-chip PLL is used to regenerate audio clock from the outside crystal oscillator. Digital audio signals in both IIS and SPDIF format are generated based on this TMDS or regenerate clock.

2.3.5 InfoFrame Data

All types of Packet/InfoFrame data can be extracted, decoded from HDMI data stream and stored in the internal registers. The AVI (Auxiliary Video Information), Audio and MS (MPEG Source) InfoFrames are always extracted and put in dedicated buffers. Other Packet/InfoFrame type can be selectively extracted and stored in 2 shared packet buffers. Whenever an InfoFrame is received, an interrupt flag is set in an internal register and INT_B pin (active low) is asserted. The MCU can extract the InfoFrame content through IIC bus.

2.3.6 Application Diagram

Figure 3 shows the application of the chip.

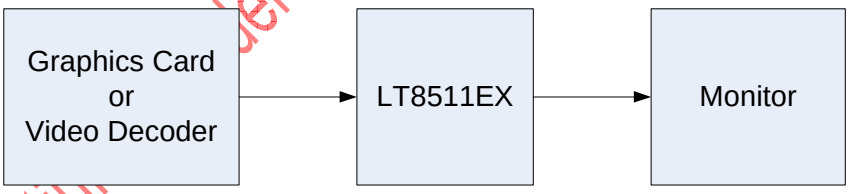


Figure 3: Application Diagram

2.4 Pin Descriptions

(I/O description: A=Analog, I=Input, O=Output, P=Power, G=Ground)

PIN	NAME	I/O	FUNCTION	NOTES
HDMI RX Pins				
1	PVCC18	AP	Power supply pins for HDMI receiver PLL	1.8V
2	PVSS18	AG	Ground supply pins for HDMI receiver PLL	
3	RXC-	AI	HDMI receiver clock negative analog input	
4	RXC+	AI	HDMI receiver clock positive analog input	
5	VTERM	AP		3.3V
6	RX0-	AI	HDMI receiver channel 0 negative analog input	
7	RX0+	AI	HDMI receiver channel 0 positive analog input	
8	VSSA33	AG	3.3V ground supply pins for HDMI Receiver	
9	VCCA33	AP	3.3V power supply pins for HDMI Receiver	3.3V
10	RX1-	AI	HDMI receiver channel 1 negative analog input	
11	RX1+	AI	HDMI receiver channel 1 positive analog input	
12	VTERM	AP		3.3V
13	RX2-	AI	HDMI receiver channel 2 negative analog input	
14	RX2+	AI	HDMI receiver channel 2 positive analog input	
15	VSSA18	AG	1.8V ground supply pins for HDMI receiver	
16	VCCA18	AP	1.8V power supply pins for HDMI receiver	1.8V
Control Pins				
17	RESET_N	I	Global reset, active low	
Power Ground Pins				
18	VDD	P	Power supply pins for digital	1.8V
19	VSS	G	Ground supply pins for digital	
Crystal Pins				
20	XTALI	I	Crystal oscillator input	25MHZ
21	XTALO	O	Crystal oscillator output	
Audio Pins				
22	MUTE	O	Mute output for audio ports	
23	SPDIF	O	SPDIF output	
24	I2S_O0	O	I2S output	
25	WS_O	O	I2S word select output	
26	SCLK_O	O	I2S serial clock output	

27	MCLK_O	O	I2S audio master clock output	
Power Ground Pins				
28	VCC33	P	Power supply pins for IO	3.3V
29	VSS33	G	Ground supply pins for IO	
30	VDD	P	Power supply pins for digital	1.8V
31	VSS	G	Ground supply pins for digital	
32	NC			
33	VCC33	P	Power supply pins for IO	3.3V
34	VSS33	G	Ground supply pins for IO	
Control Pins				
35	RX_DDC_SDA	IO	HDMI receiver DDC data channel	5V-tolerant, internal pull-up
36	RX_DDC_SCL	IO	HDMI receiver DDC clock channel	5V-tolerant, internal pull-up
37	HDCP_M_SDA	IO	Master I2C data channel	5V-tolerant
38	HDCP_M_SCL	IO	Master I2C clock channel	5V-tolerant
39	S_SDA	IO	Slave I2C data channel	5V-tolerant
40	S_SCL	IO	Slave I2C clock channel	5V-tolerant
41	INT_B	O	Chip interrupt output, active low	
Power Ground Pins				
42	VDD	P	Power supply pins for digital	1.8V
43	VSS	G	Ground supply pins for digital	
DAC Control Pins				
44	DAC_FIELD	O	Field output to indicate 1st field or 2nd field in an interlaced video output. The polarity can be program by register	
45	DAC_VS	O	VGA vertical sync output	
46	DAC_HS	O	VGA horizontal sync output	
47	DAC_DE	O	Video data enable output. When asserted, the data presents on D0/D1/D2 pins is a valid video signal	
48	NC			
Power Ground Pins				
49	VCC33	P	Power supply pins for IO	3.3V
50	VSS33	G	Ground supply pins for IO	
51	VCC33	P	Power supply pins for IO	3.3V
52	VSS33	G	Ground supply pins for IO	
53	VDD	P	Power supply pins for digital	1.8V
54	VSS	G	Ground supply pins for digital	
55	NC			
56	NC			
DAC Pins				
57	VSSA33	AG	3.3V ground supply pins for DAC	
58	DAC_R	AO	VGA R channel or YPbPr Pr channel analog output	
59	VCCA33	AP	3.3V power supply pins for DAC	3.3V

60	DAC_G	AO	VGA G channel or YPbPr Y channel analog output	
61	VSSA33	AG	3.3V ground supply pins for DAC	
62	DAC_B	AO	VGA B channel or YPbPr Pb channel analog output	
63	VCCA33	AP	3.3V power supply pins for DAC	3.3V
64	DAC_REF	AI	DAC reference	

2.5 DC Electrical Characteristics

2.5.1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC_{33}	3.3V Supply Voltage	-0.3		4.0	V
VCC_{18}	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		VCC_{33}+0.3	V
Vo	Output Voltage	-0.3		VCC_{33}+0.3	V
T_{STG}	Storage Temperature	-55		125	ºC
DIFF33	Difference between two 3.3V power pins			1.0	V
DIFF18	Difference between two 1.8V power pins			1.0	V
DIFF3318	Difference between any 3.3V power pins and 1.8V power pins	-1.0		2.0	V

Notes:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

2.5.2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VCC_{33}	3.3V Supply Voltage	3.0	3.3	3.6	V
VCC_{18}	1.8V Supply Voltage	1.62	1.8	1.98	V
VCC_N	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	-40	25	85	ºC

2.5.3 Digtal I/O Specifications

Digital I/O spec. followed LVTTL spec. under normal operating conditions.

2.5.4 DC Specifications

Under normal operating conditions unless otherwise specified

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{ID}	Deferential input voltage, single ended amplitude			150		700	mV
I_{CC}	Operating current	TMDS clk =27M	1.8V		58		mA
			3.3V		97		mA
		TMDS clk =74.25M	1.8V		82		mA
			3.3V		97		mA
		TMDS clk =148.5M	1.8V		121		mA
			3.3V		97		mA
		TMDS clk =225M	1.8V		163		mA
			3.3V		97		mA

2.6 AC Specifications

2.6.1 TMDS Input Timing Diagrams

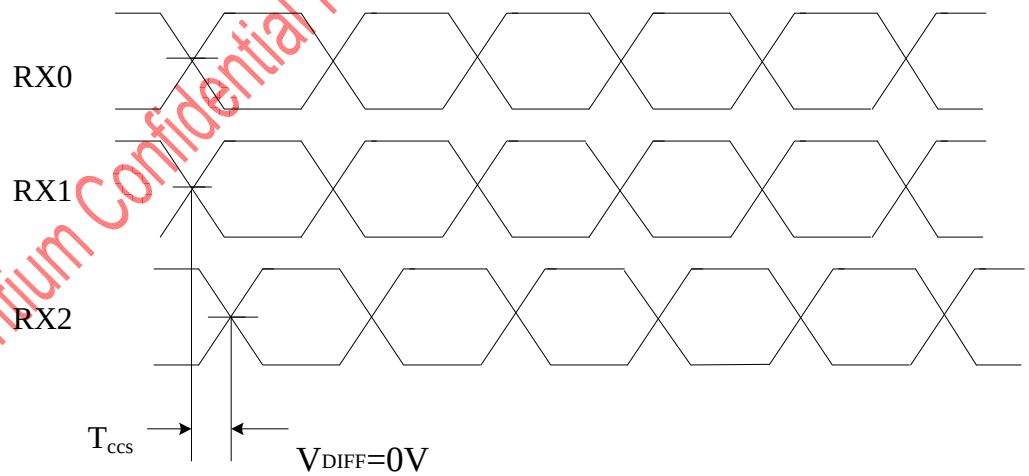


Figure4: TMDS Channel-to-Channel Skew Timing

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{RXC}	Differential Input Clock Frequency		25		340	MHz

T_{DPS}	Intra-Pair(+to-) Differential Input Skew				$0.4T_{bit}$	ps
T_{CCS}	Channel to Channel Differential Input Skew				$2T_{bit}$	ps
T_{IJIT}	Differential Input Clock Jitter Tolerance				$0.3T_{bit}$	ps

2.6.2 I²S Output Timings

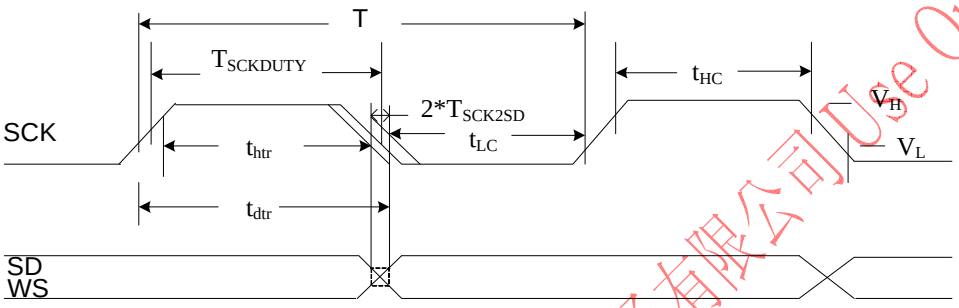


Figure5: I²S Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{tr}	SCK Clock Period(TX)	CL=10pF		1.0		T_{tr}
T_{HC}	SCK Clock HIGH Time	CL=10pF	0.35			T_{tr}
T_{LC}	SCK Clock LOW Time	CL=10pF	0.35			T_{tr}
T_{dtr}	SCK to SD and WS	CL=10pF			0.8	T_{tr}
T_{htr}	Hold Time SCK to SD and WS	CL=10pF	0			T_{tr}
$T_{SCKDUTY}$	SCK Duty Cycle	CL=10pF	40%		60%	T_{tr}
T_{SCK2SD}	SCK-to-SD Delay	CL=10pF	-5		+ 5	ns
T_{AUDDLY}	Audio Pipeline Delay			40	75	us

2.6.3 S/PDIF Output port Timing

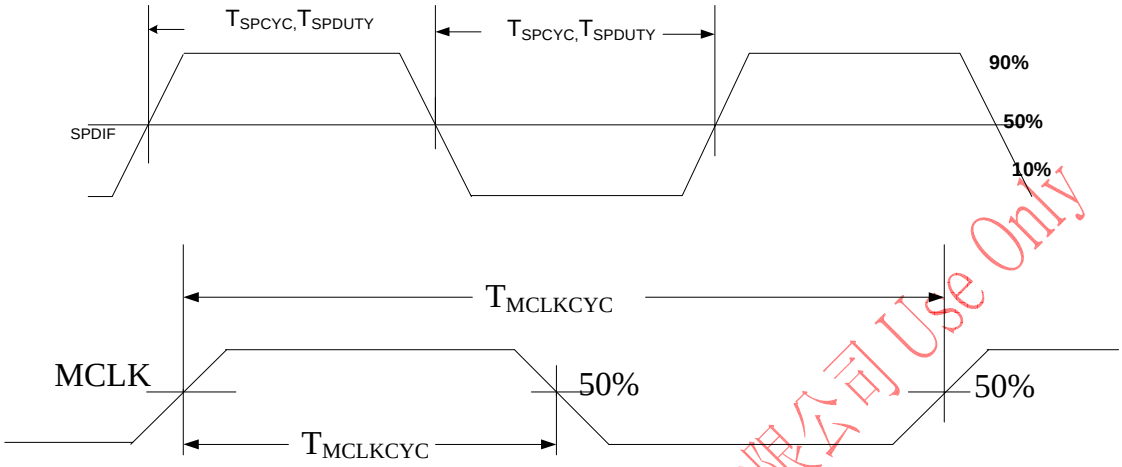


Figure6: S/PDIF Output port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{SPCYC}	SPDIF Cycle Time	CL=10pF		1.0		UI
T_{SPDIF}	SPDIF Frequency		4		24	MHz
T_{SPDUTY}	SPDIF Duty Cycle	CL=10pF	90%		110%	UI
$T_{MCLKCYC}$	MCLK Cycle Time	CL=10pF	10			ns
F_{MCLK}	MCLK Frequency	CL=10pF			98	MHz
$T_{MCLKDUTY}$	MCLK Duty Cycle	CL=10pF	40%		60%	$T_{MCLKCYC}$
T_{AUDDLY}	Audio Pipeline Delay			40	75	us

2.6.4 Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{XTAL}	External Crystal Freq		25	27	28.322	MHz

2.6.5 Miscellaneous Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{12CDVD}	SDA Data Valid delay from SCL falling edge	CL=400pF			300	ns
T_{RESET}	RESET# Signal Low Time for valid reset		45			us
$T_{HDCPINIT}$	HDCP Initialization from stable input		35			ms

2.6.6 RESET# Minimum Timings

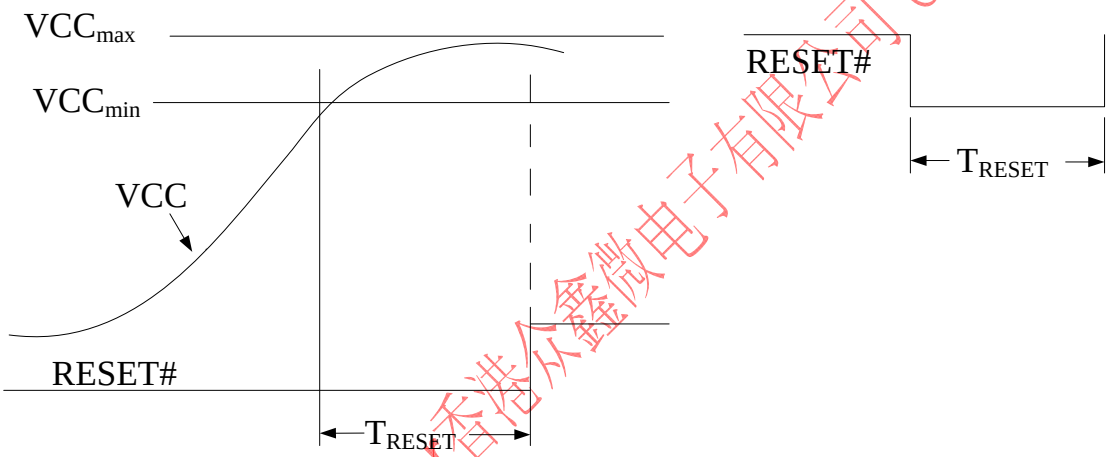


Figure7: RESET# Minimum Timings

2.6.7 Power Supply Sequencing

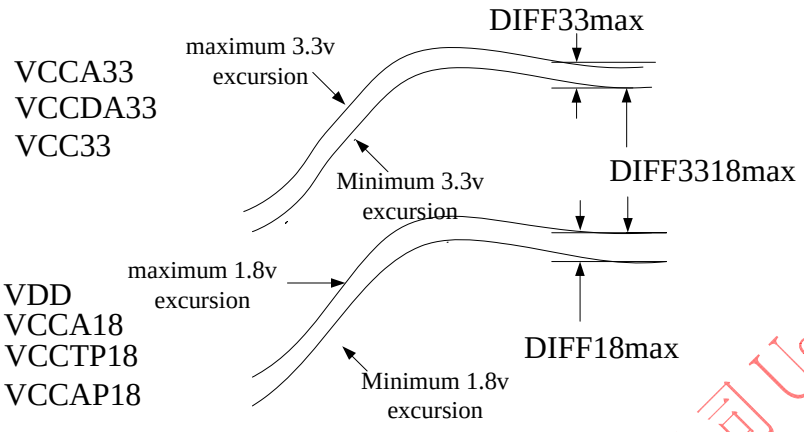


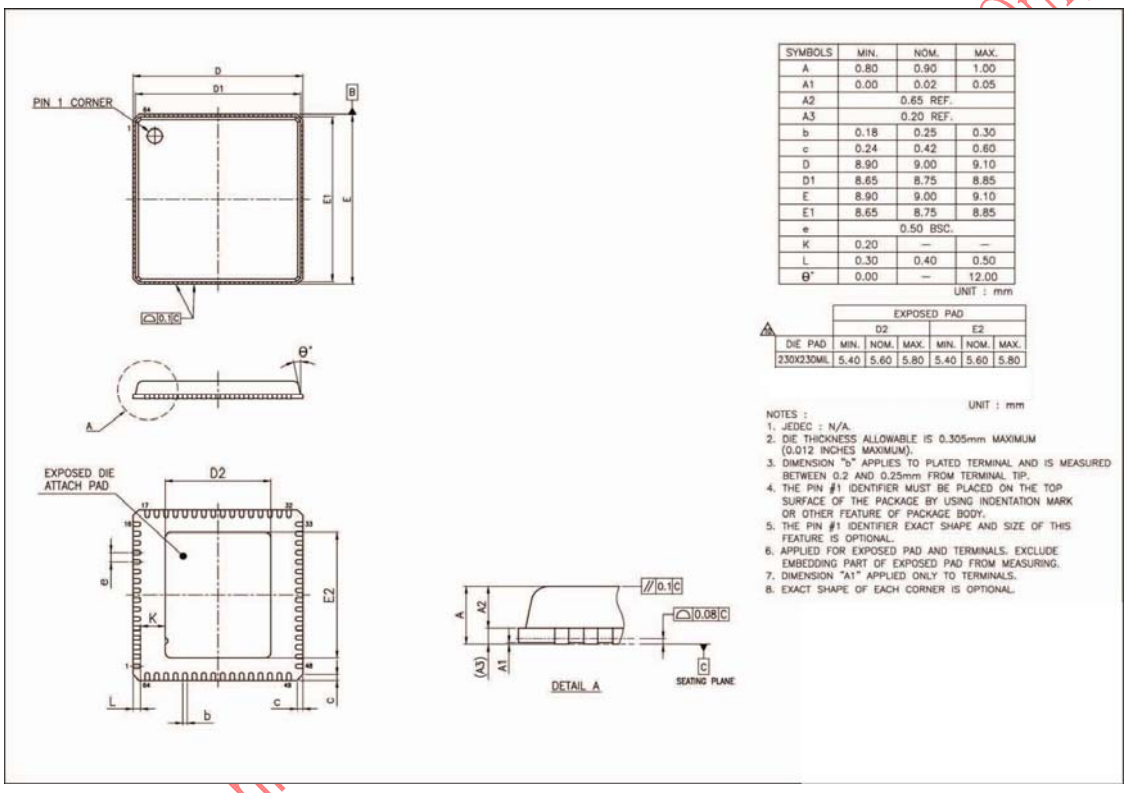
Figure8: Power Supply Sequencing

Symbol	Parameter	Min	Typ	Max	Units
DIFF33	Difference between two 3.3V power pins			1.0	V
DIFF18	Difference between two 1.8V power pins			1.0	V
DIFF3318	Difference between any 3.3V power pins and 1.8V power pins	-1.0		2.0	V

3. Package

3.1 LT8511EX-QFN64L（0909x0.85）

The ePad must not be electrically connected to any other voltage level except ground (GND). The dimension of ePad in PCB should be 5.6x5.6mm. And a clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.



SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.20 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	8.90	9.00	9.10
D1	8.65	8.75	8.85
E	8.90	9.00	9.10
E1	8.65	8.75	8.85
e		0.50 BSC.	
K	0.20	–	–
L	0.30	0.40	0.50
θ°	0.00	–	12.00

UNIT : mm

	EXPOSED PAD					
	D2			E2		
DIE PAD	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
230X230MIL	5.40	5.60	5.80	5.40	5.60	5.80

UNIT : mm

NOTES :
1. JEDEC : N/A.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.