LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT8522EX Matrix Switch

Data Sheet

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Revision History

Version	Owner	Content	Date
Preliminary	Dsren	Initial Matrix Switch Datasheet creation	02/08/2014
Preliminary	Nwang	Check package information	05/26/2014
1.0	Xhguo	Update power consumption	05/28/2014
1.1	Nwang	Update package information	05/30/2014
1.2	Dsren	Update pin description	05/30/2014
1.3	Dsren	Update pin23 and pin24 definition and pin diagram	07/07/2014
1.4	N.Wang	Check package information	07/14/2014
1.5	Xhguo	Update power consumption(add deep color info)	09/01/2014

Table of Contents

1. General Description

The LT8522EX is Lontium's matrix switch chip that supports both two inputs(VGA and HDMI) and two outputs(VGA and HDMI) based on ClearEdge™ technology. The HDMI input interface is compliant with the HDMI 1.4 (High Definition Multimedia Interface) specification. It can also support Dual-Mode DP with HDMI interface. For backward compatibility, this matrix switch also includes two high performance analog interfaces (VGA input and VGA output). It has two high quality digital audio interfaces (audio input and audio output) that support 8-channel audio.

The LT8522EX is offered in a 100-pin LQFP package, with operating temperature range of -40℃-85℃.

1.1. Features

- Direct interface to DVI 1.0 and HDMI V1.4 transmitter
- Support Dual-Mode DP on the same pins with HDMI
- Support resolution up to 4kx2k
- Multiple pixel formats: RGB 6/8/10/12 bit per component (bpc); YCbCr 422/444 8/10/12 bpc
- Compliance with DVI up to 1.65Gbps and HDMI V1.4 up to 3.4Gbps
- HDCP decryption and encryption
- On-chip VGA HDMI EDID shadows
- High input sensitivity, with differential input level down to 150mV
- Receiver side equalization up to 12dB
- Auto Loss of Signal detection
- High jitter tolerance up to 0.7UI
- External IIC slave configuration interface
- Master I2C interface for DDC connection simplifies board layout and lowers cost
- Embedded audio PCM and SPDIF TX and RX.
- Extensive power management for power savings
- Supports analogue video output up to UXGA and 1080p on chip DAC

1.2. Applications

- HD switch boxes
- HD source, Monitors and other applications

1.3. Absolute Maximum Ratings

Supply Voltage	VCC33	…… 3.0V to 3.6V
	VCCA33	…… 3.0V to 3.6V
	PVCC33	…… 3.0V to 3.6V
	ADC_VCC	…… 1.62V to 1.98V
	VCCA18	…… 1.62V to 1.98V
	PVCC18	…… 1.62V to 1.98V
	VDD	…… 1.62V to 1.98V
Operating Junction Temperature Range		…… -40°C to +85°C
Storage Temperature Range		…… -40°C to +85°C

2. Functional Block Description

Figure 1 is functional block diagram of LT8522EX, and the block detail internal relationship is also shown in the diagram.

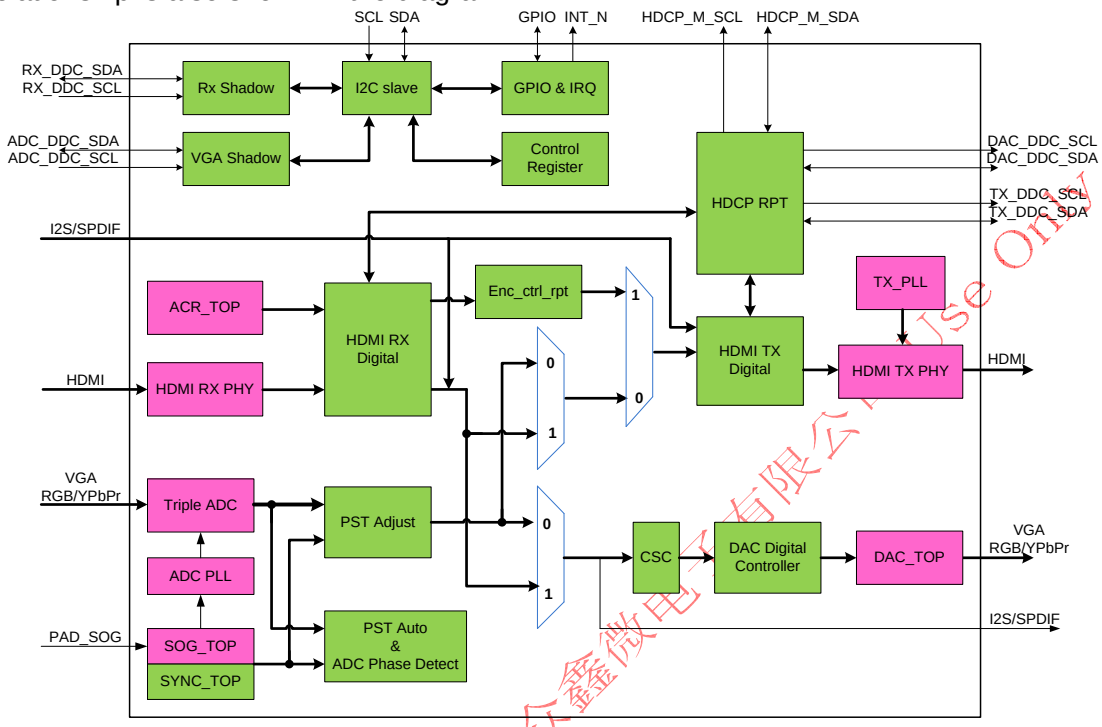


Figure 1: Functional Block Diagram

2.1. Application Diagram

Figure 2 is the normal application diagram of the matrix switch chip. In the chip it includes a triple ADC, a TMDS receiver and associated interfaces, a DAC, and a TMDS transmitter. It also includes two digital audio interfaces(a input and a output). The interface with DisplayPort can be realized through the TMDS interface by adding 500 ohm pull down resistor.

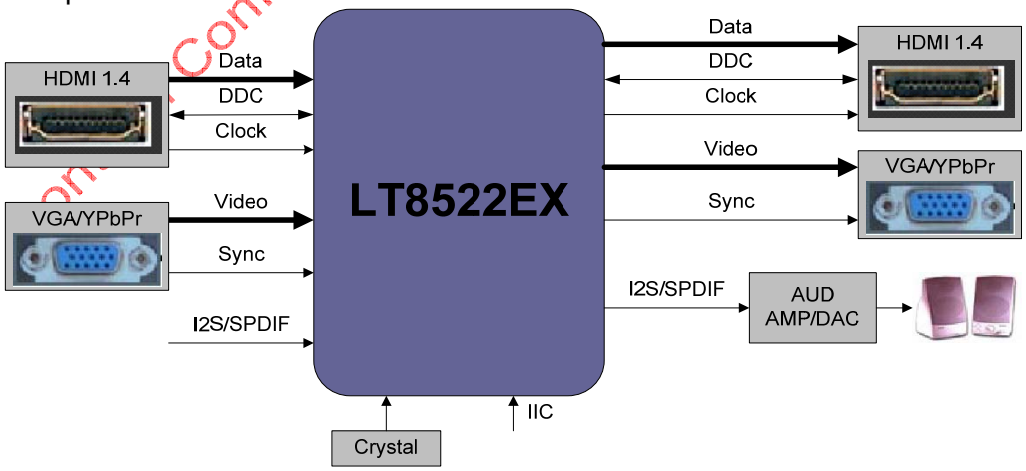


Figure 2: LCD Controller Application Diagram

2.2. Pin Configuration

Figure 3 is the pin diagram of the LT8522EX matrix switch chip.

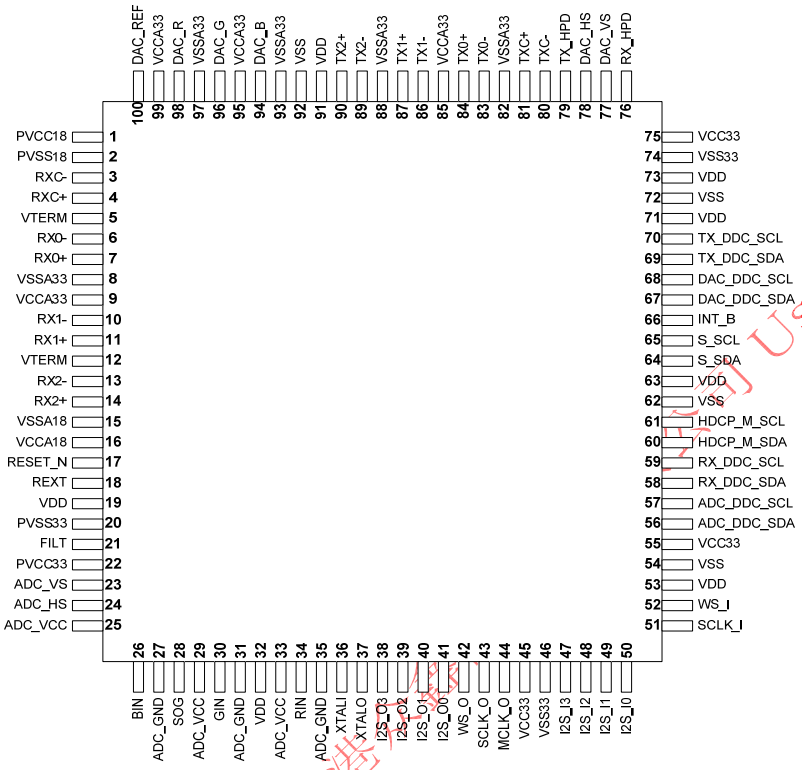


Figure 3: Pin Diagram

2.3. Pin Descriptions

(I/O description: A=Analog, I=Input, O=Output, P=Power, G=Ground)

PIN	NAME	I/O	FUNCTION	NOTES
HDMI RX Pins				
1	PVCC18	AP	Power supply pins for HDMI receiver PLL	1.8V
2	PVSS18	AG	Ground supply pins for HDMI receiver PLL	
3	RXC-	AI	HDMI receiver clock negative analog input	
4	RXC+	AI	HDMI receiver clock positive analog input	
5	VTERM	AP		3.3V
6	RX0-	AI	HDMI receiver channel 0 negative analog input	
7	RX0+	AI	HDMI receiver channel 0 positive analog input	
8	VSSA33	AG	3.3V ground supply pins for HDMI Receiver	
9	VCCA33	AP	3.3V power supply pins for HDMI Receiver	3.3V
10	RX1-	AI	HDMI receiver channel 1	

			negative analog input	
11	RX1+	AI	HDMI receiver channel 1 positive analog input	
12	VTERM	AP		3.3V
13	RX2-	AI	HDMI receiver channel 2 negative analog input	
14	RX2+	AI	HDMI receiver channel 2 positive analog input	
15	VSSA18	AG	1.8V ground supply pins for HDMI receiver	
16	VCCA18	AP	1.8V power supply pins for HDMI receiver	1.8V
Control Pins				
17	RESET_N	I	Global reset, active low	
18	REXT	AIO	Bandgap Reference resistor	6.04K
ADC And ADC PLL Pins				
19	VDD	AP	Digital power supply pins for ADC PLL and HDMI RX	1.8V
20	PVSS33	AG	Ground supply pins for ADC PLL	
21	FILT	AIO	ADC PLL external filter	
22	PVCC33	AP	Power supply pins for ADC PLL	3.3V
23	ADC_VS	I	VGA vertical sync input	5V-tolerant, internal pull-down
24	ADC_HS	I	VGA horizontal sync input	5V-tolerant, internal pull-down
25	ADC_VCC	AP	Power supply pins for ADC	1.8V
26	BIN	AI	VGA blue channel analog input	
27	ADC_GND	AG	Ground supply pins for ADC	
28	SOG	AI	SOG analog input	
29	ADC_VCC	AP	Power supply pins for ADC	1.8V
30	GIN	AI	VGA green channel analog input	
31	ADC_GND	AG	Ground supply pins for ADC	
32	VDD	AP	Digital power supply pins for ADC	1.8V
33	ADC_VCC	AP	Power supply pins for ADC	1.8V
34	RIN	AI	VGA red channel analog input	
35	ADC_GND	AG	Ground supply pins for ADC	
Crystal Pins				
36	XTALI	I	Crystal oscillator input	25MHZ
37	XTALO	O	Crystal oscillator output	
Audio Pins				
38	I2S_O3	O	I2S output	
39	I2S_O2	O	I2S output	
40	I2S_O1	O	I2S/SPDIF output	
41	I2S_O0	O	I2S output	
42	WS_O	O	I2S word select output	
43	SCLK_O	O	I2S serial clock output	
44	MCLK_O	O	I2S audio master clock output	
45	VCC33	P	Power supply pins for IO	3.3V

46	VSS33	G	Ground supply pins for IO	
47	I2S_I3	I	I2S input	
48	I2S_I2	I	I2S input	
49	I2S_I1	I	I2S/SPDIF input	
50	I2S_I0	I	I2S input	
51	SCLK_I	I	I2S serial clock input	For Slave mode
52	WS_I	I	I2S word select input	
53	VDD	P	Power supply pins for digital	1.8V
54	VSS	G	Ground supply pins for digital	
55	VCC33	P	Power supply pins for IO	3.3V
Control Pins				
56	ADC_DDC_SDA	IO	ADC DDC data channel	5V-tolerant, internal pull-up
57	ADC_DDC_SCL	IO	ADC DDC clock channel	5V-tolerant, internal pull-up
58	RX_DDC_SDA	IO	HDMI receiver DDC data channel	5V-tolerant, internal pull-up
59	RX_DDC_SCL	IO	HDMI receiver DDC clock channel	5V-tolerant, internal pull-up
60	HDCP_M_SDA	IO	Master I2C data channel	5V-tolerant
61	HDCP_M_SCL	IO	Master I2C clock channel	5V-tolerant
62	VSS	G	Ground supply pins for digital	
63	VDD	P	Power supply pins for digital	1.8V
64	S_SDA	IO	Slave I2C data channel	5V-tolerant
65	S_SCL	IO	Slave I2C clock channel	5V-tolerant
66	INT_B	O	Chip interrupt output, active low	
67	DAC_DDC_SDA	IO	DAC DDC data channel	5V-tolerant
68	DAC_DDC_SCL	IO	DAC DDC clock channel	5V-tolerant
69	TX_DDC_SDA	IO	HDMI transmitter DDC data channel	5V-tolerant, internal pull-up
70	TX_DDC_SCL	IO	HDMI transmitter DDC clock channel	5V-tolerant, internal pull-up
71	VDD	P	Power supply pins for digital	1.8V
72	VSS	G	Ground supply pins for digital	
73	VDD	P	Power supply pins for digital	1.8V
74	VSS33	G	Ground supply pins for IO	
75	VCC33	P	Power supply pins for IO	3.3V
76	RX_HPD	O	HDMI receiver hot plug detect output	5V-tolerant,
77	DAC_VS	O	VGA vertical sync output	
78	DAC_HS	O	VGA horizontal sync output	
79	TX_HPD	I	HDMI transmitter hot plug detect input	
HDMI TX Pins				
80	TXC-	AO	HDMI transmitter clock negative analog output	
81	TXC+	AO	HDMI transmitter clock positive analog output	
82	VSSA33	AG	3.3V ground supply pins for HDMI transmitter	
83	TX0-	AO	HDMI transmitter channel 0	

			negative analog output	
84	TX0+	AO	HDMI transmitter channel 0 positive analog output	
85	VCCA33	AP	3.3V power supply pins for HDMI transmitter	3.3V
86	TX1-	AO	HDMI transmitter channel 1 negative analog output	
87	TX1+	AO	HDMI transmitter channel 1 positive analog output	
88	VSSA33	AG	3.3V ground supply pins for HDMI transmitter	
89	TX2-	AO	HDMI transmitter channel 2 negative analog output	
90	TX2+	AO	HDMI transmitter channel 2 positive analog output	
91	VDD	P	HDMI transmitter/TX PLL Power supply	
92	VSS	G	HDMI transmitter/TX PLL Ground supply	
DAC Pins				
93	VSSA33	AG	3.3V ground supply pins for DAC	
94	DAC_B	AO	VGA blue channel analog output	
95	VCCA33	AP	3.3V power supply pins for DAC	3.3V
96	DAC_G	AO	VGA green channel analog output	
97	VSSA33	AG	3.3V ground supply pins for DAC	
98	DAC_R	AO	VGA red channel analog output	
99	VCCA33	AP	3.3V power supply pins for DAC	3.3V
100	DAC_REF	AI	DAC reference	

2.4. DC Specifications

Under normal operating conditions unless otherwise specified

HDMI to VGA

Symbol	Description	Conditions		Min	Typ	Max	Units
I_{CC}	Operating current	480P8bit	1.8V		62		mA
			3.3V		100		mA
		720P8bit	1.8V		85		mA
			3.3V		100		mA
		1080P8bit	1.8V		133		mA
			3.3V		100		mA

VGA to HDMI

Symbol	Description	Conditions		Min	Typ	Max	Units
I_{CC}	Operating current	640x480 8bit	1.8V		161		mA
			3.3V		94		mA
		720P 8bit	1.8V		183		mA
			3.3V		100		mA
		1080P 8bit	1.8V		216		mA
			3.3V		101		mA

VGA to HDMI , HDMI to VGA

Symbol	Description	Conditions		Min	Typ	Max	Units
I_{CC}	Operating current	1080P 8bit	1.8V		343		mA
			3.3V		202		mA

2.5. Typical Applications

Depend on the applications, it can have 2 different A/V sources: A HDMI receiver or A HDMI compatible Display Port reciever through Lontium's Level-shifter chipset or adding 500 ohm pull down resistor; A VGA reciever. Depend on the applications, it can have 2 different video output: A HDMI transmitter; A VGA transmitter. Audio output can be either SPDIF or I2S. Customers can add or delete some of the components/functions depends on the market they are trying to serve.

2.6. Major Function Block Descriptions

A functional block diagram is illustrated as Figure 1. Each of the functional units shown is described in the following sections.

2.7. VGA - ADC

The analog-to-digital converter (ADC) transfers the input analog R/G/B video signals to digital output data with each 8-bit resolution. The maximum clock sample frequency is 165M. RIN/GIN/BIN are high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.7V (p-p) full-scale. Signals should be AC-couple to these pins.

Please note that it is very important to follow the recommended layout guidelines for the circuit shown in the Figure 4.

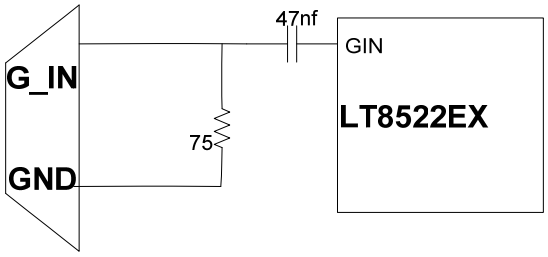


Figure 4: Example ADC Signal Terminations

2.7.1. Position Auto Adjust

Position auto adjust module is used to adjust the position of video picture vertically and horizontally. The module is made of two parts: RGB data start address counter part and position adjust part.

2.7.2. Sync Process

The LT8522EX has a sync processor block providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input timing.

Hsync /Vsync Frequency and Polarity Detection

SYNC_HCNT, the 16 bits hsync period counter counts the time of 32xhsync period, then loads the result into the SYNC_HCNT. The output value will be [((REFCLKfreq x 32)/Hfreq)], updated at posedge of vsync or negedge of vsync.

SYNC_VCNT, the 11 bits vsync period counter counts the counter of hsync pulse between two vsync pulses, then loads the result into the SYNC_VCNT. The output value will be [(VGA_V_TOTAL-1)], updated every vsync period.

The polarity functions detect the input hsync/vsync duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted.

2.7.3. Embedded HDMI Receiver

The embedded HDMI receiver is compliant with High Definition Multimedia Interface (HDMI) Specification 1.4. HDMI is unified digital video, audio, and control data over low-cost cables. LT8522EX HDMI RX can connect digital television, flat panel displays and project systems digitally to multimedia sources: DVD players, high definition set-top boxes, digital video tape recorders, and personal computers. Digital transmission, in turn, delivers an uncompromising multimedia experience. Inexpensive cables up to 20 meters and assure the widest range of interoperability against uncertain qualities of cheap cables from low-cost suppliers as the standard matures. The HDMI RX can receive and output up to eight digital audio channels at up to 192 kHz sampling rate, making it the leading component for integrated home theaters and high definition televisions. The device supports direct connections to a wide selection of audio DACs and decoders through industry standard I2S or S/PDIF interfaces.

HDMI RX Features:

- Single channel HDMI receiver
- Compliant with HDMI 1.4, and DVI 1.0 specifications
  - Supporting pixel rates from 13.5MHz to 300MHz
  - DTV resolutions: 480i, 576i, 480p, 576p, 720p, 1080i, 1080p up to 4kx2k
  - PC resolutions: VGA, SVGA, XGA, SXGA up to UXGA
- Video output interface supporting digital video standards such as:
  - 24-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces
- Intelligent adaptive channel equalization supporting up to 20m cable at the highest video data rate
- Digital audio output interface supporting
  - I2S interface supporting, audio sample rate: 32~192 kHz
  - sample size: 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio transmission

using IEC60958 and IEC 61937

- automatic audio error detection for programmable soft mute, preventing annoying harsh automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug

2.8. Digital Audio Input/Output Interface

Audio data is applied to the internal DAC filters via the digital audio interface. Four interface formats are supported:

- I^2S mode
- Right 16bit Justified mode
- Right 24bit Justified mode
- Left 24bit Justified mode

2.9. Two Wire Serial Bus Interface

The two wire serial bus interface is used to allow an external master to write control data, and read status from the LT8522EX registers. SCL is the serial clock and SDA is the serial data. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCL and SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCL is high.

The LT8522EX is operated as a bus slave device. The most significant 7-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master drives SDA from high to low, while SCL is high, this is defined to be a start condition (See Figure 21). All slaves on the bus listen to determine when a start condition has been asserted.

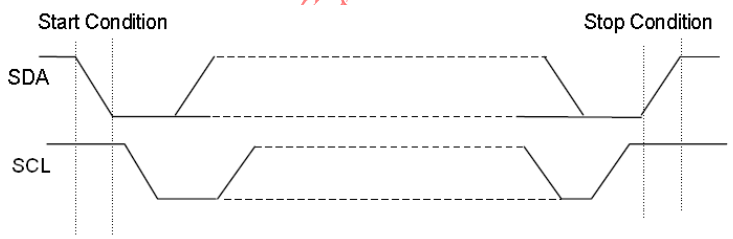


Figure 21: The Start And Stop Definition

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 22. (For the LT8522EX, the next byte is normally the index to the LT8522EX registers and is a write to the LT8522EX therefore the first R/W bit is normally low.)

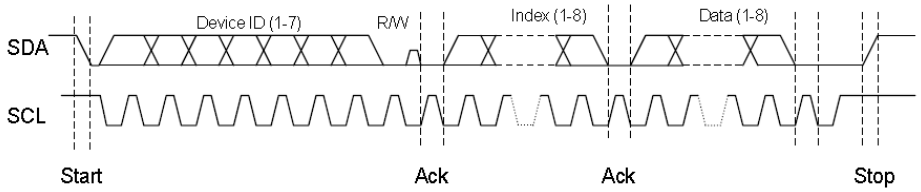


Figure 22: One Byte Write Operation

After transmitting the device address and the R/W bit, the master must release the SDA line while holding SCL low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theLT8522EX, the master sends another 8-bits of data, the LT8522EX loads this to the register pointed by the internal index register. The LT8522EX will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the LT8522EX if they are in ascending sequential order. After each 8-bit transfer the LT8522EX will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the LT8522EX the host will issue a stop condition.

A LT8522EX read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register (See Figure 23). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDA line and acknowledges the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDA is left high during a clock pulse) and issue a stop condition.

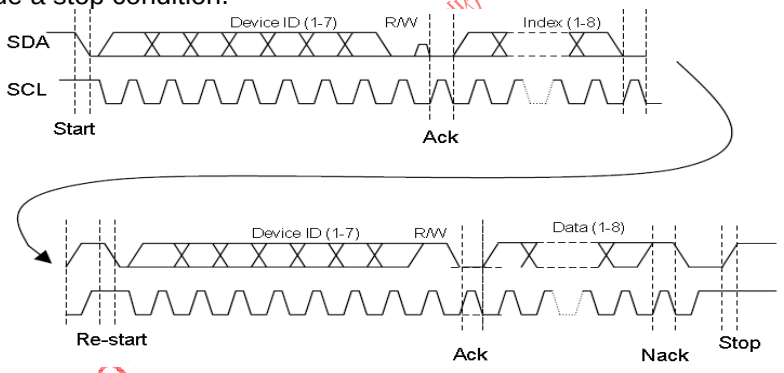


Figure 23: One Byte Read Operation

3. Packaging

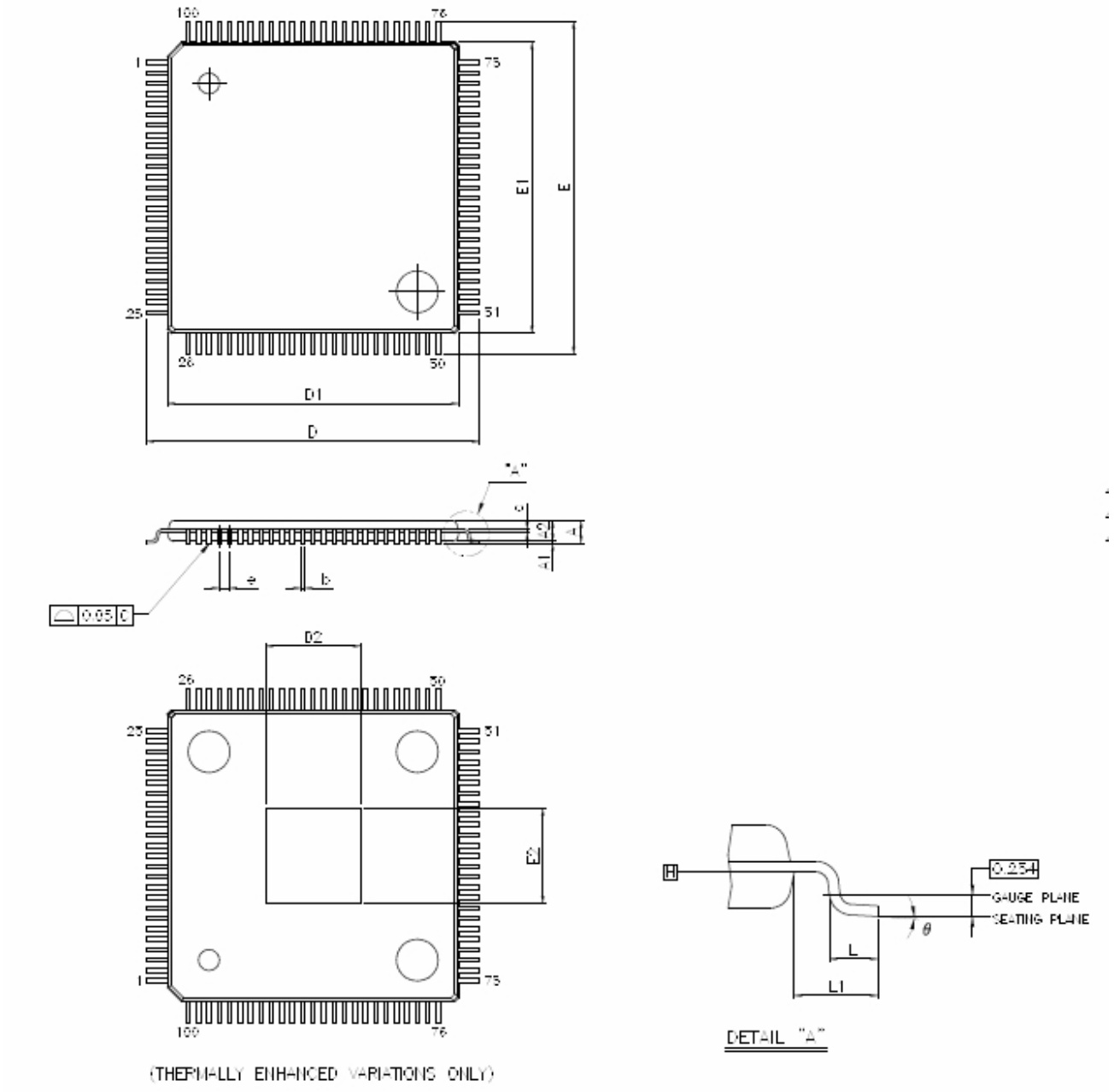
3.1. ePad Enhancement

The LT8522EX is packaged in a 100-pin TQFP package with ePad.

The ePad does not need to be soldered to the PCB. The information in the following paragraphs is provided for applications which choose to solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts. Dimensions T1 and T2 define the maximum limit of ePad size. Protrusions from the edges of the ePad may vary slightly from one package assembler to another, but all are confined to within these maximum dimensions.

3.2. Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.20
A1	0.05	--	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	0.127	0.16
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.50 BSC		
L	0.45	0.58	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
230X23E	5.64	5.84	5.64	5.84

References

Standards Documents

The abbreviations shown in column one of Table 1 is used elsewhere in this Application Note. Please contact the responsible standards bodies here for more information on these specifications.

HDMI High-Definition Multimedia Interface Specification Version 1.3a, November 2006.
HCTS High-Definition Multimedia Interface Compliance Test Specification Version 1.3a, November 2006.
HDCP High-bandwidth Digital Content Protection System Revision 1.3, December 2006.
VESA Proposed VESA and Industry Standards and Guidelines for Computer Display Monitor Timing Version 1.0, Revision 12p, Draft 3, October 2008.
CEA A DTV Profile for Uncompressed High Speed Digital Interfaces, July 2006.
DVI Digital Visual Interface, Revision 1.0, April 1999.
E-EDID Enhanced Extended Display Identification Data Standard, Revision 1, Feb 2000.
EDIDUG VESA EDID implementation Guide Version 1.0, June 2001.

These documents are available from the following standards groups:
ANSI/EIA/CEA Standards:
http://global.I.com, or by e-mail to global@I.com, or telephone at 800-854-7179.
VESA Standards:
http://www.vesa.org, or by telephone at 408-957-9270.
DVI Standard:
http://www.ddwg.org or by e-mail to ddwg.if@intel.com .
HDCP Standard:
http://www.digital-co.com or by e-mail to info@digital-cp.com .
HDMI Standard:
http://www.hdmi.org or by e-mail to admin@hdmi.org .

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