LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT86101SX HDMI/DVI Repeater

Data Sheet

We produce mixed-signal products for a better digital world!

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1.Revision History

Version	Date	Owner	Notes
1.0	04/07/2012	HF. Xia	Initial data sheet creation
1.1	05/21/2012	WJ.Liu	Update Package diagram
1.2	07/12/2014	DF.Zhou	Check package information
1.3	08/13/2014	N.Wang	Check package information

2. General Description

The LT86101SX is Lontium's 4th generation HDMI/DVI repeater based on ClearedEdge™ technology, compliant with the HDMI 1.4 (High Definition Multimedia Interface) specification. It is a 10.2Gbps (3 x 3.4Gbps) high performance re-clocking device that supports 3 TMDS data channels and a single clock channel. The device also integrates a bi-directional DDC active buffer and a parallel CEC active buffer to provide a complete HDMI/DVI repeater solution.

The LT86101SX incorporates an adaptive receive equalizer, a clock and data recovery (CDR) circuit and a de-emphasis driver on each TMDS data channel. The clock channel feeds a high-performance phase-locked loop (PLL) that regenerates a low jitter output clock. The receive equalizer analyzes the incoming data signal and automatically determines the amount of equalization to compensate the attenuation caused by long HDMI/DVI cables and FR4 traces. The CDR circuit retimes the equalized data, incorporated with PLL, to create clean clock and data outputs, reducing both deterministic and random jitter. This low level of output jitter provides system designers with extra margin and flexibility when working with stringent timing budget or long-cable applications. Also, several devices can be cascaded to extend cable reach without degrading signal fidelity. The transmitter supports configurable transmit de-emphasis so that the output can be optimized for driving additional lengths of cables or FR4 traces.

For better signal integrity, ODTs and calibration circuit are implemented in the receiver. Furthermore, offset existing on the receiver path can be automatically cancelled. The transmitter can operate at standard current level, or operate at 50% higher current level to support back-termination to achieve high return loss. This effectively improves the output signal quality due to impedance discontinuity.

The active DDC and CEC buffer bi-directionally restores signal integrity of DDC and CEC buses. The DDC buffer features compensation for cable capacitance with a range from 300pF to 3000pF on source side, and from 150pF to 1500pF on sink side. The slew-rate-limited driver prevents DDC bus from ringing and mutual coupling. The DDC buffer has parallel and serial mode. In serial mode, it isolates capacitances of source side and sink side, with the limitation of uncascadable characteristic. While in parallel mode, the buffer can be cascaded, but total capacitive loading also can be seen by both source device and sink device. Besides, the buffer can de-skew the two bus-line delays to compensate or adjust the marginal timing due to unbalanced propagation paths or bad I2C master behavior. The CEC buffer has only parallel mode because of the requirement of CEC line connectivity specification. It provides 3000pF drive capability, and compliant with CEC line degradation off-leakage specification when the chip is in the power off state.

Dual control modes are available for LT86101SX. This provides system designers with very flexible solutions, for consideration of either performance or cost. The LT86101SX supports two control modes: Pin Control Mode and I2C Control Mode. In Pin Control Mode, no external MCU is needed, and the basic functions are under control of pin configurations, however advanced functions are at default settings. In I2C Control Mode, an external MCU is required, and the chip is fully controlled by MCU while the control pin configurations are not valid any more.

The LT86101SX is offered in a 7mm x 7mm 48-lead QFN package, and operates over a 0°C to +70°C temperature range.

2.1 FEATURES

- Compatible with HDMI 1.4, supports 3.4Gbps data rate
- Supports 3D video formats and 4Kx2K extended resolution formats
- Adaptive receive equalization up to 40dB to compensate for long/cheap cable losses
- ODTs and calibration for better signal integrity
- Separate ODT supply for AC-coupled applications
- Configurable transmit de-emphasis up to -9dB to pre-compensate signal distortion
- Integrated back-termination to improve output signal quality
- 5V-tolerant active DDC buffer allowing capacitance up to 3000pF
- Parallel active CEC buffer with drive capability up to 3000pF
- Extends cable length as follows: (RX-side + TX-side)
  - Up to (55m + 20m) over 26 AWG STP HDMI cable @ 1.65Gbps
  - Up to (35m + 20m) over 26 AWG STP HDMI cable @ 2.25Gbps
  - Up to (25m + 15m) over 28 AWG STP HDMI cable @ 1.65Gbps
  - Up to (15m + 10m) over 28 AWG STP HDMI cable @ 2.25Gbps
- Cascadable for further cable reach
- Dual control modes for flexible applications
- Link activity detection to enable squelch option
- Power dissipation of 0.75W typical
- ESD rating: HBM at ±6kV
- 7mm x 7mm 48-pin QFN lead-free package

2.2 APPLICATIONS

- TMDS cable equalizer
- HD televisions and displays
- DVI/HDMI cable-extender modules
- Cable assemblies

2.3 ABSOLUTE MAXIMUM RATINGS

Supply Voltage: V_{BUS} ..... -0.5V to +6.0V
Supply Voltage: VCCA33, VTERM ..... -0.5V to +4.0V
Supply Voltage: VCCA18, VCCP18, VDD18 ..... -0.5V to +2.2V
Voltage at Normal I/O Pins ..... -0.5V to +4.0V
Voltage at 5V-Tolerant I/O Pins ..... -0.5V to +6.0V
Voltage between any CML I/O Complementary Pair ..... ±3.3V
Operating Junction Temperature Range ..... -55°C to +150°C
Storage Temperature Range ..... -55°C to +150°C

2.4 ELECTRICAL CHARACTERISTICS

(VBUS = +4.5V to +5.5V, VCCA33 = +3.0V to +3.6V, VTERM = +3.15V to +3.45V, VCCA18 = +1.6V to +2.0V, VCCP18 = +1.6V to +2.0V, VDD18 = +1.6V to +2.0V, T_A = 0°C to +70°C. Typical Values are at VBUS = +5.0V, VCCA33 = +3.3V, VTERM = +3.3V,

VCCA18 = +1.8V, VCCP18 = +1.8V, VDD18 = +1.8V, external terminations = 50 ±1%, TMDS rate = 250Mbps to 3.4Gbps, TA = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply						
Supply Voltage	VBUS	Normal Operation	4.5	5.0	5.5	V
	VCCA33	Normal Operation	3.0	3.3	3.6	V
	VTERM	Normal Operation, DC-Coupling	3.15	3.3	3.45	V
		Normal Operation, AC-Coupling	1.7	1.8	1.9	V
	VCCA18	Normal Operation	1.6	1.8	2.0	V
	VCCP18	Normal Operation	1.6	1.8	2.0	V
	VDD18	Normal Operation	1.6	1.8	2.0	V
Supply Current	IVBUS	Normal Operation			10	mA
	IVCCA33	Normal Operation			35	mA
		Power Down			10	mA
	IVTERM	Normal Operation			40	mA
		Power Down			10	mA
	IVCCA18	Normal Operation			40	mA
		Power Down			10	mA
	IVCCP18	Normal Operation			40	mA
		Power Down			10	mA
	IVDD18	Normal Operation			40	mA
		Power Down			10	mA
CML Inputs (Source Side)						
Differential Input Voltage Swing	VID		600	1000	1400	mVP-P
Common-Mode Input Voltage	VICM		VTERM -0.5	VTERM	VTERM +0.1	V
Input Resistance	RI	Single-ended	45	50	55	

CML Outputs (Sink Side)				
Standby Output Voltage	VOFF	Power Down	VTERM VTERM -10 +10	mV
Differential Output-Voltage Swing	VOD	50 Load	800 1000 1200	mVP-P
Output-Voltage High	VODH	Single-Ended	VTERM	V
Output-Voltage Low	VODL	Single-Ended	VTERM VTERM -0.6 -0.4	V
Common-Mode Output Voltage	VOCM	50 Load	VTERM -0.25	V
Rise/Fall Time	TR /TF	20% ~ 80%	80 130 200	ps
LVTTL Inputs				
LVTTL Input High Voltage	VIH		2.0	V
LVTTL Input Low Voltage	VIL		0.8	V
LVTTL Outputs				
LVTTL Output High Voltage	VOH		2.4	V
LVTTL Output Low Voltage	VOL		0.4	V
DDC Buffer I/O (5V-Tolerant)				
DDC Input High Voltage	VIHDDC		4.4	V
DDC Input Low Voltage	VILDDC		0.5	V
DDC Output High Voltage (Open-Drain)	VOHDDC	RLOAD = 2kΩ to VBUS	4.0	V
DDC Output Low Voltage (Open-Drain)	VOLDDC	RLOAD = 2kΩ to VBUS	1.0	V
DDC Bus Rise Time	TRDDC	20% ~ 80%, RLOAD = 2kΩ to VBUS, CLOAD = 3000pF to ground	1000	ns
DDC Bus Fall Time	TFDDC	80% ~ 20%, RLOAD = 2kΩ to VBUS, CLOAD = 3000pF to ground	300	ns
CEC Buffer I/O				
CEC Input High Voltage	VIHCEC		2.9 3.6	V
CEC Input Low	VILCEC		0	V

Voltage			0.4	
CEC Output High Voltage (Open-Drain)	VOHCEC	RLOAD = 27kΩ to 3.3V via a diode	3.0	V
CEC Output Low Voltage (Open-Drain)	VOLCEC	RLOAD = 27kΩ to 3.3V via a diode	0.3	V
CEC Bus Rise Time	TRCEC	10% ~ 90%, RLOAD = 27kΩ to 3.3V via a diode, CLOAD = 3000pF to ground	250	us
CEC Bus Fall Time	TFCEC	90% ~ 10%, RLOAD = 27kΩ to 3.3V via a diode, CLOAD = 3000pF to ground	50	us
CEC Off-Leakage Current	IOFFCEC	RLOAD = 27kΩ to 3.3V via a diode	1.8	uA
I2C Configuration I/O				
I2C Input High Voltage	VIHI2C		2.0	V
I2C Input Low Voltage	VILI2C		0.8	V
I2C Output Low Voltage (Open-Drain)	VOLI2C	RLOAD = 4.7kΩ to 3.3V	0.4	V
Analog Configuration Inputs				
Analog Input Voltage Range	VIA		0 3.3	V

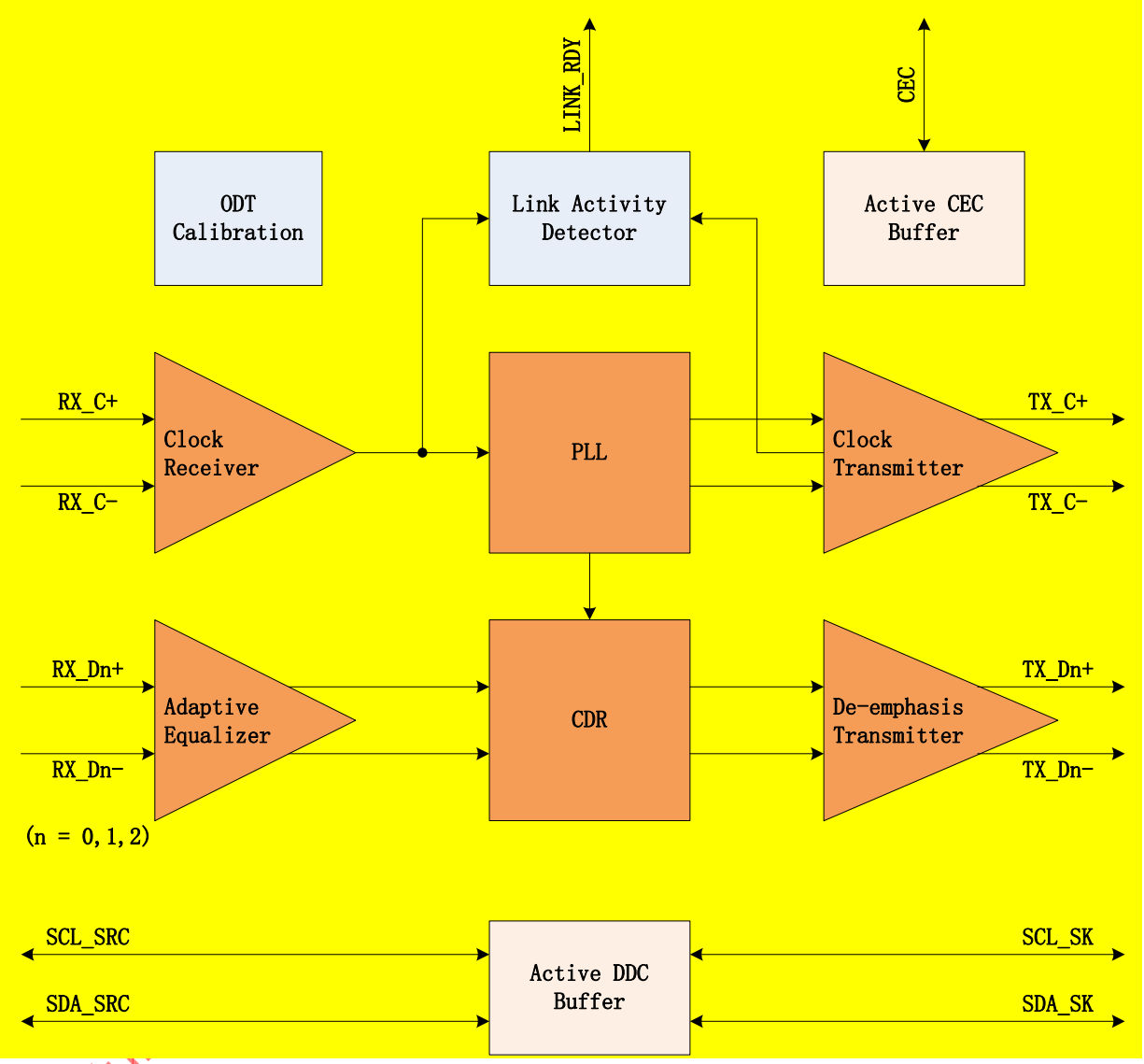
DC Specifications

Under normal operating conditions unless otherwise specified

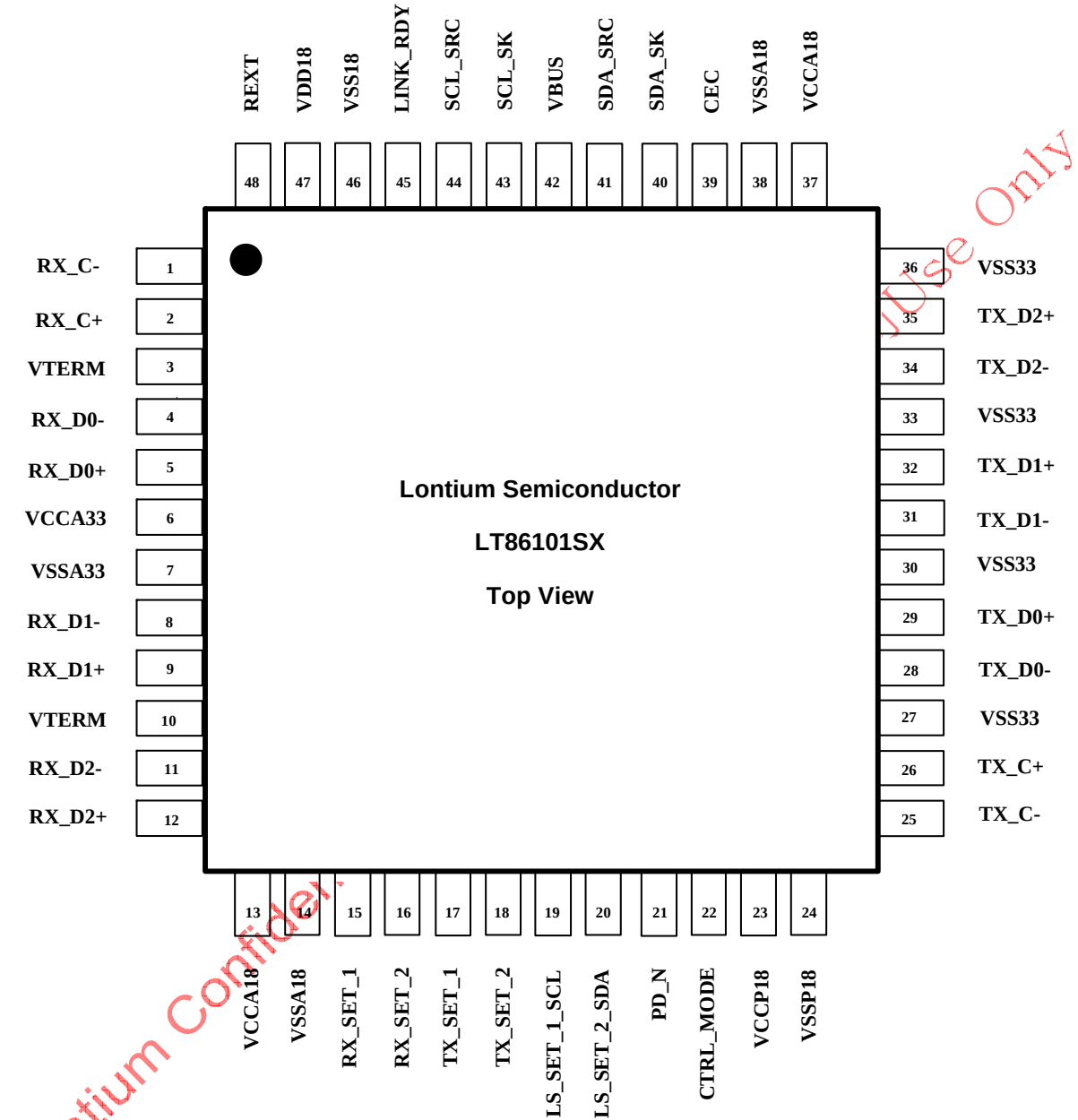
Symbol	Description	Min	Typ	Max	Units
I	3.3V	40	45	50	mA
	1.8V	90	100	110	mA

3. Function Description

3.1 FUNCTION BLOCK DIAGRAM



3.2 PIN CONFIGURATION



3.3 PIN DESCRIPTIONS

Symbol	Number	Type	Description
CML Input and Output Signals			
RX_C-	1	CML	Negative Clock Input
RX_C+	2	CML	Positive Clock Input
RX_D0-	4	CML	Negative Data Input
RX_D0+	5	CML	Positive Data Input
RX_D1-	8	CML	Negative Data Input
RX_D1+	9	CML	Positive Data Input
RX_D2-	11	CML	Negative Data Input
RX_D2+	12	CML	Positive Data Input
TX_C-	25	CML	Negative Clock Output
TX_C+	26	CML	Positive Clock Output
TX_D0-	28	CML	Negative Data Output
TX_D0+	29	CML	Positive Data Output
TX_D1-	31	CML	Negative Data Output
TX_D1+	32	CML	Positive Data Output
TX_D2-	34	CML	Negative Data Output
TX_D2+	35	CML	Positive Data Output

CEC Signal			
CEC	39	CEC I/O	Parallel Active CEC Buffer I/O. External 27k pull-up to 3.3V via a diode needed.
DDC Signals			
SDA_SK	40	DDC I/O	DDC Sink-Side Data I/O, 5V-Tolerant. External pull-up to VBUS needed.
SDA_SRC	41	DDC I/O	DDC Source-Side Data I/O, 5V-Tolerant. External pull-up to VBUS needed.
SCL_SK	43	DDC I/O	DDC Sink-Side Clock I/O, 5V-Tolerant. External pull-up to VBUS needed.
SCL_SRC	44	DDC I/O	DDC Source-Side Clock I/O, 5V-Tolerant. External pull-up to VBUS needed.
Control/Status Signals			
RX_SET_1	15	Analog	RX Setting Input #1. For function description, see table below. Only valid in Pin Control Mode.
RX_SET_2	16	Analog	RX Setting Input #2. For function description, see table below. Only valid in Pin Control Mode.
TX_SET_1	17	Analog	TX Setting Input #1. For function description, see table below. Only valid in Pin Control Mode.
TX_SET_2	18	Analog	TX Setting Input #2. For function description, see table below. Only valid in Pin Control Mode.
LS_SET_1_SCL	19	Analog/ I2C I/O	In Pin Control Mode, this pin is used as analog configuration pin (Low Speed Blocks Setting Input #1. For function description, see table below). And It is used as I2C SCL pin in I2C Control Mode. External pull-up to 3.3V needed.
LS_SET_2_SDA	20	Analog/ I2C I/O	In Pin Control Mode, this pin is used as analog configuration pin (Low Speed Blocks Setting Input #2. For function description, see table below). And It is used as I2C SDA pin in I2C Control Mode. External pull-up to 3.3V needed.
PD_N	21	LVTTL	Power-Down Input. This input allows the chip to be powered down to conserve power (except ODT Calibration, Clock Receiver, Link Activity Detector and Active DDC Buffer).

			HIGH = Normal Operation; LOW = Powered Down. Only valid in Pin Control Mode. Pulled high internally by a 100k resistor.
CTRL_MODE	22	LVTTL	Control Mode Input. HIGH = I2C Control Mode; LOW = Pin Control Mode (I2C being reset). Pulled down internally by a 100k resistor.
LINK_RDY	45	LVTTL	Link Ready Output. This pin asserts HIGH upon detection of the input TMDS clock on the upstream link and presence of the output active termination on the downstream link.
Miscellaneous			
VTERM	3, 10	Termination Supply	DC-Coupled Application: 3.3V±5%; AC-Coupled Application: 1.8V±5%.
VCCA33	6	Analog Supply	3.3V±10%
VSSA33	7	Analog Ground	Analog Ground Pin
VCCA18	13, 37	Analog Supply	1.8V±10%
VSSA18	14, 38	Analog Ground	Analog Ground Pins
VCCP18	23	PLL Supply	1.8V±10%
VSSP18	24	PLL Supply	PLL Ground Pin
VSS33	27, 30, 33, 36	Analog Ground	Transmitter Ground Pins
VBUS	42	DDC BUS Supply	DC-Coupled Application: 5V±10%; AC-Coupled Application: 3.3V±10%. In DC-coupled applications, VBUS may also be 3.3V±10%, but the rise time of DDC bus lines would increased. For the best performance of DDC buffer, 5V±10% supply is recommended.

VSS18	46	Digital Ground	Digital Ground Pin
VDD18	47	Digital Supply	1.8V±10%
REXT	48	Analog I/O	Current sense port used to provide an accurate current reference for the ODT calibration and bias circuits. Connecting this pin through a 2k resistor (±1%) to VSSA33 is recommended.

Configuration for analog control pin RX_SET_1:

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095 mV ≦ VIA ≦ 3300 mV
RX DFE	3'b000 (disable)	3'b001 (100uA)	3'b010 (200uA)	3'b011 (300uA)	3'b100 (400uA)	3'b101 (500uA)	3'b110 (600uA)	3'b111 (700uA)

Configuration for analog control pin RX_SET_2:

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095mV ≦ VIA ≦ 3300mV
ODT Calibration	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)
RX EQ Stage 2	4'b0000 (disconnect all resistors)	4'b0000 (disconnect all resistors)	4'b1111 (connect all resistors)	4'b1111 (connect all resistors)	4'b0000 (disconnect all resistors)	4'b0000 (disconnect all resistors)	4'b1111 (connect all resistors)	4'b1111 (connect all resistors)
PLL Buffer Current	2'b10 (900uA)	2'b11 (1200uA)	2'b10 (900uA)	2'b11 (1200uA)	2'b10 (900uA)	2'b11 (1200uA)	2'b10 (900uA)	2'b11 (1200uA)
PI Mixer	2'b10	2'b11	2'b10	2'b11	2'b10	2'b11	2'b10	2'b11

Current	(40uA)	(60uA)	(40uA)	(60uA)	(40uA)	(60uA)	(40uA)	(60uA)
DCC Current	2'b10 (20uA)	2'b11 (30uA)	2'b10 (20uA)	2'b11 (30uA)	2'b10 (20uA)	2'b11 (30uA)	2'b10 (20uA)	2'b11 (30uA)

Configuration for analog control pin TX_SET_1:

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095mV ≦ VIA ≦ 3300mV
1.5X Drive Current	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)
Back-Termination	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b1 (enable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)	1'b0 (disable)
De-emphasis Logic Tap 2	1'b0 (disable)	1'b0 (disable)	1'b1 (enable)	1'b1 (enable)	1'b0 (disable)	1'b0 (disable)	1'b1 (enable)	1'b1 (enable)
De-emphasis Driver Tap 2	1'b0 (disable)	1'b0 (disable)	1'b1 (enable)	1'b1 (enable)	1'b0 (disable)	1'b0 (disable)	1'b1 (enable)	1'b1 (enable)
De-emphasis Logic Tap 2 Reversion	1'b0 (positive polarity)	1'b1 (negative polarity)	1'b0 (positive polarity)	1'b1 (negative polarity)	1'b0 (positive polarity)	1'b1 (negative polarity)	1'b0 (positive polarity)	1'b1 (negative polarity)

Configuration for analog control pin TX_SET_2:

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095mV ≦ VIA ≦ 3300mV
Main Driver Swing	7'h60 (500mV)	7'h60 (500mV)	7'h60 (500mV)	7'h60 (500mV)	7'h74 (600mV)	7'h74 (600mV)	7'h74 (600mV)	7'h74 (600mV)
De-emphasis Driver Tap 1 Swing	6'h20 (100mV)	6'h20 (100mV)	6'h32 (150mV)	6'h32 (150mV)	6'h20 (100mV)	6'h20 (100mV)	6'h32 (150mV)	6'h32 (150mV)
De-emphasi	6'h20 (32mV)	6'h32 (50mV)	6'h20 (32mV)	6'h32 (50mV)	6'h20 (32mV)	6'h32 (50mV)	6'h20 (32mV)	6'h32 (50mV)

s Driver Tap 2 Swing								

Configuration for analog control pin LS_SET_1_SCL: (Pin Control Mode)

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095mV ≦ VIA ≦ 3300mV
DDC Buffer High-to-Low Threshold	2'b01 (3.94V)	2'b01 (3.94V)	2'b01 (3.94V)	2'b01 (3.94V)	2'b00 (3.79V)	2'b00 (3.79V)	2'b00 (3.79V)	2'b00 (3.79V)
DDC Buffer Low-to-High Threshold	2'b10 (1.06V)	2'b10 (1.06V)	2'b11 (1.21V)	2'b11 (1.21V)	2'b10 (1.06V)	2'b10 (1.06V)	2'b11 (1.21V)	2'b11 (1.21V)
DDC Buffer Output-Low Holding Voltage	2'b01 (0.80V)	2'b01 (0.80V)	2'b10 (0.90V)	2'b10 (0.90V)	2'b01 (0.80V)	2'b01 (0.80V)	2'b10 (0.90V)	2'b10 (0.90V)
DDC Buffer Input-Low Threshold	2'b01 (0.61V)	2'b01 (0.61V)	2'b10 (0.76V)	2'b10 (0.76V)	2'b01 (0.61V)	2'b01 (0.61V)	2'b10 (0.76V)	2'b10 (0.76V)
LPF on SCL_SRC	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)
LPF on SCL_SK	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)	4'b0010 (100ns filtering)	4'b0001 (bypassed)
LPF on SDA_SRC	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)
LPF on SDA_SK	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)	4'b0100 (200ns filtering)	4'b0001 (bypassed)

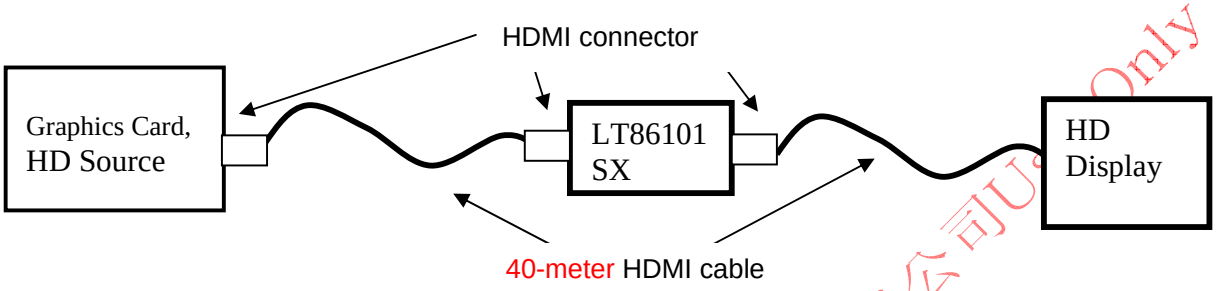
Configuration for analog control pin LS_SET_2_SDA: (Pin Control Mode)

	Analog Input Voltage Range							
	0mV ≦ VIA < 620mV	620mV ≦ VIA < 1030mV	1030mV ≦ VIA < 1445mV	1445mV ≦ VIA < 1855mV	1855mV ≦ VIA < 2270mV	2270mV ≦ VIA < 2680mV	2680mV ≦ VIA < 3095mV	3095mV ≦ VIA ≦ 3300mV
DDC Buffer Pull-Down Strength on SCL	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b1 (low)	1'b1 (low)	1'b1 (low)	1'b1 (low)
DDC Buffer Pull-Up Strength on SCL	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b1 (low)	1'b1 (low)	1'b1 (low)	1'b1 (low)
DDC Buffer Pull-Down Strength on SDA	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b1 (low)	1'b1 (low)	1'b1 (low)	1'b1 (low)
DDC Buffer Pull-Up Strength on SDA	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b0 (high)	1'b1 (low)	1'b1 (low)	1'b1 (low)	1'b1 (low)
CEC Buffer High-to-Low Threshold	2'b01 (2.6V)	2'b01 (2.6V)	2'b10 (2.7V)	2'b10 (2.7V)	2'b01 (2.6V)	2'b01 (2.6V)	2'b10 (2.7V)	2'b10 (2.7V)
CEC Buffer Low-to-High Threshold	2'b01 (0.6V)	2'b01 (0.6V)	2'b10 (0.7V)	2'b10 (0.7V)	2'b01 (0.6V)	2'b01 (0.6V)	2'b10 (0.7V)	2'b10 (0.7V)
CEC Bus Positive Deglitch on Pull-Down Path	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)
CEC Bus Positive	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)	4'b0010 (300~600ns)	4'b0001 (bypassed)

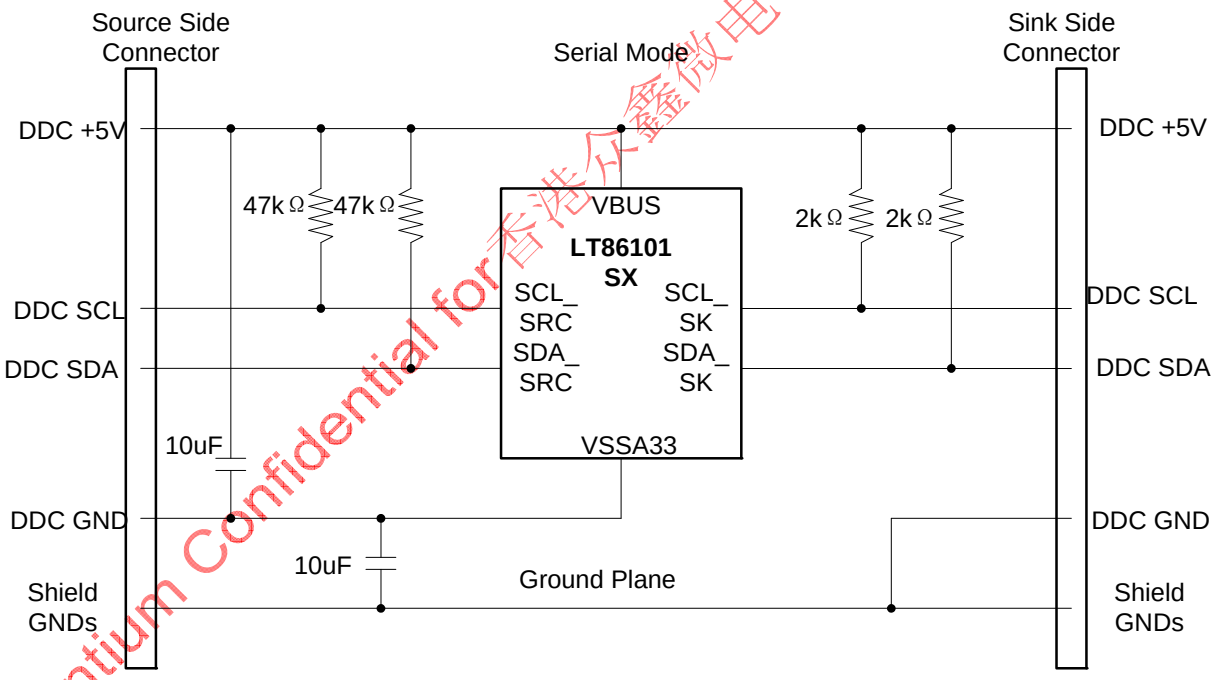
Deglitch on Pull-Up Path								
CEC Bus Negative Deglitch on Pull-Down Path	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)
CEC Bus Negative Deglitch on Pull-Up Path	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)	4’b0010 (1~2us)	4’b0001 (bypassed)

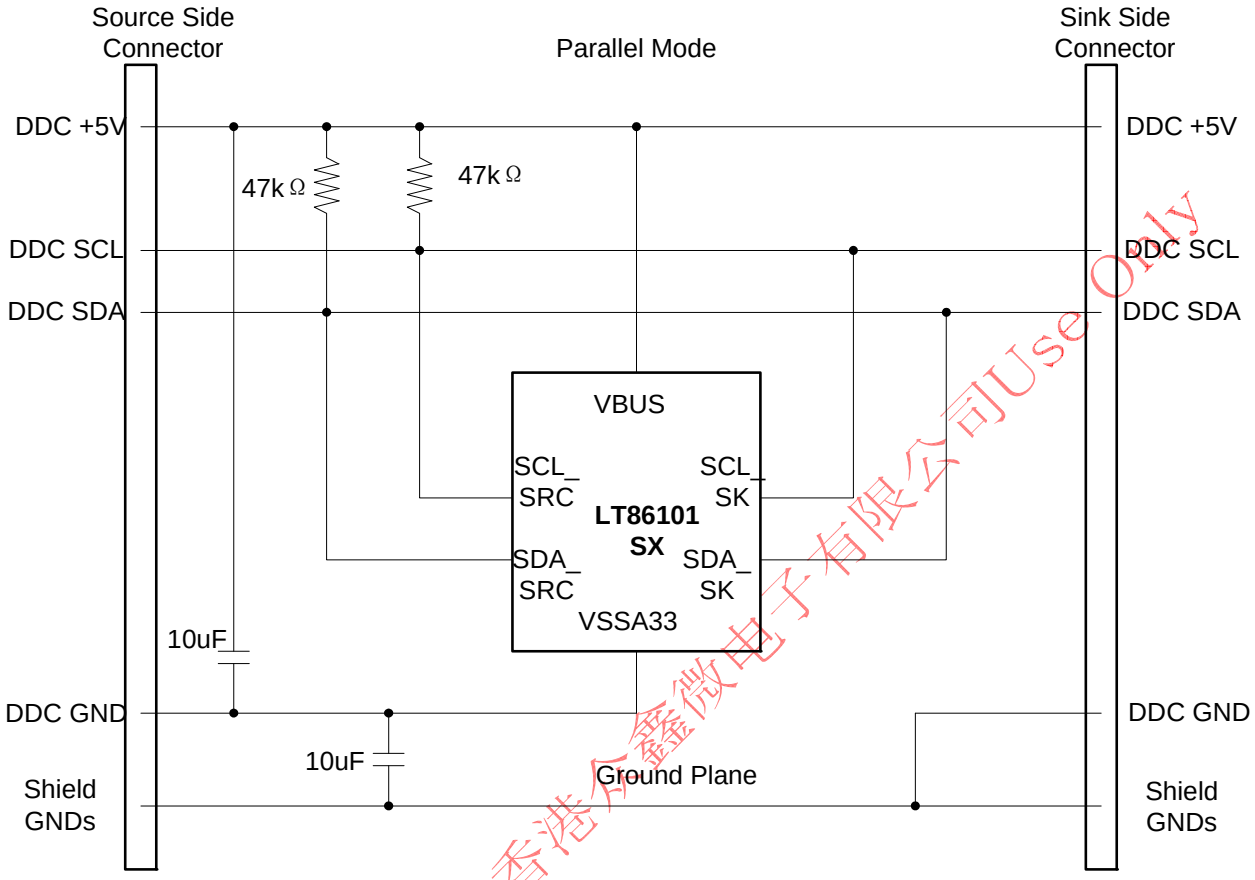
3.4 TYPICAL APPLICATIONS

The following picture shows the typical application of LT86101SX, it can sit on a HD Display board or sit on a stand alone circuit board for repeating the TMDS signal or extending the TMDS cable reach. It provides a complete solution for transmitting HDMI compliant digital video/ audio signals.

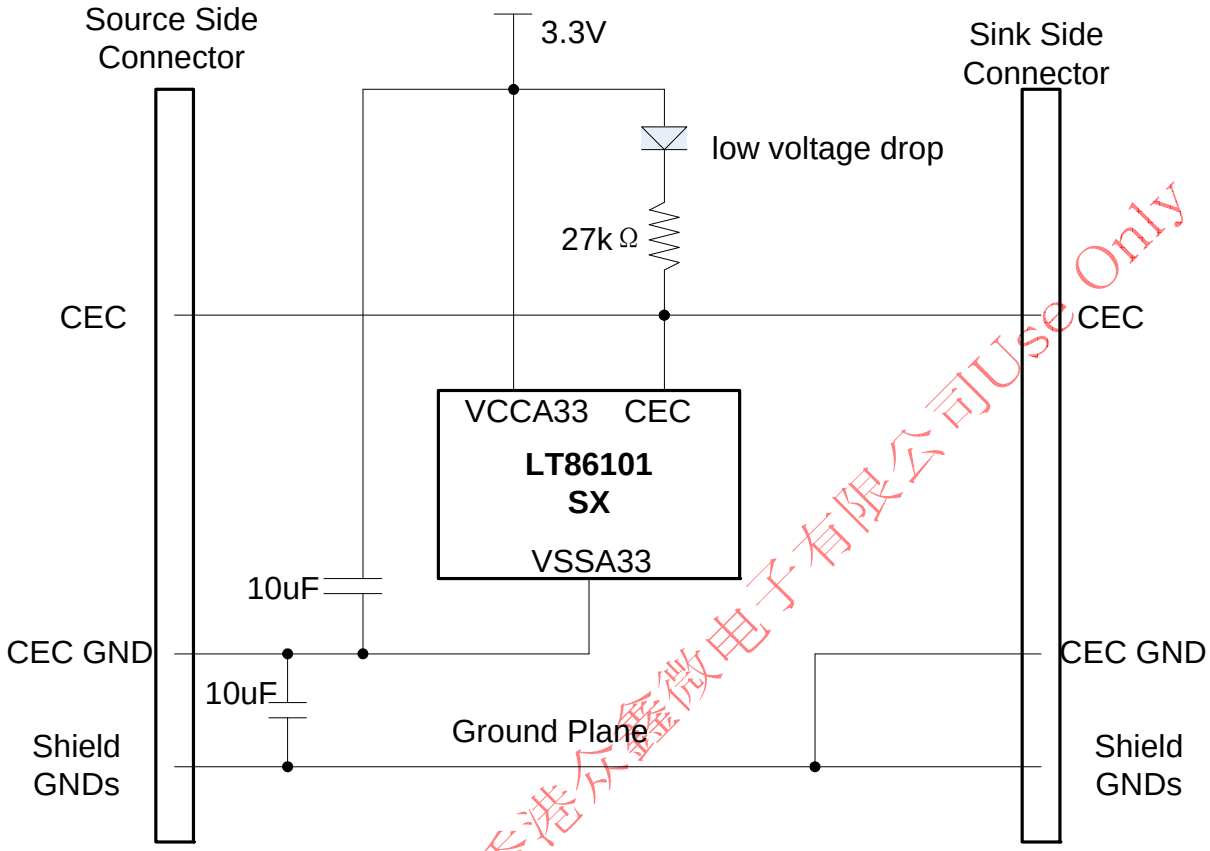


For DDC buffer, it has two application modes, shown as figures below. Serial mode DDC buffer isolates capacitance on source side and sink side but can not be cascaded, while parallel device can, with the disadvantage of non-isolation.





The CEC buffer has only parallel mode to meet CEC line connectivity specification. The typical application is shown as following figure.



4. Packaging

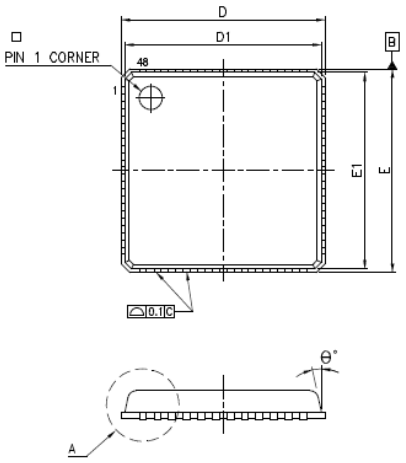
4.1 ePad ENHANCEMENT

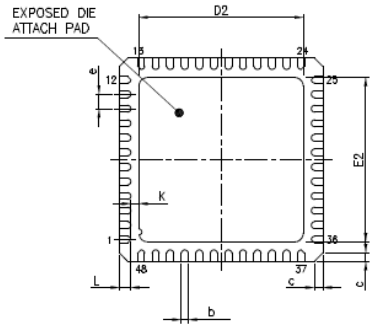
The LT86101SX is packaged in a 48-pin QFN package with ePad. The ePad dimensions is 3.7*3.7mm shown in the following figure.

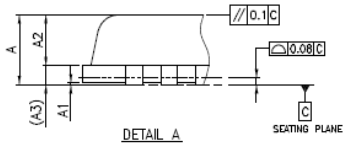
The ePad does not need to be soldered to the PCB. The information in the following paragraphs is provided for applications which choose to solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

4.2 PACKAGE DIMENSIONS







SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2		0.65 REF.	
A3		0.203 REF.	
b	0.18	0.25	0.30
c	0.24	0.42	0.60
D	6.90	7.00	7.10
D1	6.65	6.75	6.85
E	6.90	7.00	7.10
E1	6.65	6.75	6.85
e		0.50 BSC.	
K	0.20	–	–
L	0.30	0.40	0.50
θ°	0.00	–	12.00

UNIT : mm

PAD SIZE	D2			E2			MEET JEDEC OUTLINE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
138X138MIL	2.90	3.10	3.30	2.90	3.10	3.30	YES
157X157MIL	3.50	3.70	3.90	3.50	3.70	3.90	YES
208X208MIL	4.90	5.10	5.30	4.90	5.10	5.30	YES
213X213MIL	5.00	5.20	5.40	5.00	5.20	5.40	YES
220X220MIL	5.30	5.50	5.70	5.30	5.50	5.70	NO

UNIT : mm

NOTES :
1. JEDEC : MO-220 VKKD-2.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION "b" APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. THE PIN #1 IDENTIFIER EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. DIMENSION "A1" APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

References

Standards Documents

The abbreviations shown in column one of table below is used elsewhere in this data sheet. Please contact the responsible standards bodies here for more information on these specifications.

HDMI	*High Definition Multimedia Interface*, Revision 1.1, HDMI Consortium; March 2004.
HCTS	*HDMI Compliance Test Specification*, Revision 1.1, HDMI Consortium, Junu 2004.
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.1, Digital-CP, LLP; June 2003.
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999.
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000.
EDIDUG	*VESA EDID Implementation Guide*, VESA; March 2001.
CEA861	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA; January 2001.
CEA861B	*A DTV Profile For Uncomp. High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002.
EDDC	*Enhanced Display Data Channel Standard*, Version 1, VESA; September 1999.

These documents are available from the following standards groups:

ANSI/EIA/CEA Standards:

http://global.I.com or by e-mail to global@I.com, or telephone at 800-854-7179.

VESA Standards:

http://www.vesa.org or by telephone at 408-957-9270.

DVI Standard:

http://www.ddwg.org or by e-mail to ddwg.if@intel.com.

HDCP Standard:

http://www.digital-co.com or by e-mail to info@digital-cp.com.

HDMI Standard:

http://www.hdmi.org or by e-mail to admin@hdmi.org.

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