LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT8619C

HDMI to TTL/LVDS Converter

Datasheet

1. Features

- **HDMI/Dual-mode DP Input Interface**
  - Compliance with DVI V1.0 and HDMI V1.4
  - Support up to 1.65Gbps for DVI
  - Support up to 3.4Gbps for HDMI
  - Support resolution up to 4Kx2K@30Hz for HDMI
  - Support 8/10/12 bit per component (bpc)
  - Support CEC
  - Support HDCP1.4 decryption
  - Support On-chip EDID
  - Receiver side equalization up to 25 dB
- **LVDS Output Interface**
  - Compatible with VESA and JEIDA standard
  - 1~2 configurable port
  - Support port swap
  - Support maximum data rate 1.05Gb/s/lane
  - Resolution up to 4Kx2K@30Hz
  - Supports 6-bit, 8-bit output
- **TTL Output Interface**
  - Support up to 24-bit RGB or BT656/BT1120 output
  - Support both SDR and DDR output
  - Support up to 148.5MHz DDR or 300MHz SDR clock output
  - Support both 1.8V and 3.3V output voltage level
- **Video and Audio Processing**
  - Programmable color space conversion
  - Advanced dithering logic for 6-bit color depth output
  - Optional SPDIF output and 8-channel I2S output
- **Miscellaneous**
  - Support 100KHz and 400KHz I2C slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40°C to +85°C
  - Packaged in QFN76 9mm x 9mm

2. General Description

The Lontium's LT8619C is a high performance HDMI/Dual-mode DP receiver chip, compliant with the HDMI 1.4 specification. The TTL output can support RGB, BT656, BT1120 and the output resolution can support up to 4Kx2K@30Hz.

For easy implement of a multi-media system, LT8619C supports 8-channel high quality I2S audio or SPDIF audio output.

3. Applications

- Car Entertainment
- Pico Projector
- Smart Projector

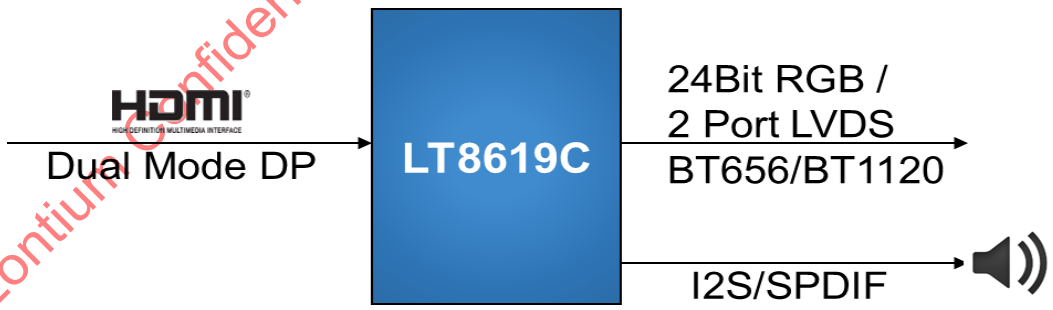

Figure 3.1 Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Product Version	Product Status	Operating Temperature Range	Package	Packing Method
LT8619C	U3	NRND	−40°C to +85°C	QFN76(9*9)	Tray
LT8619C	U5	RND	−40°C to +85°C	QFN76(9*9)	Tray

NRND: Not Recommended for New Designs.
RND: Recommended for New Designs.

Table 4.2 Product Version Information

Product Version	Information	Note
U3	1. Pin 56 is used as PCLK which can only be used in the applications where PCLK is below 150MHz. For PCLK above 150MHz, U5 is recommended. 2. Dual-port LVDS output is not recommended.	
U5	1. Both pin 56 and pin 68 can be used as PCLK. However pin 56 is of inferior performance above 150MHz and can only be used below 150MHz. Pin 68 has better performance above 150MHz, and it should be used whenever possible, whether the PCLK is below or above 150MHz. 2. Dual-port LVDS output is recommended.	

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5. Revision History

Version	Owner	Content	Date
Preliminary	Y S	Initial Release	08/02/2016
R1.1	N W	Update package information	08/08/2016
R1.2	DS R	Modify TTL output pin mapping and block diagram	08/08/2016
R1.3	Bruce Y	Update power consumption data.	03/10/2017
R1.4	PP J	Modify the format of the document	04/27/2017
	N W	Update package information	11/14/2018
R1.5	PP J	Update Figure 6.1.1	07/25/2019
R1.6	C T	Update thermal resistance info	02/26/2020
R1.7	DS R	Add U5 information	05/21/2020

6. Pinning Information

6.1 Pin Configuration

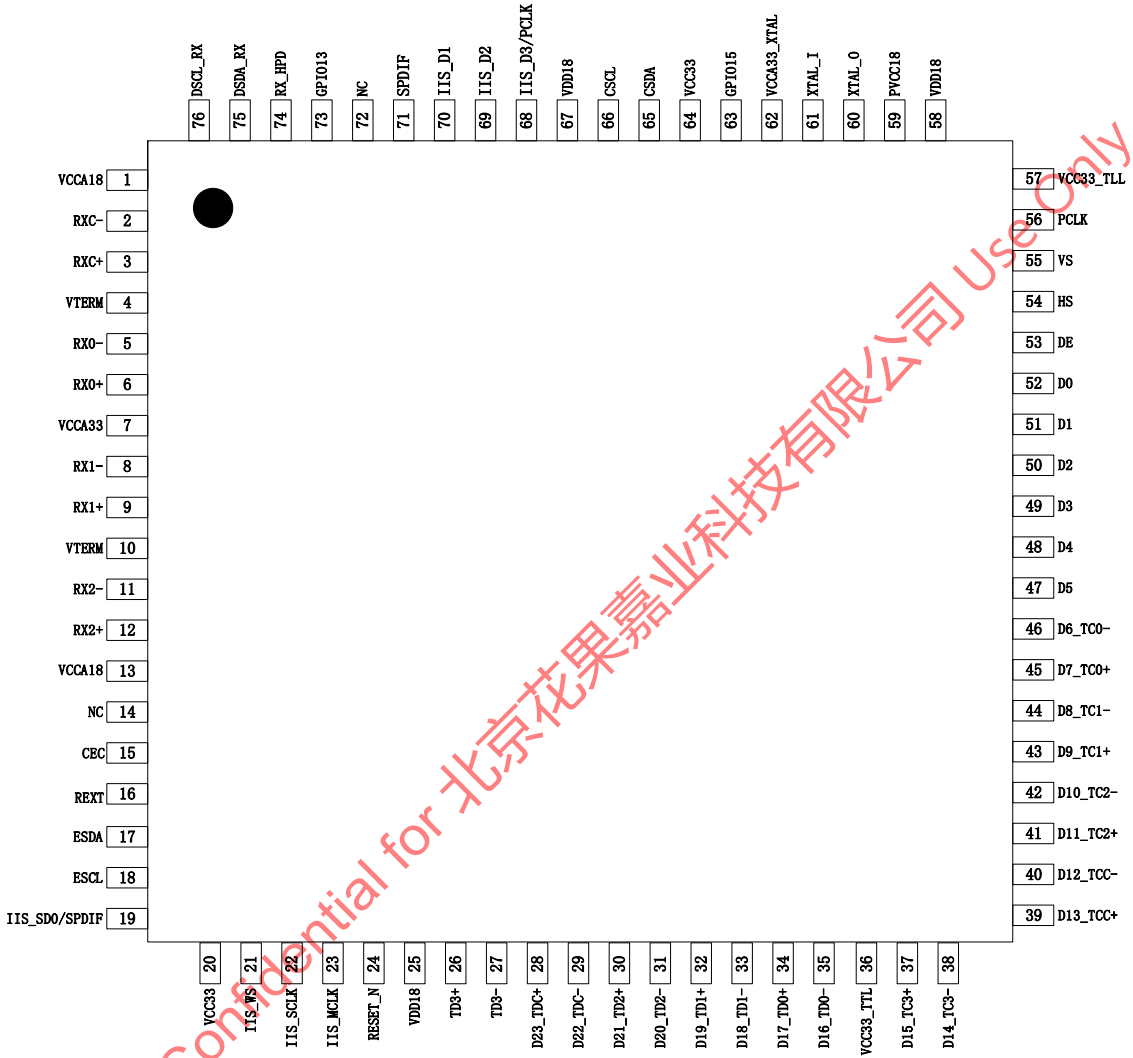

Figure 6.1.1 LT8619C QFN76 (9mm x 9mm) Top View

6.2 Pin Description

(I/O description: A=Analog, I=Input, O=Output, P=Power, G=Ground)

Table 6.2.1 Pin Description

PIN	NAME	I/O	FUNCTION	NOTES
1	VCCA18	AP	1.8V power supply pin for HDMI Receiver	1.8V
2	RXC-	AI	HDMI Receiver clock negative analog input	
3	RXC+	AI	HDMI Receiver clock positive analog input	
4	VTERM	AIO	RX input termination bias, connect to 3.3V power supply	
5	RX0-	AI	HDMI Receiver channel 0 negative analog input	
6	RX0+	AI	HDMI Receiver channel 0 positive analog input	
7	VCCA33	AP	3.3V power supply pin for HDMI Receiver	3.3V
8	RX1-	AI	HDMI Receiver channel 1 negative analog input	
9	RX1+	AI	HDMI Receiver channel 1 positive analog input	
10	VTERM	AIO	RX input termination bias, connect to 3.3V power supply	
11	RX2-	AI	HDMI Receiver channel 2 negative analog input	
12	RX2+	AI	HDMI Receiver channel 2 positive analog input	
13	VCCA18	AP	1.8V power supply pin for HDMI Receiver	1.8V
14，72	NC		No connection. It may be connected to 1.8V power supply.	
15	CEC	IO	HDMI CEC pin	
16	REXT	AIO	External resistor used for accurate current reference, connect 2K 1% resistor to ground. If use internal resistor, this pin may be connected to 1.8V power supply.	
17	ESDA	IO	Master I2C data channel for EEPROM	5V-tolerant
18	ESCL	IO	Master I2C clock channel for EEPROM	5V-tolerant
19	IIS_SD0/SPDIF	O	I2S data0 output/SPDIF audio output	
20	VCC33	P	Power supply pin for IO	3.3V
21	IIS_WS	O	I2S word select output	
22	IIS_SCLK	O	I2S serial clock output	
23	IIS_MCLK	O	I2S audio master clock output	
24	RESET_N	I	Global reset, active low	
25	VDD18	P	Power supply pin for digital	1.8V
26	TD3+	AO	LVDS output	
27	TD3-	AO	LVDS output	
28	D23_TDC+	AO	RGB data23 output(default B7)/LVDS output	
29	D22_TDC-	AO	RGB data22 output(default B6)/LVDS output	
30	D21_TD2+	AO	RGB data21 output(default B5)/LVDS output	
31	D20_TD2-	AO	RGB data20 output(default B4)/LVDS output	
32	D19_TD1+	AO	RGB data19 output(default B3)/LVDS output	
33	D18_TD1-	AO	RGB data18 output(default B2)/LVDS output	
34	D17_TD0+	AO	RGB data17 output(default B1)/LVDS output	
35	D16_TD0-	AO	RGB data16 output(default B0)/LVDS output	

PIN	NAME	I/O	FUNCTION	NOTES
36	VCC33_TTL	AP	3.3V for LVDS output 1.8V or 3.3V for TTL output	3.3V or 1.8V
37	D15_TC3+	AO	RGB data15 output(default G7)/LVDS output	
38	D14_TC3-	AO	RGB data14 output(default G6)/LVDS output	
39	D13_TCC+	AO	RGB data13 output(default G5)/LVDS output	
40	D12_TCC-	AO	RGB data12 output(default G4)/LVDS output	
41	D11_TC2+	AO	RGB data11 output(default G3)/LVDS output	
42	D10_TC2-	AO	RGB data10 output(default G2)/LVDS output	
43	D9_TC1+	AO	RGB data9 output(default G1)/LVDS output	
44	D8_TC1-	AO	RGB data8 output(default G0)/LVDS output	
45	D7_TC0+	AO	RGB data7 output(default R7)/LVDS output	
46	D6_TC0-	AO	RGB data6 output(default R6)/LVDS output	
47	D5	AO	RGB data5 output(default R5)	
48	D4	AO	RGB data4 output(default R4)	
49	D3	AO	RGB data3 output(default R3)	
50	D2	AO	RGB data2 output(default R2)	
51	D1	AO	RGB data1 output(default R1)	
52	D0	AO	RGB data0 output(default R0)	
53	DE	AO	RGB data enable output	
54	HS	AO	RGB horizontal sync output	
55	VS	AO	RGB vertical sync output	
56	PCLK	AO	RGB pixel clock output	
57	VCC33_TTL	AP	3.3V Power supply pins for RGB/LVDS output 3.3V for LVDS output 1.8V or 3.3V for TTL output	3.3V or 1.8V
58	VDD18	P	Power supply pin for digital	1.8V
59	PVCC18	AP	Power supply pin for Audio/Core PLL	1.8V
60	XTAL_O	O	Crystal oscillator output	
61	XTAL_I	I	Crystal oscillator input	25MHz
62	VCCA33_XTAL	AP	Power supply pin for XTAL	3.3V
63	GPIO15	IO	GPIO15	
64	VCC33	AP	Power supply pins for IO	3.3V
65	CSDA	IO	Slave I2C data channel	
66	CSCL	I	Slave I2C clock channel	Device Address: 0x64
67	VDD18	P	Power supply pin for digital	1.8V
68	IIS_SD3/PCLK	O	I2S data3 output. This pin can also be programmed as PCLK only for product version U5.	
69	IIS_SD2	O	I2S data2 output	
70	IIS_SD1	O	I2S data1 output	
71	SPDIF	O	SPDIF audio output	
73	GPIO13	IO	GPIO13	
74	RX_HPD	O	HDMI Receiver hot plug detect output	5V-tolerant
75	DSDA_RX	IO	HDMI Receiver DDC data channel	5V-tolerant
76	DSCL_RX	I	HDMI Receiver DDC clock channel	5V-tolerant

7. Functional Block Description

Figure 7.1 is functional block diagram of LT8619C, and the detailed sub-block relationship is also shown in the diagram.

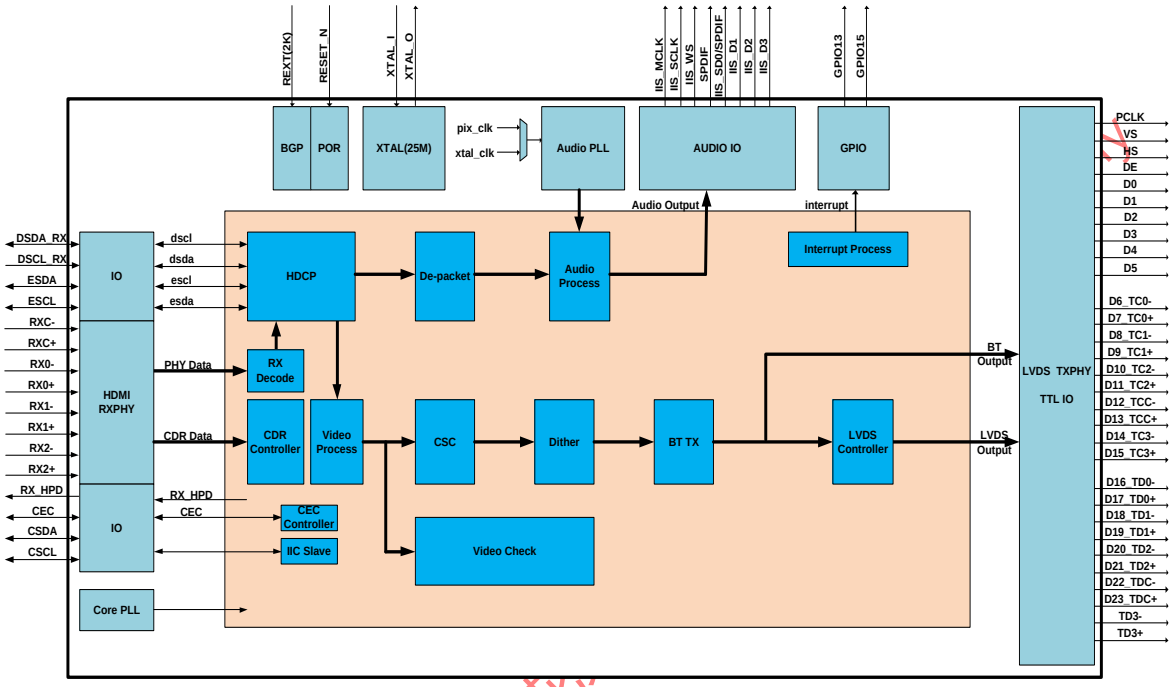

Figure 7.1 Functional Block Diagram

7.1 TTL Output

TTL Output Timing

The TTL output ports send out timing signal PCLK (Pixel Clock), HS (Horizontal Sync), VS (Vertical Sync), DE (Data Enable) and TTL data(RGB or YCbCr or BT656 or BT1120).
For easy PCB layout, LT8619C output data ports D0-D23 can switch RGB data.

Output RGB888/YCbCr data mapping:

Output Port	RGB	YCbCr 4:4:4	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2	24-bit YCbCr 4:2:2
D0	R[0]	Cr[0]	C[0]	C[2]	C[4]
D1	R[1]	Cr[1]	C[1]	C[3]	C[5]
D2	R[2]	Cr[2]	C[2]	C[4]	C[6]
D3	R[3]	Cr[3]	C[3]	C[5]	C[7]
D4	R[4]	Cr[4]	C[4]	C[6]	C[8]
D5	R[5]	Cr[5]	C[5]	C[7]	C[9]
D6	R[6]	Cr[6]	C[6]	C[8]	C[10]
D7	R[7]	Cr[7]	C[7]	C[9]	C[11]
D8	G[0]	Y[0]	Y[0]	Y[2]	Y[4]
D9	G[1]	Y[1]	Y[1]	Y[3]	Y[5]

Output Port	RGB	YCbCr 4:4:4	16-bit YCbCr 4:2:2	20-bit YCbCr 4:2:2	24-bit YCbCr 4:2:2
D10	G[2]	Y[2]	Y[2]	Y[4]	Y[6]
D11	G[3]	Y[3]	Y[3]	Y[5]	Y[7]
D12	G[4]	Y[4]	Y[4]	Y[6]	Y[8]
D13	G[5]	Y[5]	Y[5]	Y[7]	Y[9]
D14	G[6]	Y[6]	Y[6]	Y[8]	Y[10]
D15	G[7]	Y[7]	Y[7]	Y[9]	Y[11]
D16	B[0]	Cb[0]			Y[0]
D17	B[1]	Cb[1]			Y[1]
D18	B[2]	Cb[2]		Y[0]	Y[2]
D19	B[3]	Cb[3]		Y[1]	Y[3]
D20	B[4]	Cb[4]			C[0]
D21	B[5]	Cb[5]			C[1]
D22	B[6]	Cb[6]		C[0]	C[2]
D23	B[7]	Cb[7]		C[1]	C[3]

Output RGB666/RGB565 data mapping:

Output Port	RGB666 Mapping 1	RGB666 Mapping 2	RGB666 Mapping 3	RGB565 Mapping 1	RGB565 Mapping 2	RGB565 Mapping 3
D0		R[0]			R[0]	
D1		R[1]			R[1]	
D2	R[0]	R[2]			R[2]	
D3	R[1]	R[3]		R[0]	R[3]	
D4	R[2]	R[4]		R[1]	R[4]	
D5	R[3]	R[5]		R[2]	G[0]	
D6	R[4]	G[0]	R[0]	R[3]	G[1]	
D7	R[5]	G[1]	R[1]	R[4]	G[2]	
D8		G[2]	R[2]		G[3]	R[0]
D9		G[3]	R[3]		G[4]	R[1]
D10	G[0]	G[4]	R[4]	G[0]	G[5]	R[2]
D11	G[1]	G[5]	R[5]	G[1]	B[0]	R[3]
D12	G[2]	B[0]	G[0]	G[2]	B[1]	R[4]
D13	G[3]	B[1]	G[1]	G[3]	B[2]	G[0]
D14	G[4]	B[2]	G[2]	G[4]	B[3]	G[1]
D15	G[5]	B[3]	G[3]	G[5]	B[4]	G[2]
D16		B[4]	G[4]			G[3]
D17		B[5]	G[5]			G[4]
D18	B[0]		B[0]			G[5]
D19	B[1]		B[1]	B[0]		B[1]
D20	B[2]		B[2]	B[1]		B[2]
D21	B[3]		B[3]	B[2]		B[3]
D22	B[4]		B[4]	B[3]		B[4]
D23	B[5]		B[5]	B[4]		B[5]

Output 16/20/24-bit BT1120/BTA-T1004 data mapping:

Output Port	16-bit Mapping 1	16-bit Mapping 2	20-bit Mapping 1	20-bit Mapping 2	24-bit Mapping
D0	C[0]		C[0]		C[0]
D1	C[1]		C[1]		C[1]
D2	C[2]		C[2]		C[2]
D3	C[3]		C[3]		C[3]
D4	C[4]		C[4]	C[0]	C[4]
D5	C[5]		C[5]	C[1]	C[5]
D6	C[6]		C[6]	C[2]	C[6]
D7	C[7]		C[7]	C[3]	C[7]
D8	Y[0]	C[0]	C[8]	C[4]	C[8]
D9	Y[1]	C[1]	C[9]	C[5]	C[9]
D10	Y[2]	C[2]	Y[0]	C[6]	C[10]
D11	Y[3]	C[3]	Y[1]	C[7]	C[11]
D12	Y[4]	C[4]	Y[2]	C[8]	Y[0]
D13	Y[5]	C[5]	Y[3]	C[9]	Y[1]
D14	Y[6]	C[6]	Y[4]	Y[0]	Y[2]
D15	Y[7]	C[7]	Y[5]	Y[1]	Y[3]
D16		Y[0]	Y[6]	Y[2]	Y[4]
D17		Y[1]	Y[7]	Y[3]	Y[5]
D18		Y[2]	Y[8]	Y[4]	Y[6]
D19		Y[3]	Y[9]	Y[5]	Y[7]
D20		Y[4]		Y[6]	Y[8]
D21		Y[5]		Y[7]	Y[9]
D22		Y[6]		Y[8]	Y[10]
D23		Y[7]		Y[9]	Y[11]

Output 8/10/12-bit BT1120/BT656 data mapping:

Output Port	8-bit Mapping	10-bit Mapping 1	10-bit Mapping 2	12-bit Mapping 1	12-bit Mapping 2
D0		Y/C[0]		Y/C[0]	
D1		Y/C[1]		Y/C[1]	
D2		Y/C[2]		Y/C[2]	
D3		Y/C[3]		Y/C[3]	
D4		Y/C[4]		Y/C[4]	
D5		Y/C[5]		Y/C[5]	
D6		Y/C[6]		Y/C[6]	
D7		Y/C[7]		Y/C[7]	
D8	Y/C[0]	Y/C[8]		Y/C[8]	
D9	Y/C[1]	Y/C[9]		Y/C[9]	
D10	Y/C[2]			Y/C[10]	
D11	Y/C[3]			Y/C[11]	

Output Port	8-bit Mapping	10-bit Mapping 1	10-bit Mapping 2	12-bit Mapping 1	12-bit Mapping 2
D12	Y/C[4]				Y/C[0]
D13	Y/C[5]				Y/C[1]
D14	Y/C[6]		Y/C[0]		Y/C[2]
D15	Y/C[7]		Y/C[1]		Y/C[3]
D16			Y/C[2]		Y/C[4]
D17			Y/C[3]		Y/C[5]
D18			Y/C[4]		Y/C[6]
D19			Y/C[5]		Y/C[7]
D20			Y/C[6]		Y/C[8]
D21			Y/C[7]		Y/C[9]
D22			Y/C[8]		Y/C[10]
D23			Y/C[9]		Y/C[11]

7.2 LVDS Output

LVDS transmitter supports the following features:

- Programmable single port or dual ports
- Programmable 6 bit or 8 bit output
- Programmable ports swapping

In single port output mode, single pixel data (18/24-bit RGB, 3/4 LVDS data streams) is transferred to display port C on each active edge of LVDS_CLK, the rate of LVDS_CLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 7.2.1.

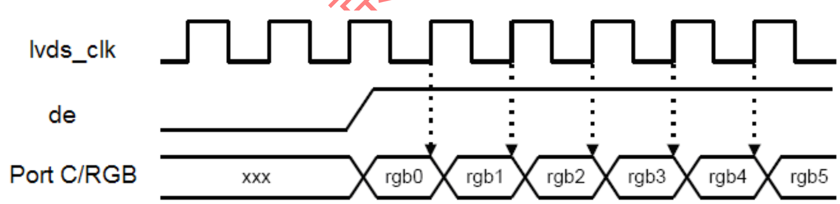

Figure 7.2.1 Single Port Mode Display Data Timing

In dual ports output mode, double pixel data(36/48-bit RGB, 6/8 LVDS data streams) is transferred to display port C & D on each active edge of LVDS_CLK and the rate of LVDS_CLK is equal to half of display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 7.2.2.

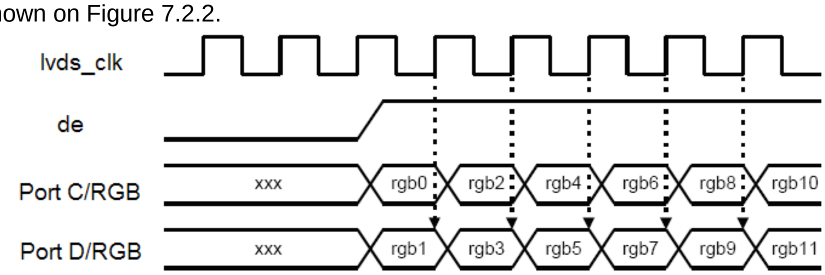

Figure 7.2.2 Dual Ports Mode Display Data Timing

8. DC Electrical Characteristics

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

Symbol	Description	MIN	TYP	MAX	Unit
VCCA18, VDD18	1.8V Power Supply Voltage	-0.3		2.4	V
VCCA33, VCC33, VCC33_TTL, VCC33_XTAL	3.3V Power Supply Voltage	-0.3		4	V
V_I / V_O	LVTTL Input/Output Voltage Range	-0.3		VCC33 +0.3	V
$V_{I(5V)}$ / $V_{O(5V)}$	5V Tolerant Input/Output Voltage Range	-0.3		6	V
T_S	Storage Temperature	-65		150	℃
TJ	Junction Temperature			125	℃
ESD	HBM Electrostatic Discharge Level		2000		V
Notes: Permanent device damage may occur if absolute maximum conditions are exceeded.					

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

Symbol	Description	MIN	TYP	MAX	Unit
VCCA18, VCC33_TTL, VDD18	1.8V Power Supply Voltage	1.7	1.8	1.9	V
VCCA33, VCC33, VCC33_TTL, VCC33_XTAL	3.3V Power Supply Voltage	3.14	3.3	3.46	V
T_A	Operating Free-air Temperature	-20		80	℃
θ_{JC}	Junction to Case Thermal Resistance		10		℃/W

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

DIGITAL I/O DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
V_{IH}	Input High-level Voltage	1.2			V
V_{IL}	Input Low-level Voltage			0.6	V
V_{OH}	Output High-level Voltage	1.4(VCC33_TTL=1.8V) 2.4(VCC33_TTL=3.3V)			V
V_{OL}	Output Low-level Voltage			0.4	V
I_{OD1}	Type 1 digital output drive(V_{OUT}=2.4V)	9.9	15.8	21.6	mA
	Type 1 digital output drive(V_{OUT}=0.4V)	8.1	9.7	10.7	mA
I_{OD2}	Type 2 digital output drive(V_{OUT}=2.4V)	23.0	36.6	50.4	mA
	Type 2 digital output drive(V_{OUT}=0.4V)	23.1	27.2	30.2	mA
TMDS RX DC Specifications					

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{IDIFF}	Differential input voltage level	150		1200	mV
V_{ICM}	Input common mode voltage	VCCA33-700		VCCA33 -37.5	mV
R_{TERM}	Single-ended termination resistance	45	50	55	Ω

Note:
1. For other HDMI DC Spec, please refer to HDMI1.4 Spec.
2. The configuration I2C conforms to I2C-Bus V2.1 Spec standard mode.
3. For digital output pins, output loading is set as CL=10pF.
4. For digital output pins: Minimum output drive specified at ambient=70° C and IOVCC=3.0V. Typical output drive specified at ambient=25° C and IOVCC=3.3V. Maximum output drive specified at ambient=0° C and IOVCC=3.6V.
5. I_{OD1} output applies to pins D23 to D0, DE, HS, VS, PCLK.
6. I_{OD2} output applies to pins IIS_SD0/SPDIF, IIS_WS, IIS_SLCK, IIS_MCLK, IIS_SD3/PCLK, IIS_SD2, IIS_SD1, SPDIF and GPIO13.
7. All parameters are guaranteed by design.

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

TMDS RX AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
V_S	Minimum differential sensitivity(peak to peak) after the reference cable equalizer	150			mV
T_{INTRA_SKEW}	Intra-pair skew at sink connector			$0.15T_{bit}+112$	ps
T_{INTER_SKEW}	Inter-pair skew at sink connector			$0.2T_{charactor}+1.78$	ns
T_{JITTER}	TMDS clock jitter			$0.3T_{bit}$	ps
LVDS Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
Tc	Output clock cycle	6.67		40	ns
T_{rise}	VOD rise time, 20% to 80%			250	ps
T_{fall}	VOD fall time, 20% to 80%			250	ps
T0	Output data position0	-0.15	0	0.15	ns
T1	Output data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Output data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Output data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Output data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Output data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Output data position6	6Tc/7-0.15		6Tc/7+0.15	ns
TTL Output AC Timing Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
T_{CIP}	SDR Mode PCLK Period, one pixel per clock	3.3		40	ns
F_{CIP}	SDR Mode PCLK Frequency, one pixel per clock	25		300	MHz
T_{CIP_DDR}	DDR Mode PCLK Period, dual-edge clock	6.6		80	ps
F_{CIP_DDR}	DDR Mode PCLK Frequency, dual-edge clock	12.5		150	MHz
T_{DUTY}	SDR Mode PCLK Duty Cycle(fixed phase)	40%		60%	T_{CIP}
T_{DUTY}	SDR Mode PCLK Duty Cycle(adjusted phase)	30%		70%	T_{CIP}
T_{DUTY_DDR}	DDR Mode PCLK Duty Cycle	45%		55%	T_{CIP_DDR}
T_{DV_MAX}	Output valid data maximum delay			2.5	ns
T_{DV_MIN}	Output valid data minimum delay	0.5			ns

T_{SU}	Setup Time to PCLK	0.8			ns
T_{HD}	Hold Time to PCLK	0.5			ns

Note:
1. For other HDMI AC Spec, please refer to HDMI1.4 Spec.
2. The configuration I2C conforms to I2C-Bus V2.1 Spec standard mode.
3. All parameters are guaranteed by design.

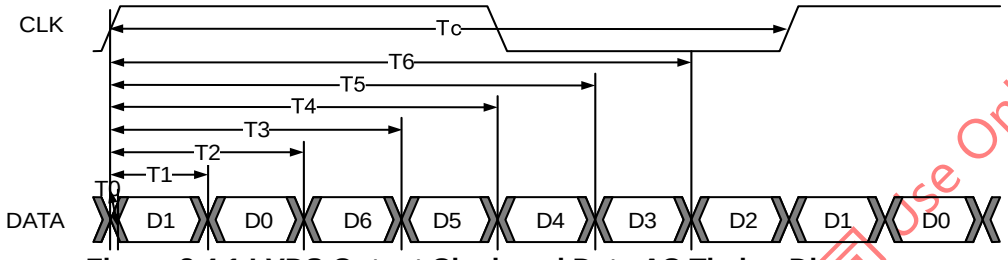

Figure 8.4.1 LVDS Output Clock and Data AC Timing Diagram

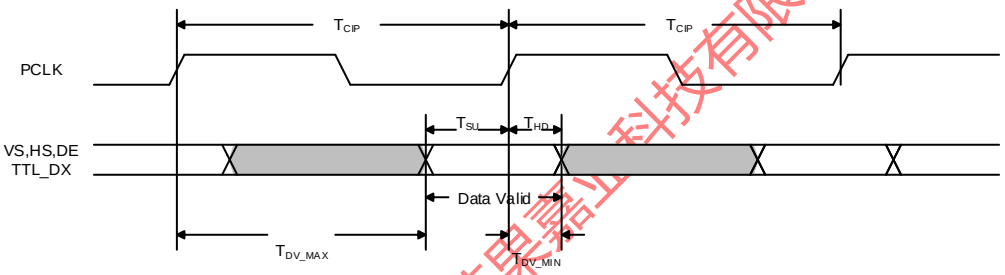

Figure 8.4.2 SDR mode TTL output setup and hold time

($T_{HD} = T_{DV\_MIN}$; $T_{SU} = T_{CIP} - T_{DV\_MAX}$)

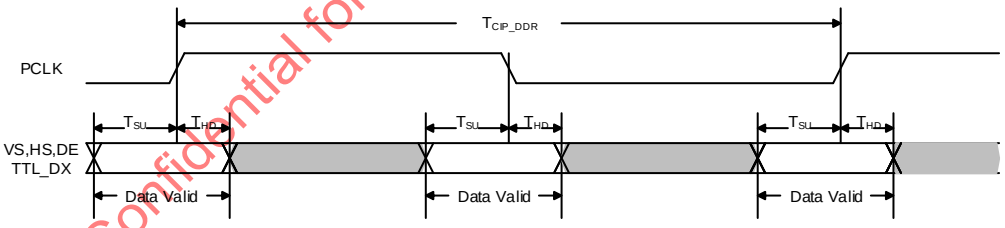

Figure 8.4.3 DDR mode TTL output setup and hold time

8.5 Power Consumption

Table 8.5.1 TTL Output Power Consumption

Symbol	Description	Conditions		MIN	TYP	MAX	Unit
I_{CC}	Operating current	TMDS CLK (27M)	1.8V		104		mA
			3.3V		55		mA
		TMDS CLK (74.25M)	1.8V		140		mA
			3.3V		60		mA
		TMDS CLK (148.5M)	1.8V		197		mA
			3.3V		72		mA
		TMDS CLK (297M)	1.8V		305		mA
			3.3V		80		mA

**Measured under RGB888 output mode. Also can be referred for BT656 and BT1120 output mode.*

Table 8.5.2 LVDS Output Power Consumption

Symbol	Description	Conditions	MIN	TYP	MAX	Unit
I_{CC}	Operating current	1.8V		176		mA
		3.3V		105		mA

**Measured under dual-port 8bit LVDS output mode and input resolution is 1080P60.*

9. Packaging

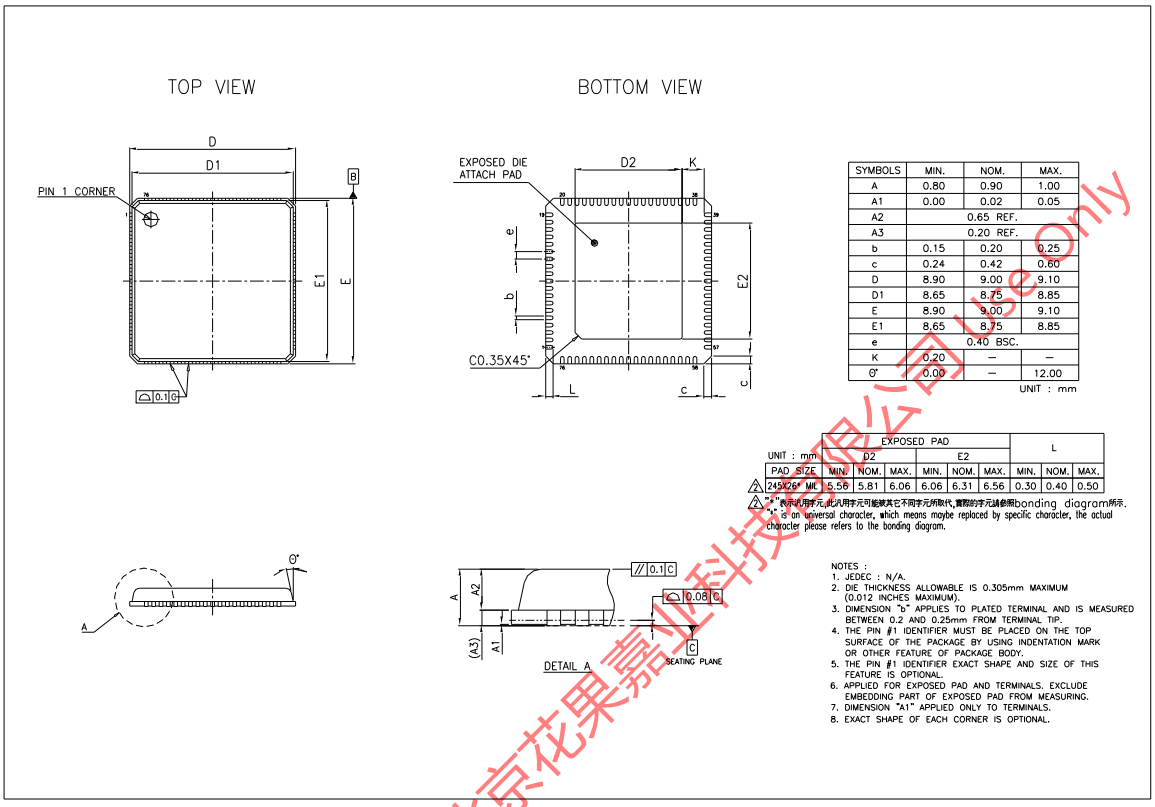

Figure 9.1 76-pin QFN package

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