# LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

# LT8668EX LCD Controller

# Data Sheet




**We produce mixed-signal products for a better digital world!**

# Revision History

| Version | Owner | Content | Date |
|---|---|---|---|
| Preliminary | YS Zhang | The second version | 07/11/2014 |
| Preliminary | N.Wang | Modify package information | 07/14/2014 |
| 1.0 | YS Zhang | LCD Controller Datasheet Version 1.0 | 10/28/2014 |
| 1.1 | N.Wang | Review package information | 12/11/2014 |

# Table of Contents

# 1. General Description

The LT8668EX is Lontium's second generation LCD controller that supports both VGA interface and the HDMI interface based on ClearEdge™ technology, compliant with the HDMI 1.4(High Definition Multimedia Interface) specification. It can also support Dual-Mode DP and MHL with HDMI interface. For backward compatibility, this LCD controller also includes a high performance analog interface to work with traditional VGA/YPbPr interface. With quad-LVDS ports it can support quad-LVDS ports monitor with 4Kx2K resolution. And dual-LVDS ports or single-LVDS port for other resolution. It can also support RGB888/RGB666/RGB565 for TTL interface panel with LVDS ports. For total solution of LCD controller, LT8668EX integrates main functions include position adjustment, programmable scalar, video processor (hue, saturation, brightness and contrast adjustment), OSD, gamma correction, PWM, MCU, total 16 GPIOs and nor-flash (optional). For easy implement of a multi-media system, LT8668EX supports 2-channel I2S audio input and 8-channel high quality I2S audio or SPDIF audio output. LT8668EX integrates 4M bits nor-flash inside, and also you can use external nor-flash by SPI interface for compatibility.

The LT8668EX is offered in a 128-pin LQFP package, with operating temperature range of -10℃-70℃.

## 1.1. Key Features

**HDMI/MHL Dual Mode Rx**

- Direct interface to DVI 1.0 and HDMI V1.4 receiver
- Compliance with DVI up to 1.65Gbps and HDMI V1.4 up to 3.0Gbps
- Support MHL V2.0 on the same pins with HDMI
- Multiple pixel formats: RGB 6/8/10/12 bit per component (bpc); YCbCr 422/444 8/10/12 bpc
- High input sensitivity, with differential input level down to 80mV
- Receiver side equalization up to 12 dB
- Auto Loss of Signal detection
- High jitter tolerance up to 0.6UI
- HDCP decryption
- On-chip EDID
- Support input resolution up to 4Kx2K@30Hz

**Analog RGB/YPbPr Input Interface**

- 1 channel Analog input supported
- On-chip EDID
- Integrated 8-bit triple-channel 165MHZ ADC/PLL
- Support RGB/YCbCr input
- Support SOG(Sync-On-Green)
- Auto adjusting true 64 phase ADC PLL
- Support input resolution up to 1080P

**Output Interface**

- Quad channels LVDS output ports
- Single, double or quad pixel mode
- 24/48/96-bit panel mapping to the LVDS channels
- 18/36/72-bit panel mapping to the LVDS channels

- Programmable LVDS ports swapping
- Programmable channel swapping
- Support output resolution up to 4Kx2K@30Hz for true 4K LCD
- Spread-Spectrum DPLL to reduce EMI
- Compliant with RGB888/RGB666/RGB565 TTL output

**On Chip Manager**

- Embedded 51 Core, and is compatible with Standard 8051 instruction
- Up to 24K bytes on chip PRAM
- One external interrupt
- Embedded SPI master for external SPI flash
- Programmable digital PWM for backlight control
- 8bit ADC for key pad control
- I2C BUS (slave mode)

**Scaling**

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality

**Video Processing**

- Programmable hue and saturation adjustment
- brightness and contrast control
- Programmable Color space conversion
- Programmable gamma correction support
- Advanced dithering logic for 18-bit panel color depth enhancement

**Audio Support**

- 2-channel of analog audio input for the support of DVI
- Optional SPDIF output and 8-channel I2S output
- Supports PWM output for audio volume control

**On-chip OSD**

- Embedded 15K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1,2 and 4-bit per pixel
- 16 color palette
- Programmable blinking effects for each character
- Programmable alpha-blending
- Optional 10x18~12x18 font matrix selection

Other Features

- Support I2C slave debug mode
- Extensive power management for power savings
- Support total 16 GPIOs
- Integrated pattern generation
- Integrated nor-flash(optional)

## 1.2. Applications

- HD LCD computer Monitors

- HD LCD Monitors for medical and other applications
- Multi-Media process and display control
- HDMI/MHL/VGA to LVDS Interface conversion

### 1.3. Absolute Maximum Ratings

| | | |
|---|---|---|
| Supply Voltage | VDD33 | ..... 3.0V to 3.6V |
| | VCCA33 | ..... 3.0V to 3.6V |
| | VCCA18 | ..... 1.7V to 1.90V |
| | VDD18 | ..... 1.62V to 1.98V |
| Operating Junction Temperature Range | | ..... -10°C to +70°C |
| Storage Temperature Range | | ..... -10°C to +70°C |

## 2. Functional Block Description

Figure 1 is functional block diagram of LT8668EX, and the block detail internal relationship is also shown in the diagram.

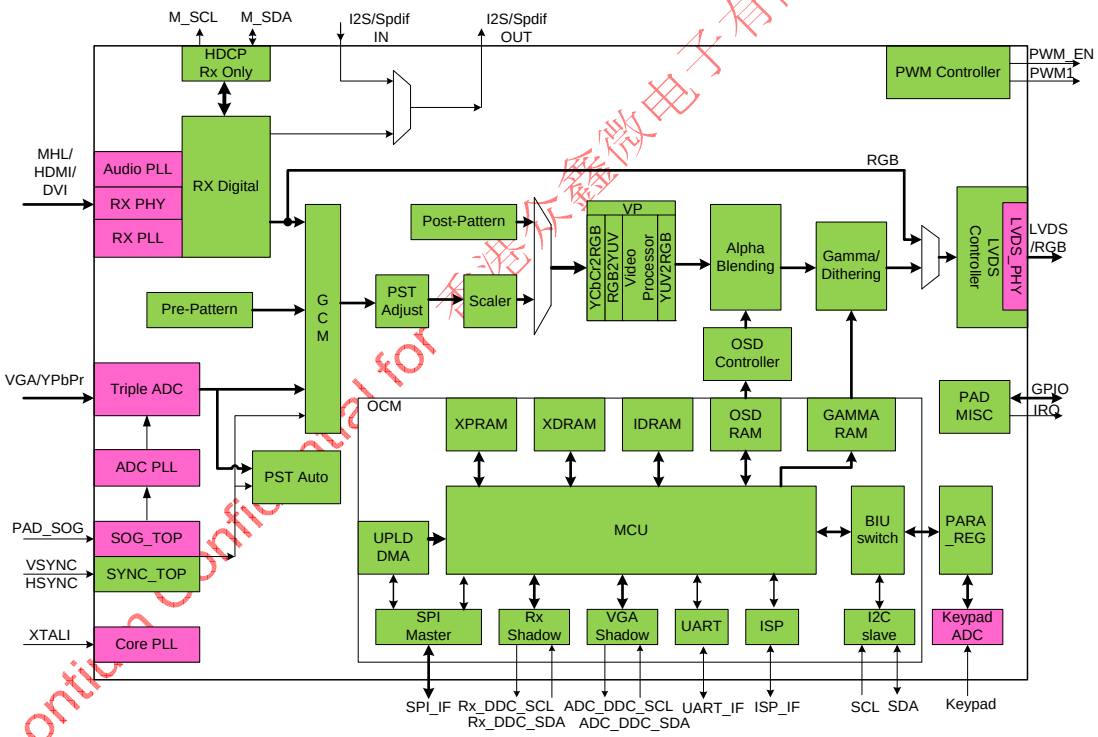


Figure 1: Functional Block Diagram

### 2.1. Application Diagram

Figure 2 is the normal application diagram of the HD-LCD controller chip. In the chip it include a triple ADC, a TMDS receiver, a Scalar, a MCU and associated interfaces, an on-chip OSD, and a quad LVDS driver for LCD panel interface. It also includes a digital audio interface, a PWM module for back light control. The interface with DisplayPort

can be realized through the TMDS interface by adding an external level-shifter chipset. HDCP is also support.

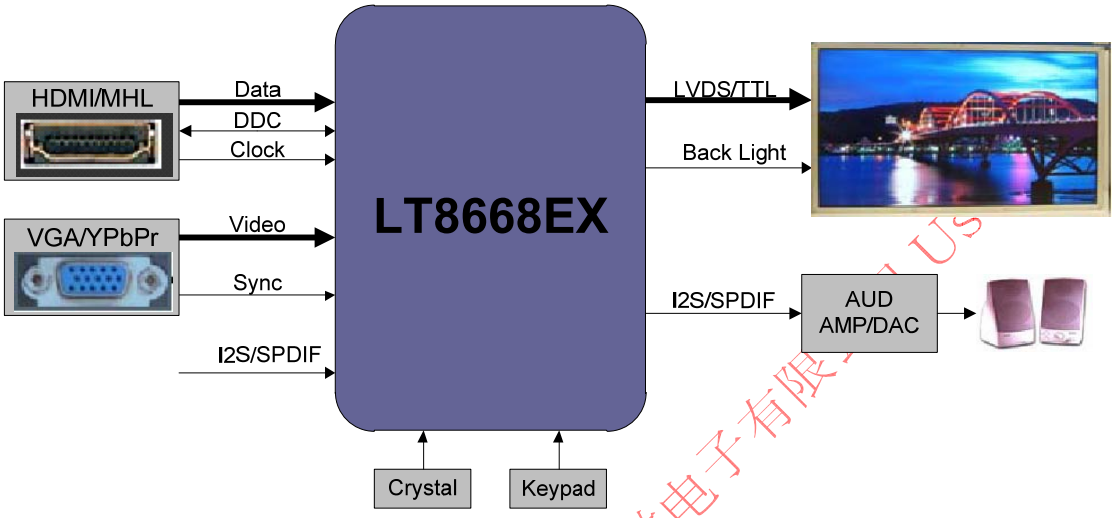


Figure 2: LCD Controller Application Diagram

## 2.2. Pin Configuration

Figure 3 is the pin diagram of the LT8668EX HD-LCD controller chip.

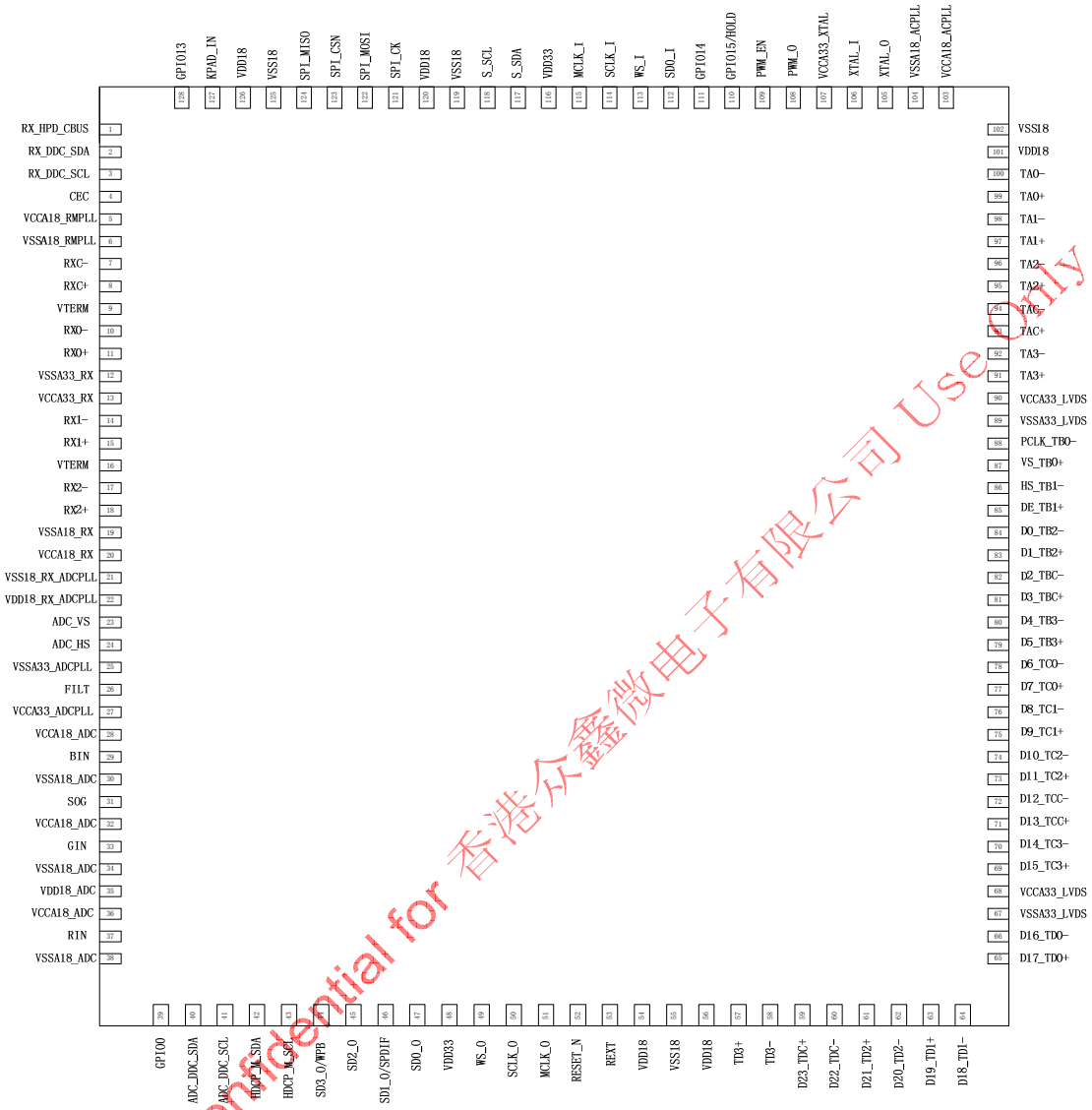


Figure 3: Pin Diagram



## 2.3. Pin Descriptions

(I/O description: A=Analog, I=Input, O=Output, P=Power, G=Ground)

| PIN | NAME | I/O | FUNCTION | NOTES |
|---|---|---|---|---|
| **ADC Pins** | | | | |
| 23 | ADC_VS | AI | VGA Vertical Sync input | 5V-tolerant |
| 24 | ADC_HS | AI | VGA Horizontal Sync input | 5V-tolerant |
| 29 | BIN | AI | VGA blue channel analog input | |
| 33 | GIN | AI | VGA green channel | |

| | | | | |
|---|---|---|---|---|
| | | | analog input | |
| 37 | RIN | AI | VGA red channel analog input | |
| 31 | SOG | AI | SOG analog input | |
| 26 | FILT | AIO | ADC PLL external filter | |
| 40 | ADC_DDC_SDA | IO | ADC DDC data channel | 5V-tolerant |
| 41 | ADC_DDC_SCL | IO | ADC DDC clock channel | 5V-tolerant |
| 28,32,36 | VCCA18_ADC | AP | Power supply pins for ADC | 1.8V |
| 30,34,38 | VSSA18_ADC | AG | Ground supply pins for ADC | |
| 35 | VDD18_ADC | AP | Power supply pins for ADC | 1.8V |
| 27 | VCCA33_ADCPLL | AP | Power supply pins for ADC PLL | 3.3V |
| 25 | VSSA33_ADCPLL | AG | Ground supply pins for ADC PLL | |
| **HDMI/MHL RX Pins** | | | | |
| 1 | RX_HPD_CBUS | IO | HDMI Receiver hot plug detect output and MHL CBUS | 5V-tolerant |
| 2 | RX_DDC_SDA | IO | HDMI Receiver DDC data channel | 5V-tolerant |
| 3 | RX_DDC_SCL | IO | HDMI Receiver DDC clock channel | 5V-tolerant |
| 4 | CEC | IO | HDMI CEC pin | 5V-tolerant |
| 7 | RXC_n | AI | HDMI Receiver clock negative analog input | |
| 8 | RXC_p | AI | HDMI Receiver clock positive analog input | |
| 10 | RX0_n | AI | HDMI Receiver channel 0 negative analog input | |
| 11 | RX0_p | AI | HDMI Receiver channel 0 positive analog input | |
| 14 | RX1_n | AI | HDMI Receiver channel 1 negative analog input | |
| 15 | RX1_p | AI | HDMI Receiver channel 1 positive analog input | |
| 17 | RX2_n | AI | HDMI Receiver channel 2 negative analog input | |
| 18 | RX2_p | AI | HDMI Receiver channel 2 positive analog input | |
| 9,16 | VTERM | AIO | RX input termination bias, connect 3.3V or 1.8 power supply | |
| 53 | REXT | AIO | External resistor used for accurate current reference, connect 6.04K 1% resistor to ground | |
| 12 | VSSA33_RX | AG | 3.3V Ground supply pins | |

| | | | | |
|---|---|---|---|---|
| | | | for HDMI Receiver | |
| 13 | VCCA33_RX | AP | 3.3V Power supply pins for HDMI Receiver | 3.3V |
| 20 | VCCA18_RX | AP | 1.8V Power supply pins for HDMI Receiver | 1.8V |
| 19 | VSSA18_RX | AG | 1.8V Ground supply pins for HDMI Receiver | |
| 5 | VCCA18_RMPLL | AP | Power supply pins for HDMI/MHL Receiver PLL | 1.8V |
| 6 | VSSA18_RMPLL | AG | Ground supply pins for HDMI/MHL Receiver PLL | |
| **Display PLL Pins** | | | | |
| 105 | XTALO | O | Crystal oscillator output | |
| 106 | XTALI | I | Crystal oscillator input | |
| 103 | VCCA18_ACPLL | AP | Power supply pin for Audio/Core PLL | 1.8V |
| 104 | VSSA18_ACPLL | AG | Ground supply pin for Audio/Core PLL | |
| 107 | VCCA33_XTAL | AP | Power supply pin for XTAL | 3.3V |
| **LVDS Pins** | | | | |
| 100 | TA0_n | AO | LVDS PortA channel 0 negative output | |
| 99 | TA0_p | AO | LVDS PortA channel 0 positive output | |
| 98 | TA1_n | AO | LVDS PortA channel 1 negative output | |
| 97 | TA1_p | AO | LVDS PortA channel 1 positive output | |
| 96 | TA2_n | AO | LVDS PortA channel 2 negative output | |
| 95 | TA2_p | AO | LVDS PortA channel 2 positive output | |
| 94 | TAC_n | AO | LVDS PortA clock channel negative output | |
| 93 | TAC_p | AO | LVDS PortA clock channel positive output | |
| 92 | TA3_n | AO | LVDS PortA channel 3 negative output | |
| 91 | TA3_p | AO | LVDS PortA channel 3 positive output | |
| 88 | PCLK_TB0_n | AO | LVDS PortB channel 0 negative output/TTL pixel clock output | |
| 87 | VS_TB0_p | AO | LVDS PortB channel 0 positive output/TTL | |

| | | | | |
|---|---|---|---|---|
| | | | vertical sync output | |
| 86 | HS_TB1_n | AO | LVDS PortB channel 1 negative output/TTL horizontal sync output | |
| 85 | DE_TB1_p | AO | LVDS PortB channel 1 positive output/TTL display enable output | |
| 84 | D0_TB2_n | AO | LVDS PortB channel 2 negative output/TTL data0 output | |
| 83 | D1_TB2_p | AO | LVDS PortB channel 2 positive output/TTL data1 output | |
| 82 | D2_TBC_n | AO | LVDS PortB clock channel negative output/TTL data2 output | |
| 81 | D3_TBC_p | AO | LVDS PortB clock channel positive output/TTL data3 output | |
| 80 | D4_TB3_n | AO | LVDS PortB channel 3 negative output/TTL data4 output | |
| 79 | D5_TB3_p | AO | LVDS PortB channel 3 positive output/TTL data5 output | |
| 78 | D6_TC0_n | AO | LVDS PortC channel 0 negative output/TTL data6 output | |
| 77 | D7_TC0_p | AO | LVDS PortC channel 0 positive output/TTL data7 output | |
| 76 | D8_TC1_n | AO | LVDS PortC channel 1 negative output/TTL data8 output | |
| 75 | D9_TC1_p | AO | LVDS PortC channel 1 positive output/TTL data9 output | |
| 74 | D10_TC2_n | AO | LVDS PortC channel 2 negative output/TTL data10 output | |
| 73 | D11_TC2_p | AO | LVDS PortC channel 2 positive output/TTL data11 output | |

| | | | | |
|---|---|---|---|---|
| 72 | D12_TCC_n | AO | LVDS PortC clock channel negative output/TTL data12 output | |
| 71 | D13_TCC_p | AO | LVDS PortC clock channel positive output/TTL data13 output | |
| 70 | D14_TC3_n | AO | LVDS PortC channel 3 negative output/TTL data14 output | |
| 69 | D15_TC3_p | AO | LVDS PortC channel 3 positive output/TTL data15 output | |
| 66 | D16_TD0_n | AO | LVDS PortD channel 0 negative output/TTL data16 output | |
| 65 | D17_TD0_p | AO | LVDS PortD channel 0 positive output/TTL data17 output | |
| 64 | D18_TD1_n | AO | LVDS PortD channel 1 negative output/TTL data18 output | |
| 63 | D19_TD1_p | AO | LVDS PortD channel 1 positive output/TTL data19 output | |
| 62 | D20_TD2_n | AO | LVDS PortD channel 2 negative output/TTL data20 output | |
| 61 | D21_TD2_p | AO | LVDS PortD channel 2 positive output/TTL data21 output | |
| 60 | D22_TDC_n | AO | LVDS PortD clock channel negative output/TTL data22 output | |
| 59 | D23_TDC_p | AO | LVDS PortD clock channel positive output/TTL data23 output | |
| 58 | TD3_n | AO | LVDS PortD channel 3 negative output | |
| 57 | TD3_p | AO | LVDS PortD channel 3 positive output | |
| 68,90 | VCCA33 | AP | 3.3V Power supply pins | 3.3V |

| | | | | |
|---|---|---|---|---|
| | | | for LVDS | |
| 67,89 | VSSA33 | AG | Ground supply pins for LVDS | |
| **SPI Flash Pins** | | | | |
| 121 | SPI_CK | O | External flash SPI chip clock | |
| 122 | SPI_MOSI | O | External flash SPI chip serial data input | |
| 123 | SPI_CSN | O | External flash SPI chip enable | |
| 124 | SPI_MISO | I | External flash SPI chip serial data output | |
| **Audio Pins** | | | | |
| 49 | WS_O | O | I2S word select output/GPIO2 | |
| 50 | SCLK_O | O | I2S serial clock output/GPIO1 | |
| 51 | MCLK_O | O | I2S audio master clock output | |
| 47 | SD0_O | O | I2S data0 output/GPIO3 | |
| 46 | SD1_O | O | I2S data1 output/SPDIF audio output/GPIO4 | |
| 45 | SD2_O | O | I2S data2 output/GPIO5 | |
| 44 | SD3_O/WPB | O | I2S data3 output/Integrated flash WPB pin/GPIO6 | |
| 114 | SCLK_I | I | I2S serial clock input/GPIO9 | |
| 115 | MCLK_I | I | I2S audio master clock input/GPIO8 | |
| 112 | SD0_I | I | I2S input/SPDIF input/GPIO11 | |
| 113 | WS_I | I | I2S word select input/GPIO10 | |
| **Control Pins** | | | | |
| 52 | RESET_N | I | Global reset, active low | |
| 127 | KPAD_IN | AI | Keypad Analog Input | |
| 108 | PWM | O | Panel backlight control/GPIO7 | |
| 109 | PWM_EN | O | Panel backlight control/GPIO12 | |
| 39 | GPIO0 | IO | General purpose input/output | |
| 128 | GPIO13 | IO | General purpose input/output | |
| 111 | GPIO14 | IO | General purpose input/output | |
| 110 | GPIO15/HOLD | IO | General purpose input/output; Integrated flash HOLD pin | |

| | | | | |
|---|---|---|---|---|
| 42 | HDCP_M_SDA | IO | Master I2C data channel | 5V-tolerant |
| 43 | HDCP_M_SCL | IO | Master I2C clock channel | 5V-tolerant |
| 117 | S_SDA | IO | Slave I2C data channel | 5V-tolerant |
| 118 | S_SCL | IO | Slave I2C clock channel | 5V-tolerant |
| **Power and Ground Pins** | | | | |
| 22,54,56,101,120,126 | VDD18 | P | Power supply pins for digital | 1.8V |
| 21,55,102,119,125 | VSS18 | G | Ground supply pins for digital | |
| 48,116 | VDD33 | P | Power supply pins for IO | 3.3V |

## 2.4. Major Function Block Descriptions

A functional block diagram is illustrated as Figure 1. Each of the functional units shown is described in the following sections.

### 2.4.1. VGA - ADC

The analog-to-digital converter (ADC) transfers the input analog R/G/B video signals to digital output data with each 8-bit resolution. The maximum clock sample frequency is 165M. RIN/GIN/BIN is high-impedance input pins that accept the RED, GREEN, and BLUE channel graphics signals. They accommodate input signals ranging from 0.7V (p-p) full-scale. Signals should be AC-couple to these pins.
Please note that it is very important to follow the recommended layout guidelines for the circuit shown in the Figure 4.

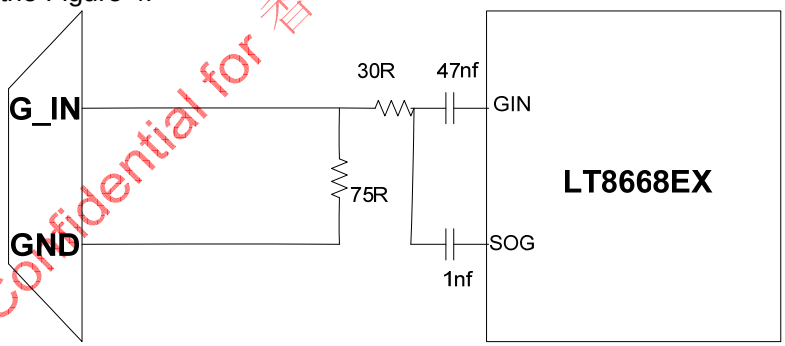


Figure 4: Example ADC Signal Terminations

### 2.4.2. Position Auto Adjust

Position auto adjust module is used to adjust the position of video picture vertically and horizontally. The module is made of two parts: RGB data start address counterpart and positions adjust part.

### 2.4.3. Sync Process

The LT8668EX has a sync processor block providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input timing.

**Hsync /Vsync Frequency and Polarity Detection**

SYNC_HCNT, the 16 bits hsync period counter counts the time of 32xhsync period, then loads the result into the SYNC_HCNT. The output value will be [((REFCLKfreq x 32)/Hfreq)], updated at positive edge of vsync or negative edge of vsync.

SYNC_VCNT, the 11 bits vsync period counter counts the counter of hsync pulse between two vsync pulses, and then loads the result into the SYNC_VCNT. The output value will be [(VGA_V_TOTAL)], updated every vsync period.

The polarity functions detect the input hsync/vsync duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted.

### 2.4.4. Embedded HDMI Receiver

The embedded HDMI receiver is compliant with High Definition Multimedia Interface (HDMI) Specification 1.4. HDMI is unified digital video, audio, and control data over low-cost cables. LT8668EX HDMI RX can connect digital television, flat panel displays and project systems digitally to multimedia sources: DVD players, high definition set-top boxes, digital video tape recorders, and personal computers. Digital transmission, in turn, delivers an uncompromising multimedia experience. Inexpensive cables up to 20 meters and assure the widest range of interoperability against uncertain qualities of cheap cables from low-cost suppliers as the standard matures. The HDMI RX can receive and output up to eight digital audio channels at up to 192 kHz sampling rate, making it the leading component for integrated home theaters and high definition televisions. The device supports direct connections to a wide selection of audio DACs and decoders through industry standard I2S or S/PDIF interfaces.

**HDMI/MHL Dual Mode Rx Features:**

- Single channel HDMI receiver
- Compliant with HDMI1.4, DVI 1.0, and MHL2.0 specifications
  - Supporting pixel rates from 13.5MHz to 300MHz
  - DTV resolutions: 480p, 576p, 720p, 1080p up to 4kx2k
  - PC resolutions: VGA, SVGA, XGA, SXGA up to UXGA
- Video output interface supporting digital video standards such as:
  - 24-bit RGB/YCbCr 4:4:4
  - 16 YCbCr 4:2:2
- Intelligent adaptive channel equalization supporting up to 20m cable at the highest video data rate
- Up sampling from YCbCr 4:2:2 to YCbCr 4:4:4
- Digital audio output interface supporting
  - I2S interface supporting, audio sample rate: 32~192 kHz
  - sample size: 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio transmission using IEC60958 and IEC 61937
  - automatic audio error detection for programmable soft mute, preventing annoying harsh automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug

### 2.4.5. Scaling

The scaling engine uses an advanced scaling technique that provides simultaneous high quality scaling of real time video and graphics images. An input frame is scalable arbitrarily in both the vertical and horizontal dimensions. The Scalar provides independently horizontal and vertical zoom Scalar with adjustable zoom factor from 1/4x to 4x.

**Scaling Feature**

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality

### 2.4.6. Color Enhance Processing

LT8668EX provided color and image enhance control. The color process consists of YCbCr convert to RGB, Contrast and Brightness control, Hue and Saturation Control, Dithering Control, Gamma Correction Control.

The following diagram presents the data flow among OSD signal, video process signal, alpha blending, gamma correction, dithering

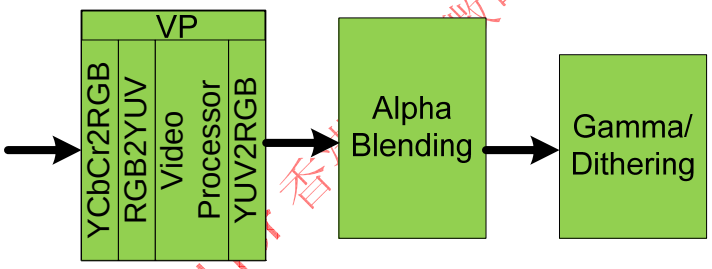


Figure 5: Video Data Path Diagram

**VP**

VP includes YCbCr2RGB, programmable Contrast and Brightness adjustment, programmable Hue and Saturation adjustment. YCbCr2RGB include 4 YCbCr convert to RGB formulas, include SDPC (16~235), SDTV (0~255), HD normal and HD PC color space conversion.

**Alpha Blending**

8 levels of blending are supported for the OSD images. OSD color value 0 is reserved for transparency and is unaffected by the blend attribute. Blend levels for binary codes “111” through “000” are 12.5%, 25%, 37.5%, 50%, 62.5%, 75%, 87.5%, and 100%. Blend percentage level refers the percentage of the output data that is OSD. For example, 001 mean output data stream 87.5% OSD data blending 12.5% image data. This OSD picture would be only slightly translucent.

**Gamma Correction**

Screen brightness is a function of the voltage applied to the LCD display. A “gamma” effect will occur when the change in brightness is different from an increase in applied voltage at low magnitude versus the same voltage increase at high magnitudes. LCD displays typically

characterize this non-uniform behavior with a “Gamma Curve”. A typical curve is shown below.

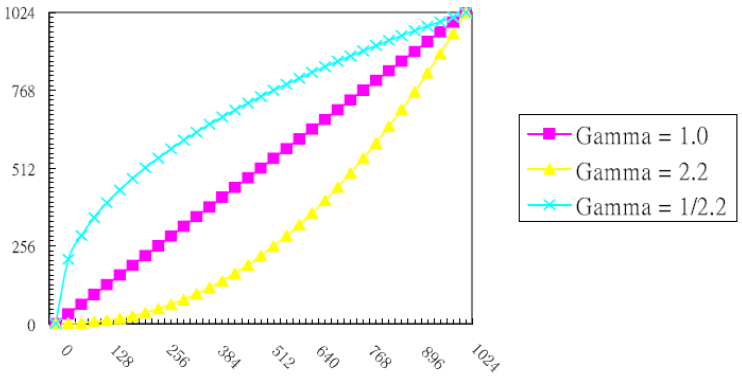


Figure 6: Gamma Correction Curve

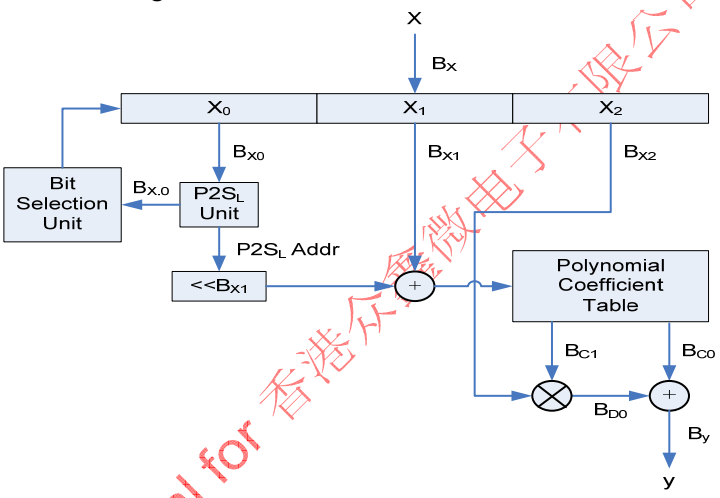


Figure 7: Proposed Gamma Correction Architecture



**Dithering**

A 10-bit output results in an improved color depth control. The 10-bit output is optionally dithered down to 8 bits (or 6 bits) per channel at the display. Dithering works by spreading quantization error over neighboring pixels both spatially and temporally. The benefit of dithering is that the human eye will tend to average neighboring pixels and a smooth image free of contours will be perceived. Both ordered-type and random-type dithering methods are available, though ordered-type is preferred to optimize quality.

### 2.4.7. OSD

The build-in OSD has the following features that listed below.

- Programmable multi-color RAM font OSD
- Totally 184 programmable 1 bits/pixel RAM Fonts, 64 programmable 2 bits/pixel RAM fonts, and 8 programmable 4 bits/pixel RAM Fonts
- Character attributes for 1, 2, 4 bits/pixel
- Optional 10x18, 12x18 font matrix selection
- Internal SRAM allows up to 2048 characters
- Fully programmable character array of 32 rows by 64 columns

- Programmable blinking effects for each character
- Background Translucent, transparent, and opaque effects
- Programmable vertical and horizontal positioning for display
- Maximum pixel CLK of UXGA resolution

### OSD Font's Attribute

| | |
|---|---|
| bit_sel[1:0] | Font type select |
| fg3_sel[3:0] | Foreground(font) color3 select(2bit/pixel) |
| fg2_sel[3:0] | Foreground(font) color2 select(2bit/pixel) |
| fg1_sel[3:0] | Foreground(font) color1 select(2bit/pixel) |
| bg_sel[3:0] | Background color select |

One bit per pixel.(bit_sel == 2'b00)
Foreground '1' pixel [3:0] <= fg1_sel[3:0]
Background '0' pixel [3:0] <= bg_sel[3:0]

Two Bit per pixel. (bit_sel[1] == 1'b1)
Foreground '11' pixel [3:0] <= fg3_sel[3:0]
Foreground '10' pixel [3:0] <= fg2_sel[3:0]
Foreground '01' pixel [3:0] <= fg1_sel[3:0]
Background '00' pixel [3:0] <= bg_sel[3:0]

Four Bit per pixel. (bit_sel == 2'b01)
Foreground '1111' pixel [3:0] <= bg_sel[3:0] + '1111'
Foreground '1110' pixel [3:0] <= bg_sel[3:0] + '1110'
Foreground '1101' pixel [3:0] <= bg_sel[3:0] + '1101'
Foreground '1100' pixel [3:0] <= bg_sel[3:0] + '1100'
Foreground '1011' pixel [3:0] <= bg_sel[3:0] + '1011'
Foreground '1010' pixel [3:0] <= bg_sel[3:0] + '1010'
Foreground '1001' pixel [3:0] <= bg_sel[3:0] + '1001'
Foreground '1000' pixel [3:0] <= bg_sel[3:0] + '1000'
Foreground '0111' pixel [3:0] <= bg_sel[3:0] + '0111'
Foreground '0110' pixel [3:0] <= bg_sel[3:0] + '0110'
Foreground '0101' pixel [3:0] <= bg_sel[3:0] + '0101'
Foreground '0100' pixel [3:0] <= bg_sel[3:0] + '0100'
Foreground '0011' pixel [3:0] <= bg_sel[3:0] + '0011'
Foreground '0010' pixel [3:0] <= bg_sel[3:0] + '0010'
Foreground '0001' pixel [3:0] <= bg_sel[3:0] + '0001'
Background '0000' pixel [3:0] <= bg_sel[3:0]

### Palette Address and map

| | | | |
|---|---|---|---|
| P0 | P1 | P2 | P3 |
| P4 | P5 | P6 | P7 |
| P8 | P9 | P10 | P11 |
| P12 | P13 | P14 | P15 |

Figure 8: OSD Palette

| Palette N | Palette Address | Bits [23:16] | Bits [15:8] | Bits [3:0] |
|---|---|---|---|---|
| Palette 0 | 0 | R0[3:0] | G0[3:0] | B0[3:0] |
| Palette 1 | 1 | R1[3:0] | G1[3:0] | B1[3:0] |
| Palette 2 | 2 | R2[3:0] | G2[3:0] | B2[3:0] |
| … | … | | | |
| Palette 15 | 15 | R15[3:0] | G15[3:0] | B15[3:0] |

Figure 9 Palette Address And Map



## OSD Character Map

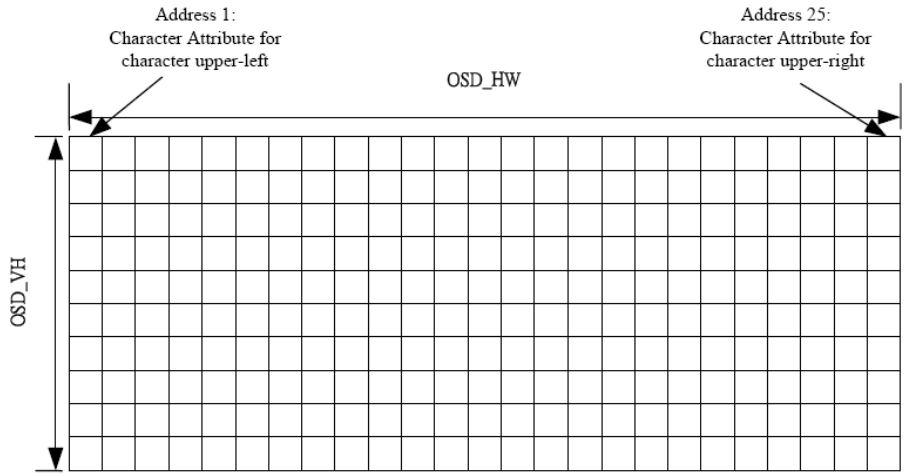


Figure 10: OSD Character Map



## OSD Font Definitions

### One Bit per pixel

One bit per pixel font definitions are arranged in Color Character Font SRAM Memory on a 12-bit by 18-address grid.

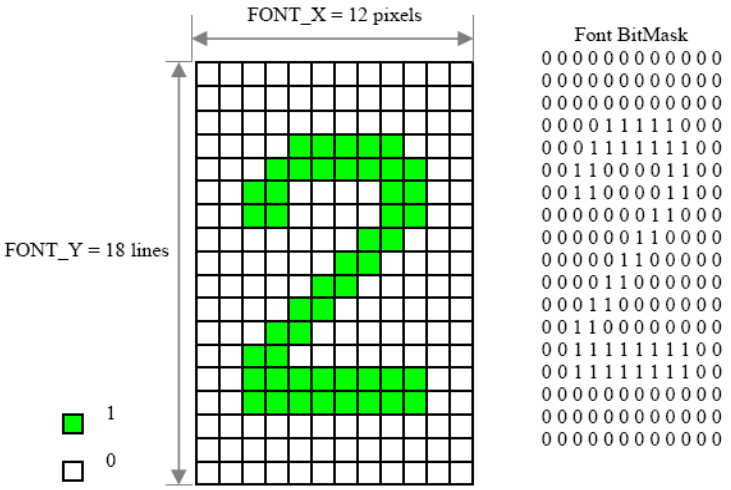


Figure11: One Bit per Pixel Font

**Two Bit per pixel**

Two bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 18 addresses.

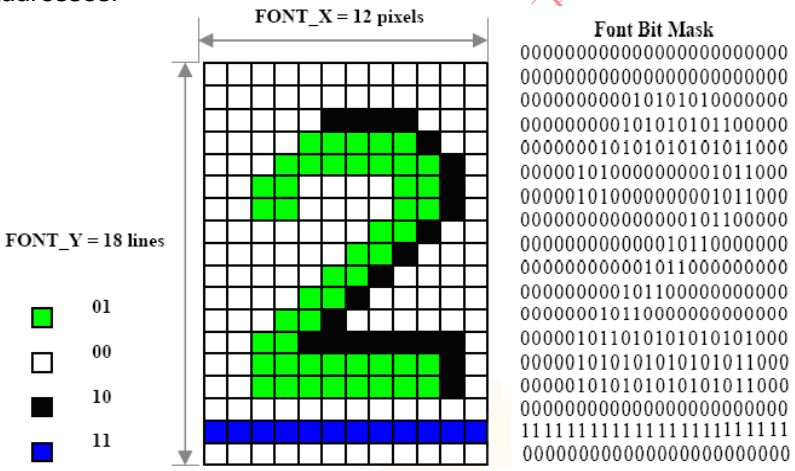


Figure 12: Two Bit per Pixel Font

**Four Bit per pixel**

Four bits per pixel font definitions are arranged in Color Character Font SRAM Memory on a 24-bit by 36 addresses.

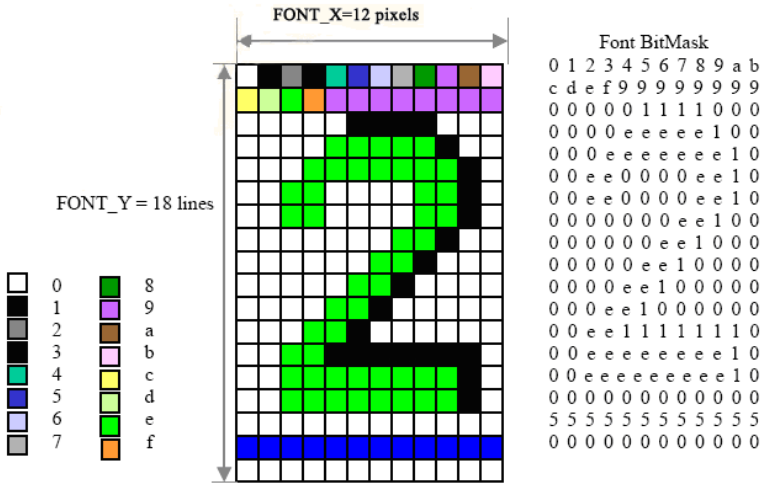


Figure 13: Four Bit per Pixel Font

**OSD Frame Definition:**

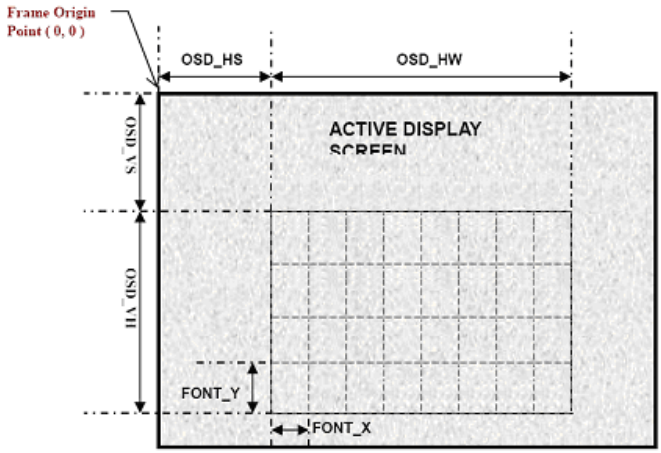


Figure 14: OSD Active Frame

OSD_HS : OSD frame horizontal start (0 – 4095 pixels)
OSD_HW : OSD frame horizontal width (1 – 64 chars)
OSD_VS : OSD frame vertical start (0 – 2047 pixels)
OSD_VH : OSD frame vertical height (1 – 32 chars)
FONT_X : Font X size (12/10 pixels)
FONT_Y : Font Y size (16/18 lines)

## 2.4.8. LVDS Driver

**Display Output Timing**

The display output port sends single/double/quad pixel data transfer and synchronized display timing to an external device. The display port also support display panel with 6-bit per

color, turn on the dithering function to enhance color depth. It can also support RGB888/RGB666/RGB565 for TTL interface panel with LVDS ports.

**LVDS transmitter can support the following:**

1. Single, double or quad pixel mode
2. 24/48/96-bit panel mapping to the LVDS channels
3. 18/36/72-bit panel mapping to the LVDS channels
4. Programmable LVDS ports swapping
5. Programmable channel swapping

In single pixel output mode, single pixel data (24-bit RGB, 4 LVDS data streams) is transferred to display port odd on each active edge of LVDS_CLK, the rate of LVDS_CLK is also equal to display pixel clock. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 15:

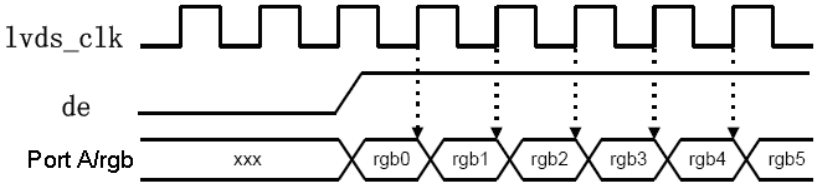


Figure 15: Single Pixel Mode Display Data Timing

In double pixel output mode, double pixel data (48-bit RGB, 8 LVDS data streams) is transferred to display port odd & even on each active edge of LVDS_CLK and the rate of LVDS_CLK is equal to half display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 16:

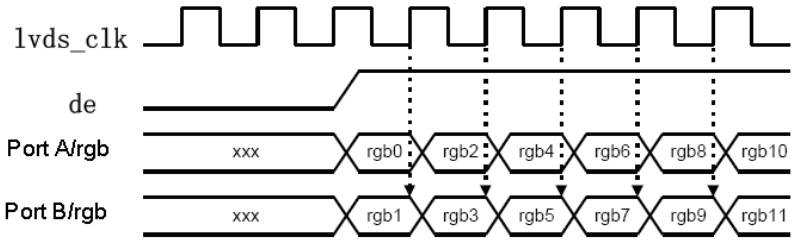


Figure 16: Double Pixel Mode Display Data Timing

In quadruple pixel output mode, quadruple pixel data (96-bit RGB, 16 LVDS data streams) is transferred to display port A/B/C/D on each active edge of LVDS_CLK and the rate of LVDS_CLK is equal to quarter display pixel clock at this moment. The sync & enable signals are also sent to display port on each active edge of LVDS_CLK. Shown on Figure 17:

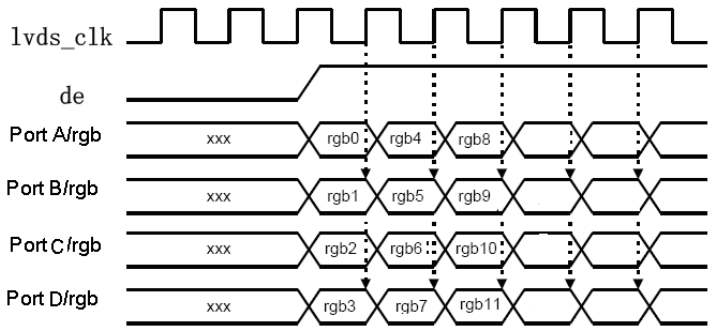


Figure 17: quadruple Pixel Mode Display Data Timing

**Output TTL RGB data can support:**

1. RGB888, D[23:0] = {R[7:0], G[7:0], B[7:0]}
2. RGB666, D[23:0] = {6'h00, R[7:2], G[7:2], B[7:2]}
3. RGB565, D[23:0] = {8'h00, R[7:3], G[7:2], B[7:3]}

For easy PCB layout, output data ports D0-D23 can be switched as following:

| Output Port | Default RGB | R/B Swap | LSB/MSB Swap |
|---|---|---|---|
| D0 | B[0] | R[0] | B[7] |
| D1 | B[1] | R[1] | B[6] |
| D2 | B[2] | R[2] | B[5] |
| D3 | B[3] | R[3] | B[4] |
| D4 | B[4] | R[4] | B[3] |
| D5 | B[5] | R[5] | B[2] |
| D6 | B[6] | R[6] | B[1] |
| D7 | B[7] | R[7] | B[0] |
| D8 | G[0] | G[0] | G[7] |
| D9 | G[1] | G[1] | G[6] |
| D10 | G[2] | G[2] | G[5] |
| D11 | G[3] | G[3] | G[4] |
| D12 | G[4] | G[4] | G[3] |
| D13 | G[5] | G[5] | G[2] |
| D14 | G[6] | G[6] | G[1] |
| D15 | G[7] | G[7] | G[0] |
| D16 | R[0] | B[0] | R[7] |
| D17 | R[1] | B[1] | R[6] |
| D18 | R[2] | B[2] | R[5] |
| D19 | R[3] | B[3] | R[4] |
| D20 | R[4] | B[4] | R[3] |
| D21 | R[5] | B[5] | R[2] |
| D22 | R[6] | B[6] | R[1] |
| D23 | R[7] | B[7] | R[0] |

### 2.4.9. Digital Audio Input/output Interface

Audio data is applied to the internal DAC filters via the digital audio interface. Four interface formats are supported:

- $I^2S$ mode
- Right 16bit Justified mode
- Right 24bit Justified mode
- Left 24bit Justified mode

The audio RX supports word lengths of 16-32 bits in I2Smode. In I2S mode, the digital audio interface receives data on the DIN input. Audio data is time multiplexed with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.
25-32 bits: LRCLK must be high for a minimum of data word length BCLK and low for a minimum of data word length BCLK. The LSB will be truncated and the most significant 24 bits will be used by the internal processing.
24 bits: LRCLK must be high for a minimum of 24 BCLKs and low for a minimum for 24 BCLKs.
17-23 bits: Data must be zero padded to 24 bits and LRCLK must be high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.
16 bits: Either data must be zero padded to 24 bits or LRCLK must be high for minimum 24 BCLKs and low for a mini mum of 24 BCLKs.
OR data must be zero padded to 16 bits and LRCLK must be high for exactly 16 BLCKs and low for exactly 16 BCLKs. The device auto-detects this 16-bit packed mode and switches to 16 bit data length.
Any mask to space ratio on LRCLK is acceptable provided the above requirements are met.
In I2S mode, the MSB is sampled in the second rising edge of BCLK following a LRCLK transition.

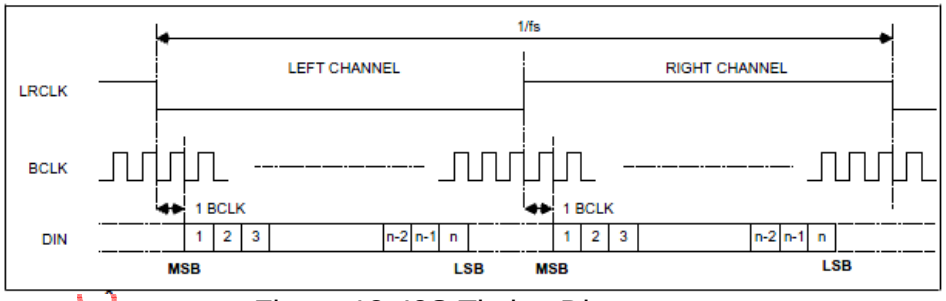


Figure 18: I2S Timing Diagram

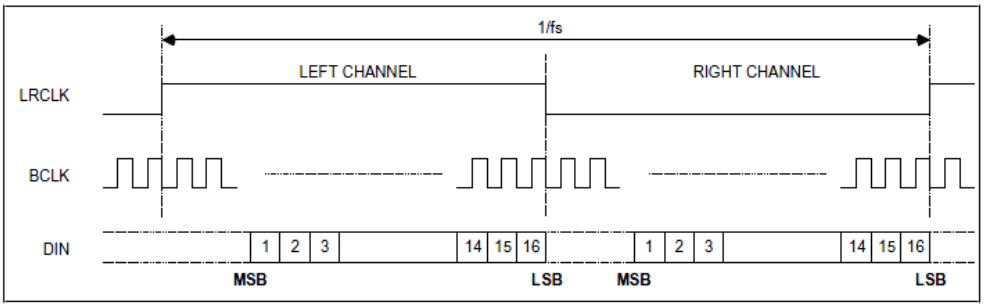


Figure 19: Right Justified Mode Timing Diagram

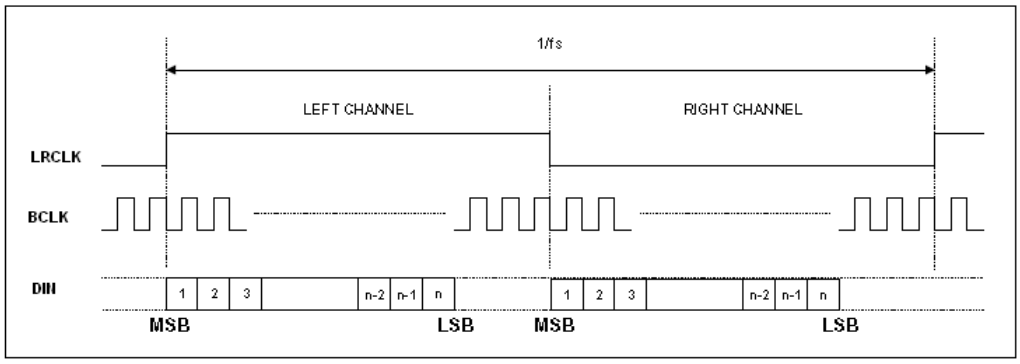


Figure 20: Left Justified Mode Timing Diagram

## 2.4.10. Two Wire Serial Bus Interface

The two wire serial bus interface is used to allow an external master to write control data, and read status from the LT8668EX registers. SCL is the serial clock and SDA is the serial data. Both lines are pulled high by resistors connected to VDD. ICs communicate on the bus by pulling SCL and SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever SCL is high.

The LT8668EX is operated as a bus slave device. The most significant 7-bits are fixed. The 7-bit address field is concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master drives SDA from high to low, while SCL is high, this is defined to be a start condition (See Figure 21). All slaves on the bus listen to determine when a start condition has been asserted.

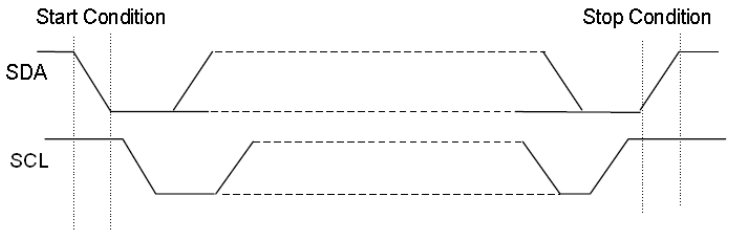


Figure 21: The Start and Stop Definition

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 22. (For the LT8668EX, the next byte is normally the index to the LT8668EX registers and is a write to the LT8668EX therefore the first R/W bit is normally low.)

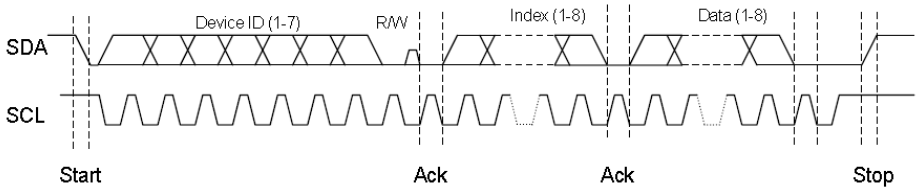


Figure 22: One Byte Write Operation

After transmitting the device address and the R/W bit, the master must release the SDA line while holding SCL low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register of theLT8668EX, the master sends another 8-bits of data, the LT8668EX loads this to the register pointed by the internal index register. The LT8668EX will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes to the LT8668EX if they are in ascending sequential order. After each 8-bit transfer the LT8668EX will acknowledge the receipt of the 8-bits with an acknowledge pulse. To end all transfers to the LT8668EX the host will issue a stop condition.

A LT8668EX read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register (See Figure 23). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the SDA line and acknowledge the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (SDA is left high during a clock pulse) and issue a stop condition.

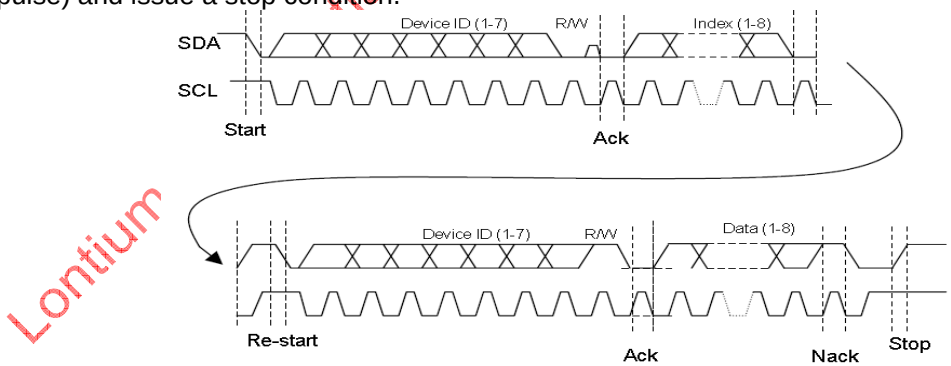


Figure 23: One Byte Read Operation

## 2.4.11. OCM (On Chip Manager)

The embedded OCM (on-chip micro-controller) serves as the system micro-controller. The OCM integrates enhanced 8051 Micro-controller. This micro-controller is fully compatible with standard 8051 instructions. The 8051 Core retains all of the features of standard 8051

and clock is up to 50MHz. OCM contains 24Kbyte memory for instruction, 1Kbyte RAM block for XDATA and 256-Byte RAM block for IDATA. Embedded MCU executes firmware program running from external flash through build-in SPI master. And the external flash ROM size is up to 32Mbyte. OCM has 8-source 2-level interrupt controller, 3 timer/counters and 1 external interrupts. In OCM, ISP mode is designed to system debug and software update on the line. In addition, it contains an 8-bit ADC for Keyboard, two PWM for backlight controller.

**OCM Feature List**

- Embedded 51 Core, and is compatible with Standard 8051 instruction
- 256 Bytes IDATA RAM
- 1K bytes on chip SRAM for XDATA
- Up to 24K bytes on chip PRAM
- Expand SFR for additional function
- 16 bits addressable I/O pins (GPIO)
- Three 16bit timer/counter fully compatible standard 8051
- One UART
- One external interrupt
- Embedded SPI master for external SPI flash
- PWM for back light control
- 8bit ADC for key pad control
- I2C BUS (slave mode)
- Support ISP(In System Program) mode

# 3. Packaging

## 3.1. ePad Enhancement

The LT8668EX is packaged in a 128-pin LQFP package with ePad.
The ePad does not need to be soldered to the PCB. The information in the following paragraphs is provided for applications which choose to solder the ePad to the PCB.
The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts. Dimensions T1 and T2 define the maximum limit of ePad size. Protrusions from the edges of the ePad may vary slightly from one package assembler to another, but all are confined to within these maximum dimensions.

## 3.2. Package Dimensions

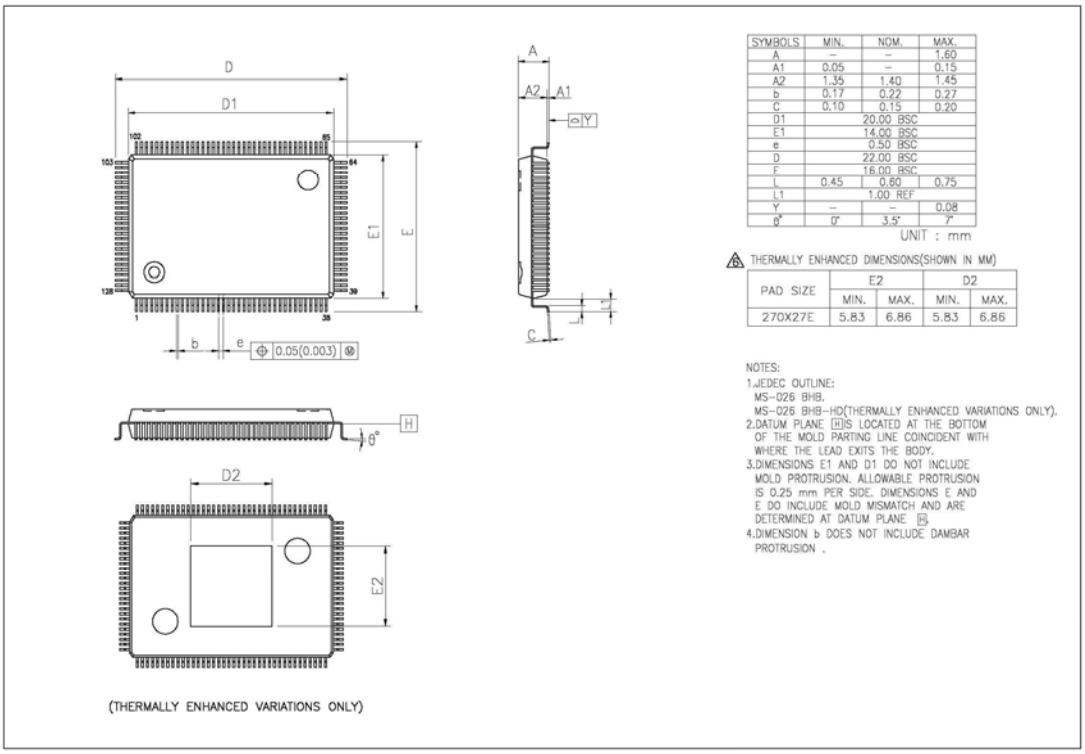


Figure 24: Mechanical Specification

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