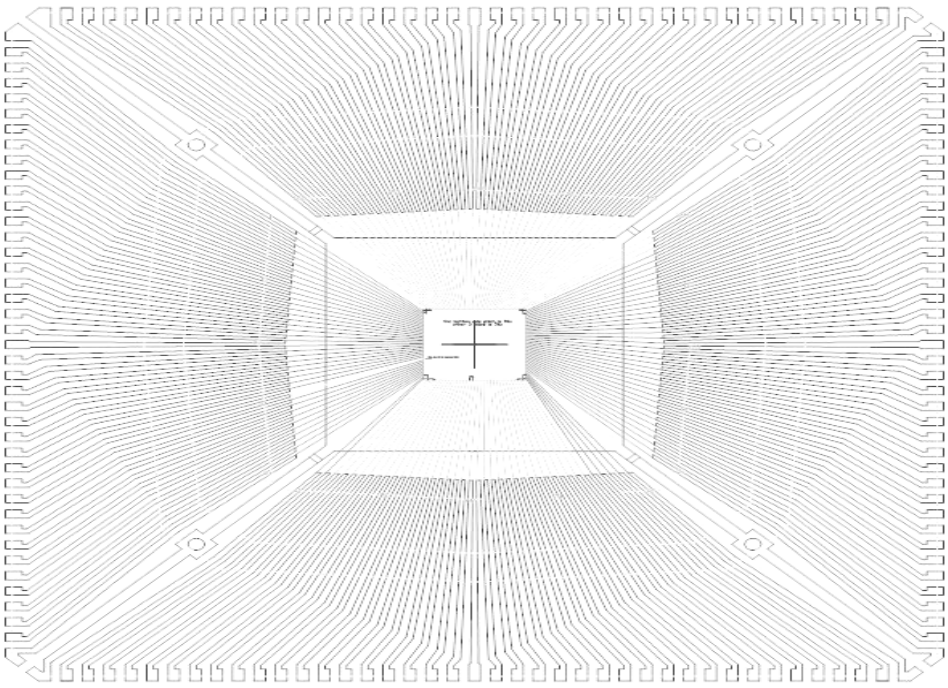
LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT8711H DP to HDMI Converter with USB Type-C Support

Data Sheet



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Revision History

Date	Owner	Notes	Version
6/15/2015	HF. Xia	Initial data sheet creation	Preliminary
6/16/2015	N. Wang	Updated package dimensions	Preliminary
11/17/2015	HF. Xia	Added power-up sequence	R1.1
3/30/2016	HF. Xia	Added LT8711H-C package information	R1.2
4/21/2016	HF. Xia	Updated power consumption	R1.3
9/30/2016	HF. Xia	Updated operating temperature range	R1.4
12/6/2016	HF. Xia	Updated features and description	R1.5
12/21/2016	HF. Xia	Updated temperature data	R1.6

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1. General Description

The LT8711H is a DisplayPort (DP) to HDMI converter, designed to connect a DP source to a HDMI sink. The LT8711H integrates a DP 1.2 compliant receiver, and a HDMI 1.4 compliant transmitter. The receiver port integrates a CC controller which enables DP Alternate Mode support when connected to a USB Type-C source.

The DP interface comprises 4 main lanes, AUX channel, and HPD signal. The receiver supports maximum 5.4Gbps (HBR2) data rate per lane. The DP receiver incorporates HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content.

The HDMI interface includes 4 TMDS clock/data pairs, DDC, and HPD signal. The HDMI transmitter is capable of supporting up to 3Gpbs data rate, quite adequate for handling video resolutions up to FHD 1080p 120Hz 3D and UHD 4k 30Hz formats. The transmitter also performs downstream RX sensing and calibrates its output swing automatically. The HDMI transmitter integrates a HDCP 1.4 encryption engine which provides digital audio-video content protection through this port.

The device is capable of automatic operation that is enabled by an integrated MCU that uses an embedded SPI flash for microcode. System control is also available through the use of a dedicated configuration I2C slave interface.

Two package types are available, LT8711H and LT8711H-C, and both are provided in a 64-lead QFN package with ePad and specified over -40℃ to +85℃ operating temperature range.

1.1 FEATURES

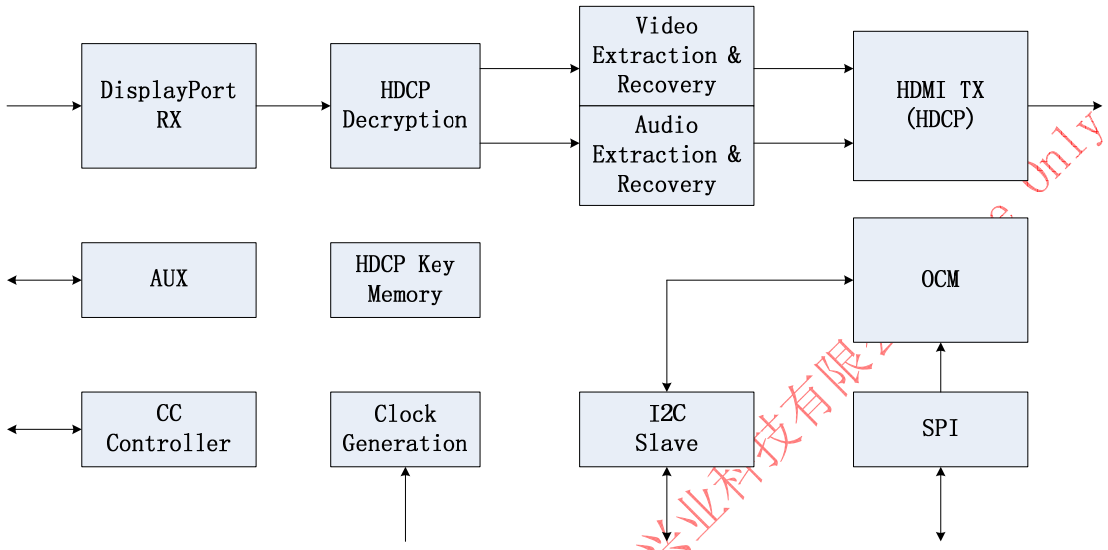
- DisplayPort receiver
  - DP 1.2 compliant
  - HDCP 1.3 compliant
  - Link rate 5.4/2.7/1.62Gbps (HBR2/HBR/RBR)
  - 1/2/4 lanes
  - Integrated CC controller for USB type-C Alt Mode support
  - 1Mbps AUX channel
  - Equalizer
- HDMI transmitter
  - HDMI 1.4 compliant
  - DVI 1.0 compliant
  - AC-couple capable
  - Data rate up to 3Gbps
  - FHD 1080p 60Hz 3D
  - UHD 4k 30Hz
  - Pre-emphasis
  - Downstream RX sensing
  - Output swing calibration
  - 5V tolerance DDC/HPD I/Os
- Integrated MCU with embedded SPI flash
- Power supply: 3.3V for I/O and 1.2V for core
- 64-pin QFN package

1.2 APPLICATIONS

- Docking station
- DP-to-HDMI dongle/adapter

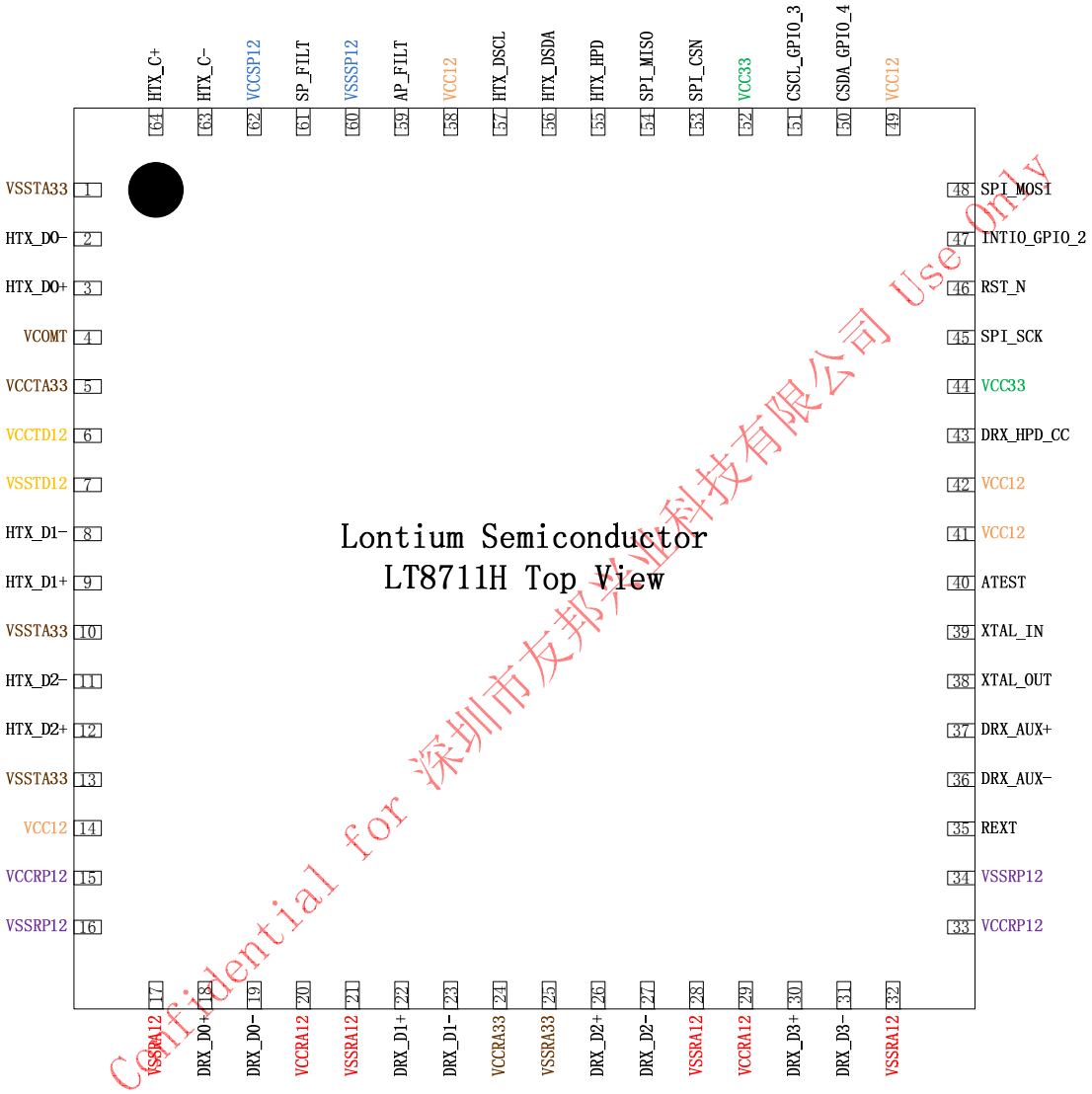
2. Function Description

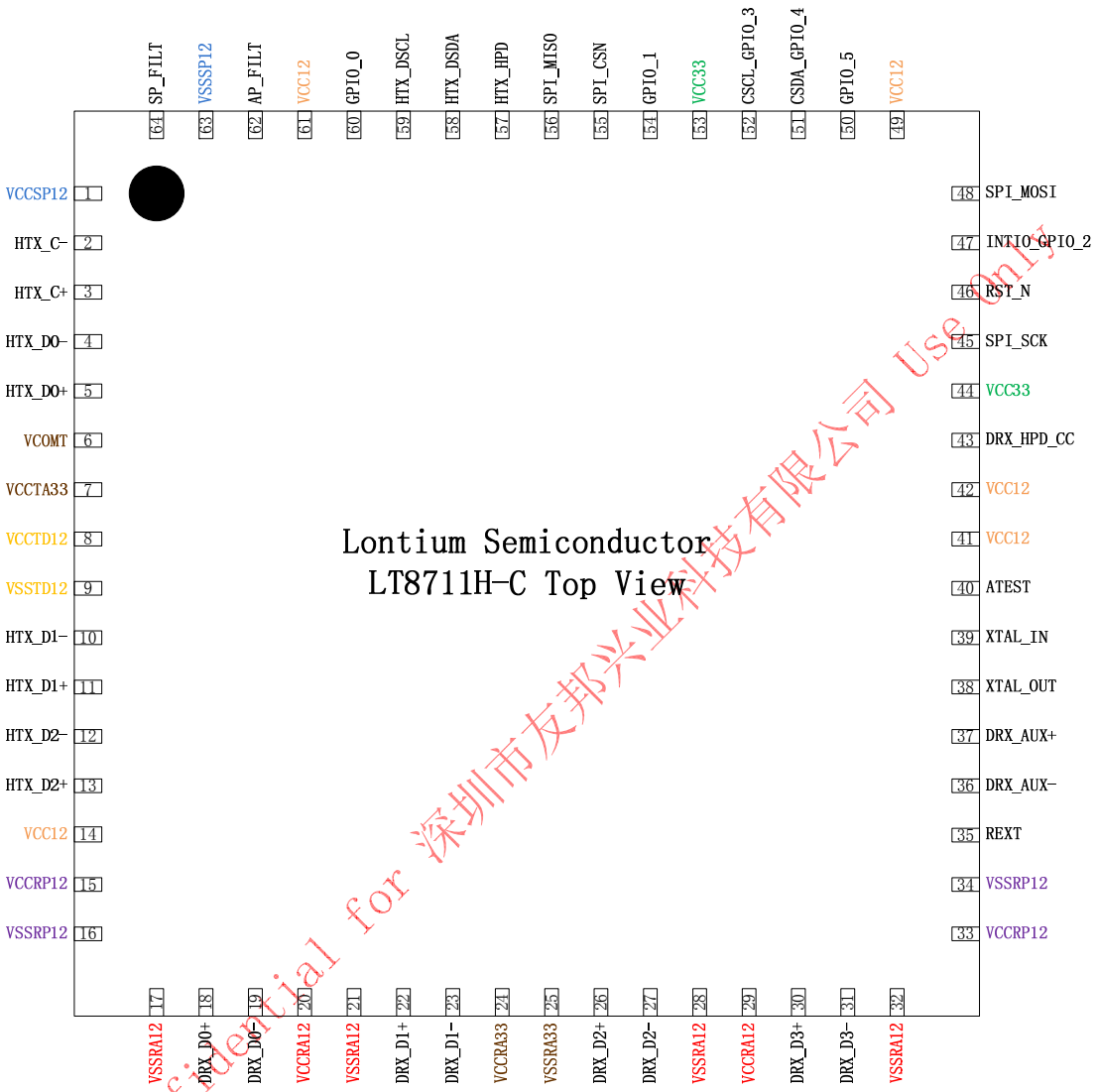
2.1 FUNCTION BLOCK DIAGRAM



2.2 PIN CONFIGURATION

Two package types are available: LT8711H and LT8711H-C.





2.3 PIN DESCRIPTIONS

LT8711H:

PIN	NAME	FUNCTION	NOTES
1, 10, 13	VSSTA33	Ground rail of 3.3V analog power for HDMI TX	
63, 64, 2, 3, 8, 9, 11, 12	HTX_C-, HTX_C+, HTX_D0-, HTX_D0+, HTX_D1-, HTX_D1+, HTX_D2-, HTX_D2+	High speed output of HDMI TX	AC-coupling capable
4	VCOMT	AC-couple biasing common ground for HDMI TX	
5	VCCTA33	Power rail of 3.3V analog power for HDMI TX	
6	VCCTD12	Power rail of 1.2V digital power for HDMI TX	
7	VSSTD12	Ground rail of 1.2V digital power for HDMI TX	
14, 41, 42, 49, 58	VCC12	Power rail of 1.2V digital core power	
15, 33	VCCRP12	Power rail of 1.2V analog power for DisplayPort RX PLL	
16, 34	VSSRP12	Ground rail of 1.2V analog power for DisplayPort RX PLL	
17, 21, 28, 32	VSSRA12	Ground rail of 1.2V analog power for DisplayPort RX	
18, 19, 22, 23, 26, 27, 30, 31	DRX_D0+, DRX_D0-, DRX_D1+, DRX_D1-, DRX_D2+, DRX_D2-, DRX_D3+, DRX_D3-	DisplayPort RX main link input	
20, 29	VCCRA12	Power rail of 1.2V analog power for DisplayPort RX	
24	VCCRA33	Power rail of 3.3V analog power for DisplayPort RX	
25	VSSRA33	Ground rail of 3.3V analog power for DisplayPort RX	
35	REXT	Analog current reference. A resistor of 2KΩ (1%) should tie this pin to VSSRA33.	
36, 37	DRX_AUX-, DRX_AUX+	DisplayPort RX AUX interface	
38, 39	XTAL_OUT, XTAL_IN	Crystal interface	
40	ATEST	Analog test pin	
43	DRX_HPD_CC	HPD output(low-driving open drain) of DisplayPort RX, which can also be configured as CC I/O in USB type-C application	5V tolerance. Optional internal 4.7kΩ pull-up.
44, 52	VCC33	Power rail of 3.3V LVTTL I/O power	
45, 48, 53, 54	SPI_SCK, SPI_MOSI, SPI_CSN, SPI_MISO	Flash SPI programming interface	Internal weak pull-down for SPI_MISO
46	RST_N	Active low reset input	Internal weak pull-up
47	INTIO_GPIO_2	GPIO 2 of on-chip MCU, shared with interrupt input or output	
50	CSDA_GPIO_4	GPIO 4 of on-chip MCU, shared with configuration I2C SDA	
51	CSCL_GPIO_3	GPIO 3 of on-chip MCU, shared with configuration I2C SCL	

55	HTX_HPD	HPD input of HDMI TX	5V tolerance
56, 57	HTX_DSDA, HTX_DSCL	DDC interface of HDMI TX	5V tolerance. Internal 20kΩ pull-up.
59	AP_FILT	Low-pass loop filter connection for audio stream PLL	
60	VSSSP12	Ground rail of 1.2V analog power for video stream PLL	
61	SP_FILT	Low-pass loop filter connection for video stream PLL	
62	VCCSP12	Power rail of 1.2V analog power for video stream PLL	
65	EPAD	Common ground	

LT8711H-C:

PIN	NAME	FUNCTION	NOTES
1	VCCSP12	Power rail of 1.2V analog power for video stream PLL	
2, 3, 4, 5, 10, 11, 12,13	HTX_C-, HTX_C+, HTX_D0-, HTX_D0+, HTX_D1-, HTX_D1+, HTX_D2-, HTX_D2+	High speed output of HDMI TX	AC-coupling capable
6	VCOMT	AC-couple biasing common ground for HDMI TX	
7	VCCTA33	Power rail of 3.3V analog power for HDMI TX	
8	VCCTD12	Power rail of 1.2V digital power for HDMI TX	
9	VSSTD12	Ground rail of 1.2V digital power for HDMI TX	
14, 41, 42, 49, 61	VCC12	Power rail of 1.2V digital core power	
15, 33	VCCRP12	Power rail of 1.2V analog power for DisplayPort RX PLL	
16, 34	VSSRP12	Ground rail of 1.2V analog power for DisplayPort RX PLL	
17, 21, 28, 32	VSSRA12	Ground rail of 1.2V analog power for DisplayPort RX	
18, 19, 22, 23, 26, 27, 30, 31	DRX_D0+, DRX_D0-, DRX_D1+, DRX_D1-, DRX_D2+, DRX_D2-, DRX_D3+, DRX_D3-	DisplayPort RX main link input	
20, 29	VCCRA12	Power rail of 1.2V analog power for DisplayPort RX	
24	VCCRA33	Power rail of 3.3V analog power for DisplayPort RX	
25	VSSRA33	Ground rail of 3.3V analog power for DisplayPort RX	
35	REXT	Analog current reference. A resistor of 2KΩ (1%) should tie this pin to VSSRA33.	
36, 37	DRX_AUX-, DRX_AUX+	DisplayPort RX AUX interface	
38, 39	XTAL_OUT, XTAL_IN	Crystal interface	
40	ATEST	Analog test pin	
43	DRX_HPD_CC	HPD output(low-driving open drain) of DisplayPort RX, which can also be configured as CC I/O in USB type-C application	5V tolerance. Optional internal 4.7kΩ pull-up.
44, 53	VCC33	Power rail of 3.3V LVTTL I/O power	
45, 48, 55, 56	SPI_SCK, SPI_MOSI, SPI_CSN, SPI_MISO	Flash SPI programming interface	Internal weak pull-down for SPI_MISO
46	RST_N	Active low reset input	Internal weak pull-up
47	INTIO_GPIO_2	GPIO 2 of on-chip MCU, shared with interrupt input or output	
50	GPIO_5	GPIO 5 of on-chip MCU	
51	CSDA_GPIO_4	GPIO 4 of on-chip MCU, shared with configuration I2C SDA	
52	CSCL_GPIO_3	GPIO 3 of on-chip MCU, shared with configuration I2C SCL	

54	GPIO_1	GPIO 1 of on-chip MCU	
57	HTX_HPD	HPD input of HDMI TX	5V tolerance
58, 59	HTX_DSDA, HTX_DSCL	DDC interface of HDMI TX	5V tolerance. Internal 20kΩ pull-up.
60	GPIO_0	GPIO 0 of on-chip MCU	
62	AP_FILT	Low-pass loop filter connection for audio stream PLL	
63	VSSSP12	Ground rail of 1.2V analog power for video stream PLL	
64	SP_FILT	Low-pass loop filter connection for video stream PLL	
65	EPAD	Common ground	

2.4 ELECTRICAL CHARACTERISTICS

Absolute maximum conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC33 VCCRA33 VCCTA33	3.3V Supply	-0.3		4.0	V
VCC12 VCCRA12 VCCRP12 VCCTD12 VCCSP12	1.2V Supply	-0.3		1.5	V
Vstg	Storage Temperature	-65		+150	℃
Tj	Junction Temperature			+150	℃

Notes:

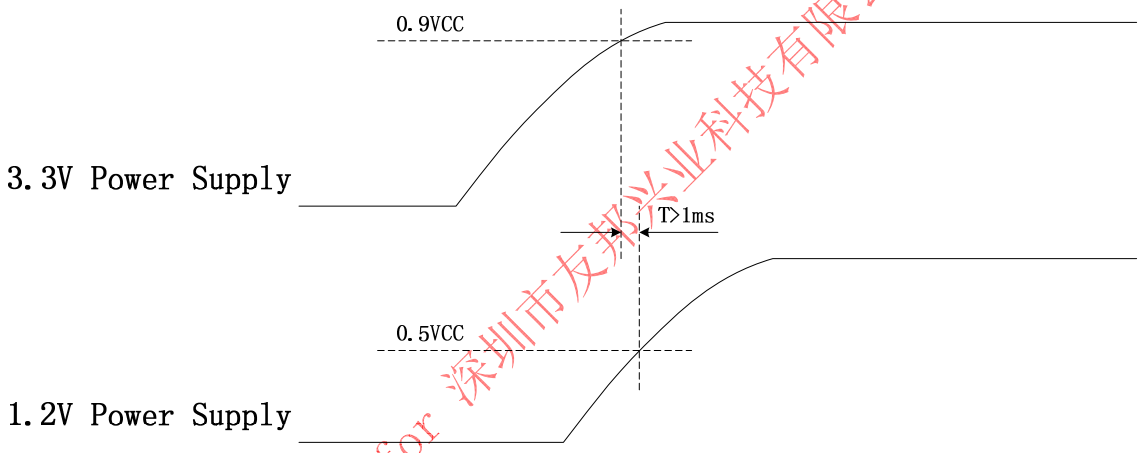
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Normal operating conditions

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
3.3V Power Supply	DC	3.0	3.3	3.6	V
1.2V Power Supply	DC	1.1	1.2	1.3	V
Supply-Noise Tolerance	DC to 500kHz			100	mVp-p
Ambient Temperature		-40		+85	℃
DP INPUTS					
Differential Input Voltage Swing	At input pin	150			mVp-p
Common-Mode Input Voltage		0		2	V
Input Resistance	Single-ended	45	50	55	Ω
HDMI OUTPUTS					
Differential Output-Voltage Swing	50 ohm load	800	1000	1200	mVp-p
Output-Voltage High	Single-ended	VCCTA33			V
Output-Voltage Low	Single-ended	VCCTA33-0.6		VCCTA33-0.4	V
Output Voltage During Power-Down	Single-ended	VCCTA33-0.01		VCCTA33+0.01	V
Common-Mode Output Voltage	50 ohm load	VCCTA33-0.3		VCCTA33-0.2	V
Rise /Fall Time	20% to 80%	100	150	200	ps
LVTTL CONTROL AND STATUS INTERFACE					
LVTTL Input High Voltage		2.0			V
LVTTL Input Low Voltage				0.8	V
Open-Drain Output High	R_{LOAD} 2kΩ to VCC33	2.4			V
Open- Drain Output Low	R_{LOAD} 2kΩ to VCC33			0.4	V
Open- Drain Output Sink Current				5	mA
Supply Current					

Normal operation: HBR2, 4-lane, 2160p@30Hz	3.3V	113	mA
	1.2V	399	mA
Normal operation: HBR, 4-lane, 1080p@60Hz	3.3V	113	mA
	1.2V	366	mA
Normal operation: RBR, 4-lane, 720p@60Hz	3.3V	113	mA
	1.2V	348	mA
Normal operation: Idle State	3.3V	22	mA
	1.2V	195	mA

2.5 POWER-UP SEQUENCE



3. Packaging

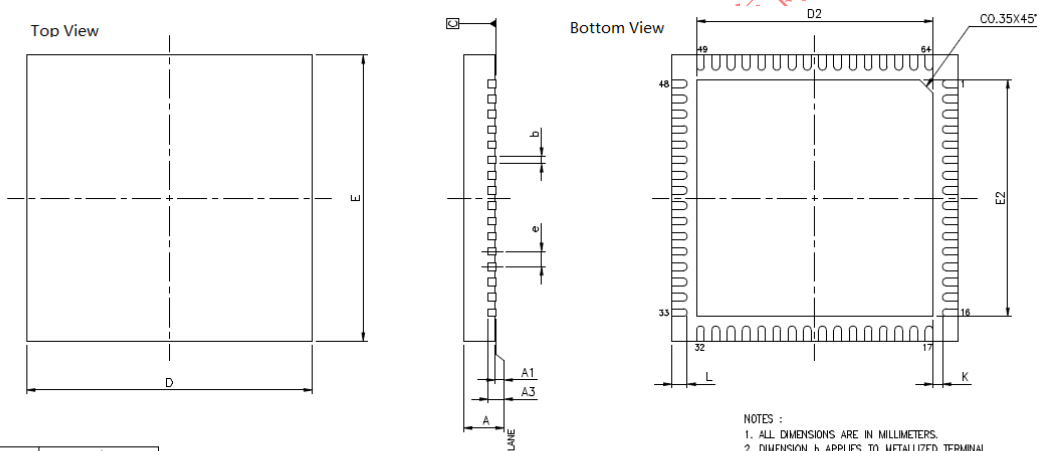
3.1 ePad ENHANCEMENT

The LT8711H/LT8711H-C is packaged in a 64-pin QFN package with ePad.

The ePad must be soldered to the PCB ground. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

3.2 PACKAGE DIMENSIONS



JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X252 MIL	6.10	6.20	6.25	6.10	6.20	6.25	X	V	N/A