LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT9211

2-Port LVDS/MIPI/TTL to 2-Port LVDS/MIPI/TTL Converter

Datasheet

1. Features

- **MIPI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - Two Port Simultaneous Display Supported
  - Up to 1.8Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Dual-Port LVDS Transmitter**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - Two Port Simultaneous Display Supported
  - Up to 1080P 60Hz
  - Data Port ,Data Lane and Polarity Swapping
  - Programmable Pre-emphasis
  - Support output SSC(30KHz±5%)
- **TTL Output**
  - Support 24-bit RGB and BT656/BT1120
  - Both DDR and SDR supported
  - Support both 1.8V and 3.3V Voltage Output
  - Resolution up to 1080P 60Hz
- **MIPI Receiver**
  - Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - Two Port Input switchable
  - Up to 1.8Gb/s per Data Lane
  - Resolution Up to 1080P 60Hz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Dual-Port LVDS Receiver**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - Up to 1080P 60Hz
  - Data Port ,Data Lane and Polarity Swapping
  - Internal Rterm Calibration with Less than 5% Error
  - Programmable Equalization
  - Support input Dessc(30KHz±5%)
- **TTL Input**
  - Support 24-bit RGB and BT656/BT1120
  - Both DDR and SDR supported
  - Support both 1.8V and 3.3V Input Voltage
  - Resolution up to 1080P 60Hz
- **Miscellaneous**
  - 1.8V and 3.3V Power Supply
  - Alternative Input and Output configuration for LVDS/TTL/MIPI
  - MIPI/LVDS muxer and splitter supported
  - MIPI-LVDS Levelshifter for FPGA
  - Support 100KHz and 400KHz I2C Slave
  - External 25MHz Crystal Reference Clock
  - Temperature Range: -40°C ~ +85°C
  - Packaged in QFN64 7.5mm x 7.5mm

2. General Description

The Lontium LT9211 is a high performance convertor which interconvertible between MIPI DSI/CSI-2/Dual-Port LVDS and TTL except for TTL to TTL. The LT9211 deserializes input MIPI/LVDS/TTL video data, decodes packets, and converts the formatted video data stream to MIPI/LVDS/TTL transmitter output between AP and mobile display panel or camera.

The LT9211 can be used as 2-Port MIPI/LVDS Repeater which support maximum 14dB input equalization and programmable pre-emphasis to improve performance.

The LT9211 can also be used as MIPI/LVDS Muxer and Splitter.

The LT9211 is fabricated in advanced CMOS process and implemented in 7.5x7.5mm QFN64 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

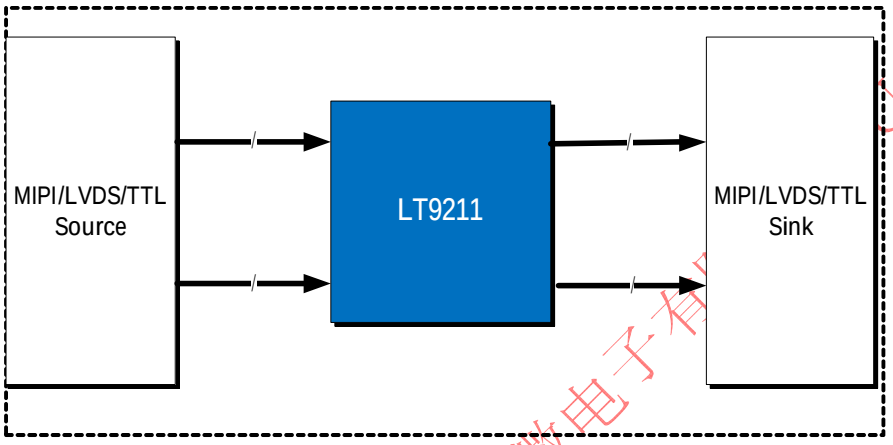


Figure 3.1 LT9211 Typical Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
LT9211	-40°C to +85°C	QFN64 (7.5*7.5)	

5. IC Version Information

Table 5.1 IC Version Information

Version	Mark
LT9211	

Table of Contents

6. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	03/30/2018
R2.0	Y C	Change input and output data format	07/10/2018

7. Pinning Information

7.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance a. Maximum trace length mismatch should be less than 2.5mil and keep total trace length to a minimum for all differential traces. It is highly recommended to route differential pairs on top or bottom layer with no vias on signal path.

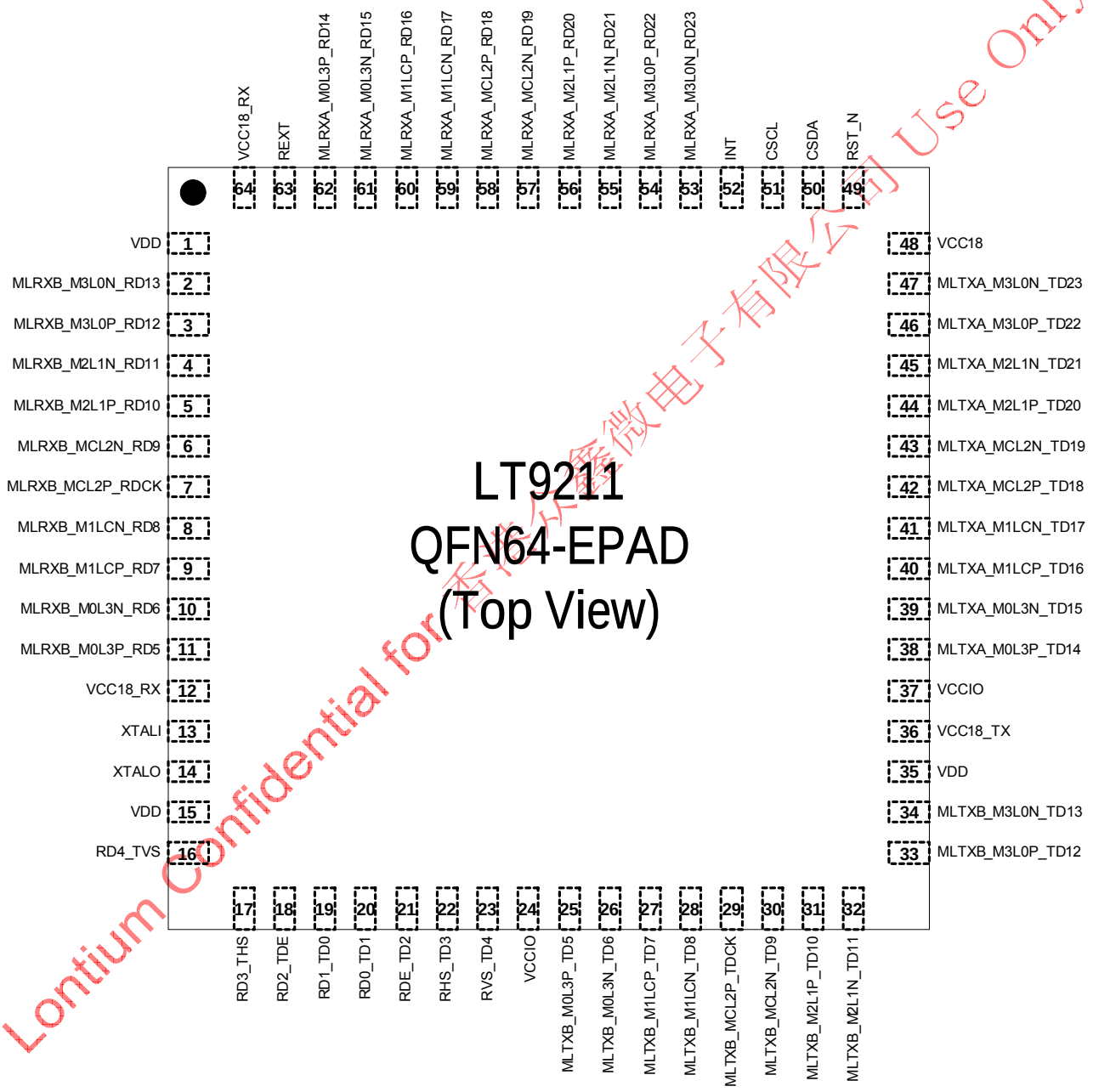


Figure 7.1.1 QFN64 Pin Configuration

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT9211 1.8V/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power input pins must be minimized.

7.2 Pin Description

Table 7.2.1 QFN64 Pin Description

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
53,54	MLRXA_M3L0N_RD23 MLRXA_M3L0P_RD22	Analog	I	**Port-A MIPIRX Lane-3/LVDSRX Lane-0 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
55,56	MLRXA_M2L1N_RD21 MLRXA_M2L1P_RD20	Analog	I	**Port-A MIPIRX Lane-2/LVDSRX Lane-1 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
57,58	MLRXA_MCL2N_RD19 MLRXA_MCL2P_RD18	Analog	I	**Port-A MIPIRX Lane-C/LVDSRX Lane-2 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
59,60	MLRXA_M1LCN_RD17 MLRXA_M1LCP_RD16	Analog	I	**Port-A MIPIRX Lane-1/LVDSRX Lane-C and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
61,62	MLRXA_M0L3N_RD15 MLRXA_M0L3P_RD14	Analog	I	**Port-A MIPIRX Lane-0/LVDSRX Lane-3 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
2,3	MLRXB_M3L0N_RD13 MLRXB_M3L0P_RD12	Analog	I	**Port-B MIPIRX Lane-3/LVDSRX Lane-0 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
4,5	MLRXB_M2L1N_RD11 MLRXB_M2L1P_RD10	Analog	I	**Port-B MIPIRX Lane-2/LVDSRX Lane-1 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
6,7	MLRXB_MCL2N_RD9 MLRXB_MCL2P_RDCK	Analog	I	**Port-B MIPIRX Lane-C/LVDSRX Lane-2 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
8,9	MLRXB_M1LCN_RD8	Analog	I	**Port-B MIPIRX Lane-1/LVDSRX Lane-C and TTL Input**

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
	MLRXB_M1LCP_RD7			MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
10,11	MLRXB_M0L3N_RD6 MLRXB_M0L3P_RD5	Analog	I	**Port-B MIPIRX Lane-0/LVDSRX Lane-3 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
16,17 18,19 20,21 22,23	RD4_TVS,RD3_THS RD2_TDE,RD1_TD0 RD0_TD1,RDE_TD2 RHS_TD3,RVS_TD4	Analog	I/O	**TTL Data and Control Signal and Debug Gpo Output** These Pins can be selected as TTL input or output. Also, they can be configured as outputs for debug function.
38,39	MLTXA_M0L3P_TD14 MLTXA_M0L3N_TD15	Analog	O	**Port-A MIPITX Lane-0/LVDSTX Lane-3 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
40,41	MLTXA_M1LCP_TD16 MLTXA_M1LCN_TD17	Analog	O	**Port-A MIPITX Lane-1/LVDSTX Lane-C and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
42,43	MLTXA_MCL2P_TD18 MLTXA_MCL2N_TD19	Analog	O	**Port-A MIPITX Lane-C/LVDSTX Lane-2 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
44,45	MLTXA_M2L1P_TD20 MLTXA_M2L1N_TD21	Analog	O	**Port-A MIPITX Lane-2/LVDSTX Lane-1 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
46,47	MLTXA_M3L0P_TD22 MLTXA_M3L0N_TD23	Analog	O	**Port-A MIPITX Lane-3/LVDSTX Lane-0 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
25,26	MLTXB_M0L3P_TD5 MLTXB_M0L3N_TD6	Analog	O	**Port-B MIPITX Lane-0/LVDSTX Lane-3 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
27,28	MLTXB_M1LCP_TD7 MLTXB_M1LCN_TD8	Analog	O	**Port-B MIPITX Lane-1/LVDSTX Lane-C and TTL Output** MIPI output of polarity swappable differential pairs up to

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
				1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
29,30	MLTXB_MCL2P_TDCK MLTXB_MCL2N_TD9	Analog	O	**Port-B MIPITX Lane-C/LVDSTX Lane-2 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
31,32	MLTXB_M2L1P_TD10 MLTXB_M2L1N_TD11	Analog	O	**Port-B MIPITX Lane-2/LVDSTX Lane-1 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
33,34	MLTXB_M3L0P_TD12 MLTXB_M3L0N_TD13	Analog	O	**Port-B MIPITX Lane-3/LVDSTX Lane-0 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
63	REXT	Analog	I/O	**BandGap External Resistor** External 6.04K (1%) resistor for setting internal reference current.
13,14	XTALI XTALO	Analog	I/O	**25M Crystal oscillator interface**
49	RST_N	Schmitt	I	**Hardware Reset Input** Chip reset signal. Active LOW.
50,51	CSDA CSCL	Schmitt OPD	I/O	**I2C Serial Clk and Data Input and Output** It serves as 3.3V/1.8V serial port clk and data IO slave for register access.
52	INT	OPD CMOS	I/O	**Interrupt Request Output** This pin is interrupt request output. It can be configured as Open-drain or CMOS output, when configured as CMOS output, the output high voltage is 1.8V.
12,64	VCC18_RX	PWR	I/O	**1.8V RX Power** 1.8V power for RX.
36	VCC18_TX	PWR	I/O	**1.8V TX Power** 1.8V power for TX.
24,37	VCCIO	PWR	I/O	**IO Power** 1.8V or 3.3V power for TTL input, when 3.3V TTL voltage level input, it should be connect to 3.3V.
48	VCC18	PWR	I/O	**1.8V Power for Control Signal** 1.8V power for control signal.
1,15,35	VDD	PWR	I/O	**1.8V Power** 1.8V power for digital block.
129	#EPAD	—	—	**EPAD** Connect to VSS on PCB.

8. Function Description

8.1 Function Block Diagram

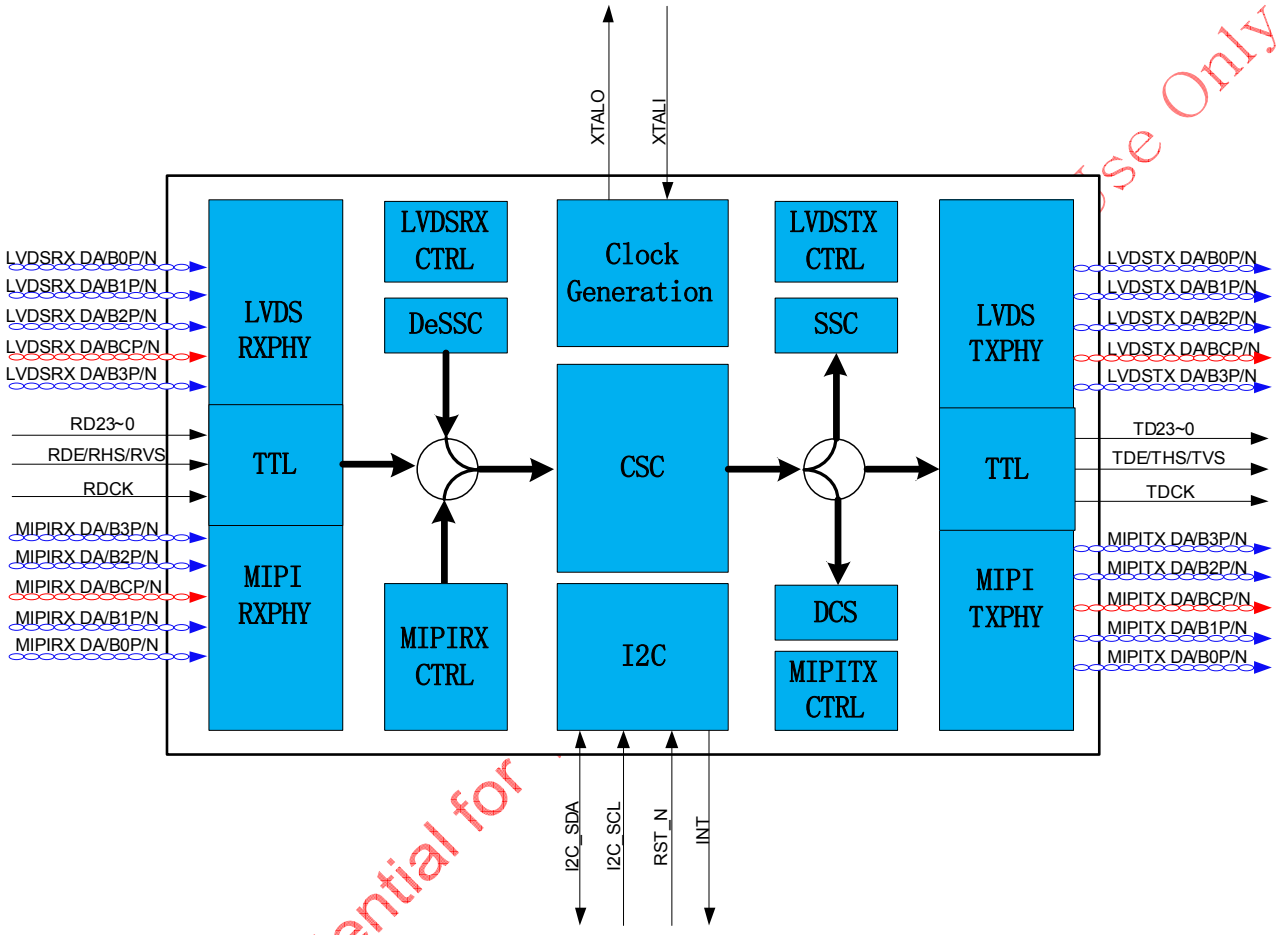


Figure 8.1.1 Function Block Diagram

9. Specification

9.1 Absolute Maximum Conditions

Table 9.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18,VDD	1.8V Power Supply Voltage	-0.3		2.0	V
VCCIO	1.8V/3.3V Power Supply Voltage	-0.3		3.63	V
V_I	CMOS Terminal Input Voltage Range	-0.3		2.0	V
V_O	CMOS Terminal Output Voltage Range	-0.3		2.0	V
T_S	Storage Temperature	-55		125	℃
ESD	HBM Elastrostatic Discharge Level		4K		V
Notes: 1. Permanent device damage may occur if absolute maximum conditions are exceeded. 2. Function operation should be restricted to the conditions described under Normal Operating Conditions.					

9.2 Normal Operating Conditions

Table 9.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18,VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCCIO	1.8V/3.3V Power Supply Voltage	1.62		3.63	V
VCC_N	Power Supply Voltage Noise			50	mV
T_A	Operating Free-air Temperature	-40	27	85	℃

9.3 DC Characteristics

Table 9.3.1 DC Characteristics

MIPI HS Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70	200	330	mV
Rterm	Differential input impedance	80	100	125	Ω
MIPI LP Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIL	Input low voltage			550	mV
VIH	Input high voltage，data rate<1.5Gbps	880			mV
	Input high voltage，data rate>1.5Gbps	740			mV
VHYST	Input hysteresis	25			mV
MIPI HS Line Transmitter DC Specifications					

Symbol	Parameter	MIN	TYP	MAX	Unit
Vcm	HS Transmit Static Common mode Voltage	150	200	250	mV
∆Vcm	HS Transmit Static Common mode Voltage Mismatch			5	mV
Vod	HS Transmit Differential Voltage	140	200	270	mV
∆Vod	HS Transmit Differential Voltage Mismatch			14	mV
Vohhs	HS Transmit Output High Voltage			360	mV
Zos	Single ended output impedance	40	50	62.5	Ω
∆Zos	Single ended output impedance Mismatch			10	%
MIPI LP Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOL	Output low-level SE voltage	-50	0	50	mV
VOH	Output high-level SE voltage	1.1	1.2	1.3	V
ZOLP	Single-ended output impedance	110			Ω
∆ZOLP(01,10)	Single-ended output impedance mismatch driving opposite level			20	%
∆ZOLP(00,11)	Single-ended output impedance mismatch driving same level			5	%
LVDS Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			50	mV
VIDTL	Differential input low voltage threshold	-50			mV
VCMRXDC	Input common mode voltage	0	1200	1800	mV
Rterm	Termination Resister	80	100	125	Ω
VIDTH	Differential input high voltage threshold			50	mV
LVDS Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOD	Differential Out Voltage: RL=100Ω	150	350	500	mV
ΔVOD	Change in VOD between complementary output states: RL=100Ω			35	mV
VOC	Common Mode Voltage: RL=100Ω	1.1	1.25	1.4	V
ΔVOC	Change in VOC between complementary output states: RL=100Ω			35	mV
IOS	Output Short Circuit Current : Vout=0V，RL=100Ω			-24	mA
IOZ	Output TRI-STATE Current: Vout=0V to Vcc			±10	uA

9.4 AC Characteristics

Table 9.4.1 AC Characteristics

MIPI HS Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
ΔVCMRX(HF)	Common mode interference beyond 450MHz			200	mVpp
ΔVCMRX(LF)	Common mode interference between 50MHz and 450MHz.	-50		50	mVpp
Ccm	Common mode termination			60	pF
Rterm	Termination Resister	80	100	125	Ω
MIPI LP Line Receiver AC Specifications					

Symbol	Parameter	MIN	TYP	MAX	Unit
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
MIPI HS Line Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
ΔVcmtx(hf)	Common mode Voltage variation above 450MHz			15	mVrms
ΔVcmtx(lf)	Common mode Voltage variation between 50-450MHz			25	mVpeak
Rise/Fall Time 20%-80%	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
	Data rate >1.5Gbps	50		0.4UI	ps
MIPI LP Line Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
trlp , tflp	Single ended output rise/fall time,15% to 85%, CL< 70pF			25	ns
treot	Single ended output rise/fall time,30% to 85%, CL< 70pF			35	ns
TLP-PULSE-TX	Pulse width of the LP exclusive-OR clock	20			ns
TLP-PER-TX	Period of the LP exclusive-OR clock	90			ns
δV/δtSR	Slew rate @ CLOAD = 0			500	mV/ns
	Slew rate @ CLOAD = 5pF			350	mV/ns
	Slew rate @ CLOAD = 20pF			250	mV/ns
	Slew rate @ CLOAD = 70pF			150	mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Falling Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30			mV/ns
	Slew rate @ CLOAD = 0 to 70pF (Rising Edge Only)	30–0.075*(VO,INST-700)			mV/ns
LVDS Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
CLK	output clk cycle	6.25	Tc	37	ns
T0	Input data position0	-0.15	0	0.15	ns
T1	Input data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Input data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Input data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Input data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Input data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Input data position6	6Tc/7-0.15		6Tc/7+0.15	ns
LVDS Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
CLK	output clk cycle	6.25	Tc	37	ns
trise	VOD rise time, 20% to 80%	250	350	500	ps
tfall	VOD fall time, 20% to 80%	250	350	500	ps
T0	Output data position0	-0.15	0	0.15	ns
T1	Output data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Output data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Output data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Output data position4	4Tc/7-0.15		4Tc/7+0.15	ns

T5	Output data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Output data position6	6Tc/7-0.15		6Tc/7+0.15	ns

9.5 Power Consumption

Table 9.5.1 MIPI to LVDS Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.2 MIPI to TTL Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.3 MIPI to MIPI Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.4 LVDS to LVDS Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.5 LVDS to TTL Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.6 LVDS to MIPI Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.7 TTL to MIPI Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

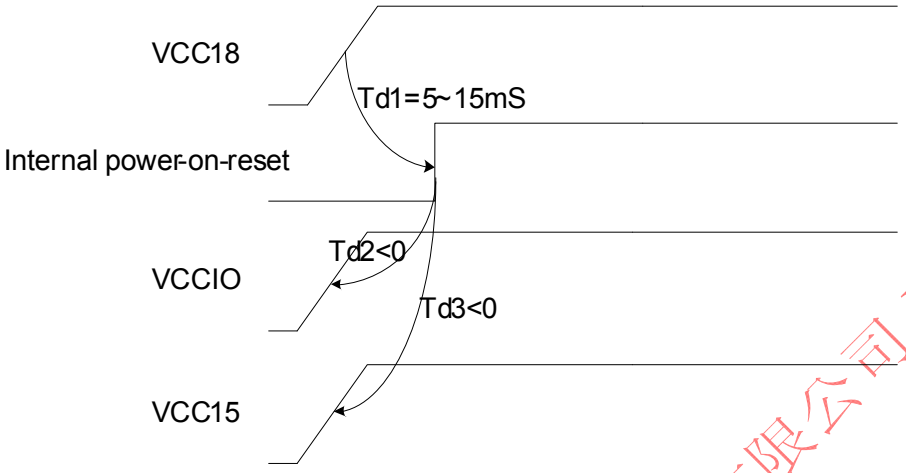
Table 9.5.8 TTL to LVDS Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

Table 9.5.9 TTL to TTL Power Consumption

Symbol	Resolution	Power Consumption	Unit
I_{VCC18}	1080P	TBD	mA
I_{VCC15}		TBD	mA
I_{VCCIO}		TBD	mA

9.6 Power-up and Reset Sequence



Note：Internal power-on-reset is generated by VCC18, VCCIO and VCC15 should be stable when Internal power-on-reset is high.

Figure 9.6.1 Power-up Sequence

10. Package Information

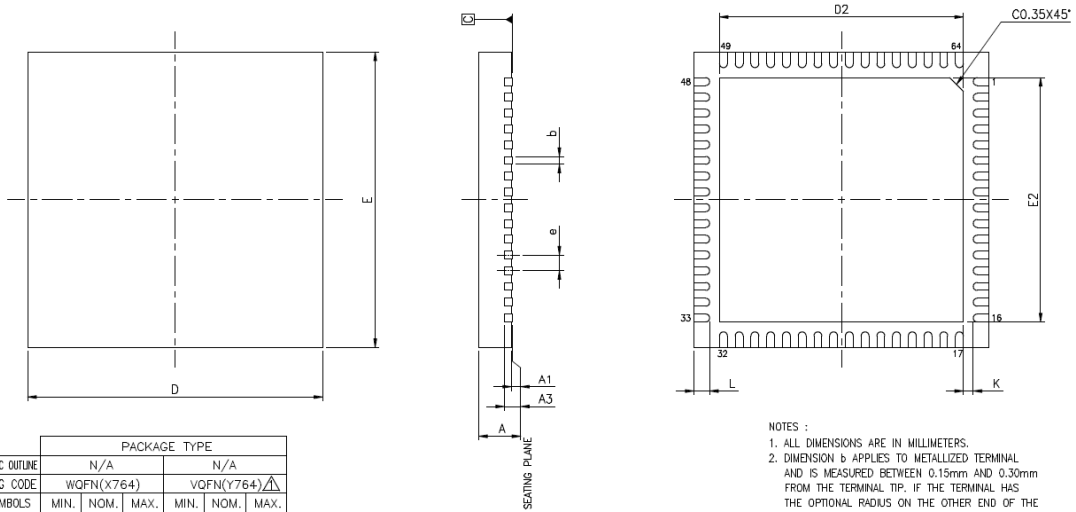
10.1 ePad Enhancement

The LT9211 is packaged in QFN64 package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

10.2 Package Dimensions



	PACKAGE TYPE					
JEDEC OUTLINE	N/A			N/A		
PKG CODE	WQFN(X764)			VQFN(Y764)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.20 REF.			0.20 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	7.50 BSC			7.50 BSC		
E	7.50 BSC			7.50 BSC		
e	0.40 BSC			0.40 BSC		
L	0.30	0.40	0.50	0.30	0.40	0.50
K	0.20	—	—	0.20	—	—

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
252X252 MIL	6.10	6.20	6.25	6.10	6.20	6.25	X	V	N/A

Figure 10.2.1 QFN64 Package Dimensions

Visit our corporate web page at: www.lontiumsemi.com
Technical support: support@lontium.com
Sales: sales@lontium.com