



SAMSUNG TFT-LCD

**MODEL: LTA550HQ23-W**

The Information described in this specification is for the first draft and can be changed without prior notice.

Samsung Display Co., LTD

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## General Description

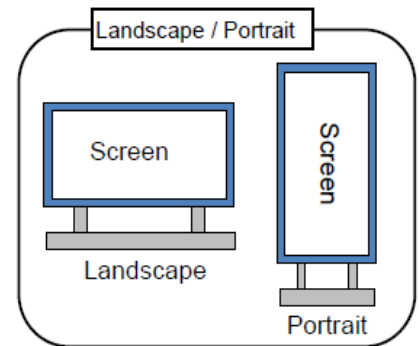
### Description

LTA550HQ23 is a color active matrix liquid crystal display (LCD) that uses amorphous silicon TFT (Thin Film Transistor) as switching components. This model is composed of a TFT LCD panel, a driver circuit, and a back-light unit. This 46.0" model has a resolution of 1920 x 1080 pixels (16:9) can display up to 1.07 Billion colors (Dithering) with the wide viewing angle of 89° or higher in all directions. This panel is intended to support applications by providing an excellent performance for the display products with a flat panel such as Home-alone Multimedia TFT-LCD TV and a High Definition TV.

## General Information

### Features

- High contrast ratio & aperture ratio with the wide color gamut
- SVA (Super Vertical Align) mode
- Wide viewing angle ( $\pm 178^\circ$ )
- High speed response
- FHD resolution (16:9)
- Edge Type LED (Light Emitted Diode) BLU
- ROHS compliance (Pb-free)
- Low power consumption
- DE (Data enable) mode
- 2 Channel LVDS (Low Voltage Differential Signaling) interface
- The interface (1pixel/clock) of LVDS serial interface)



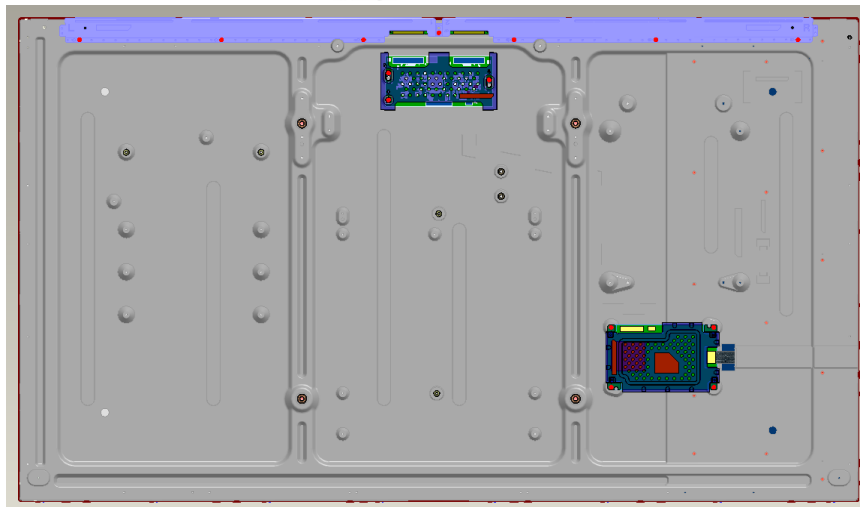
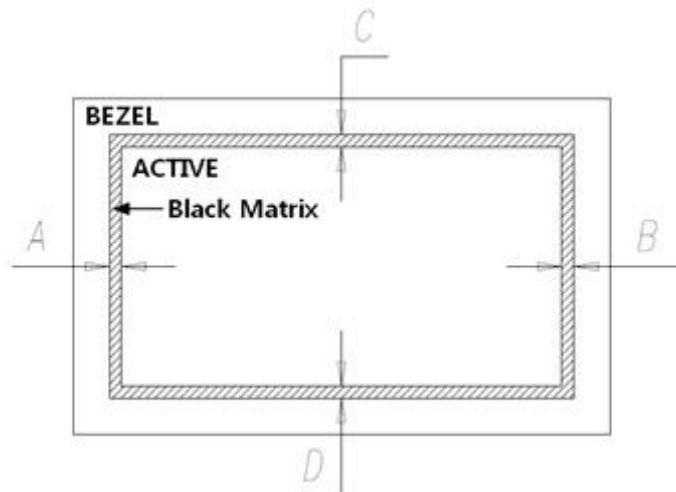
Items	Specification	Unit	Note
Active Display Area	1209.600(H) x 680.400(V)	mm	
Switching Components	a-Si TFT Active matrix		
Module Size	1229.4(H) x 704.2 (V)	mm	+1.0mm ~ -0.5mm
	31.7 (D)	mm	+3mm, -1mm
Weight	16700	g	$\pm 10\%$
Display Colors	16.7M (True Display) 1.07B (Dithered 10bit)	color	
Number of Pixels	1920 x 1080	pixel	16 : 9
Pixel Arrangement	RGB vertical stripe		
Display Mode	Normally Black		
Surface Treatment	AG POL		
Haze	Haze 2.3%		$\pm 2.1\%$
Hardness	Hard coating 2H		

MECHANICAL INFORMATION

Item		Min.	Typ.	Max.	Note
Module size	Horizontal(H)	1228.9	1229.4	1230.4	mm
	Vertical(V)	703.7	704.2	705.2	mm
	Depth(D)	30.7	31.7	34.7	mm ( With Converter )
Bezel Open	Horizontal(H)	1216.6	1217.6	1218.6	mm
	Vertical(V)	687.4	688.4	689.4	mm
Black Matrix Shift	Horizontal(H)	3.4	4.0	4.6	mm (1)
	Vertical(V)	3.5	4.0	4.5	
Weight			16700	18370	g

NOTE (1) Measure the figure for **Black Matrix shift** to be recorded on the spec. with referring to the drawings.

- $| A - B | \leq$  Horizontal Spec
- $| C - D | \leq$  Vertical Spec



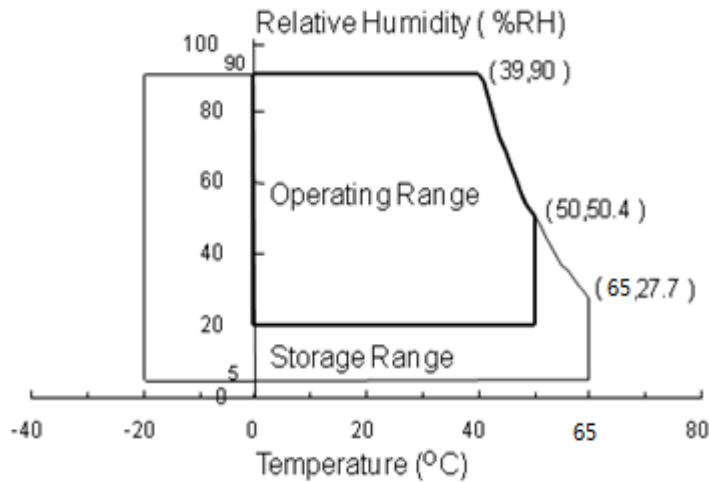
<Module Depth Measure Point>

# 1. ABSOLUTE MAXIMUM RATINGS

## 1.1 Environmental Absolute Ratings

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	65	°C	(1)
Operating temperate	TOPR	0	50	°C	(1)
Humidity for storage	HSTG	5	90	%RH	
Operating humidity	HOPR	20	90	%RG	
Endurance on static electricity			150	V	(2)
Shock (non-operating)	Snop(X,Y)		30	G	(3),(5)
	Snop(Z)	-	30		
Vibration (non-operating)	Vnop	-	1.5	G	(4),(5)

Note (1) The ranges of temperature and relative humidity are shown in the graph below. 90% RH Max.  
 (The temperature of Ta shall be over 39°C.)  
 The maximum temperature of wet-bulb shall be less than 39°C.  
 No condensation



Note (2) Keep the static electricity under 150V in Polarizer attaching process.

Note (3) 11ms, half sine wave, one time for ±X, ±Y, ±Z axis

Note (4) 10 ~ 300 Hz, Swap rate for X, Y, Z axis one time\*

Note (5) The fixture for the test of the vibration and shock, which holds the module to be tested shall be hard and rigid in order for the module not to be twisted or bent by the fixture.

## 1.2 Electrical Absolute Ratings

### (1) TFT LCD MODULE

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V <sub>DD</sub>	10.8		13.2	V	(1)
Dimming Control	V <sub>dim</sub>	0	-	3.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

The permanent damage or defect to the device may occur if the panel is operated at the figure set, which exceeds a limit of maximum value stated in the former spec.

The functional operation should be limited to the conditions described above under normal operating conditions.

### (2) BACK-LIGHT UNIT

Ta (25 ± 2 °C)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Supply Voltage / Converter	V <sub>cc</sub>	-	-	26	V	
LED Current(2D)	I <sub>LED,2D</sub>		-	147	mA <sub>mean</sub>	Continuous operation @String (1 String/PCB)
LED Current(3D)	I <sub>LED,3D</sub>		-	265	mA <sub>high</sub>	Duty 56%

## 1.3 The Others Absolute Ratings

### STATIC ELECTRICITY PRESSURE RESISTANCE

Item	Test Conditions	Remark
CONTACT DISCHARGE	150pF, 330Ω, ± 10kV, 210points, 1 time/point	Operating
AIR DISCHARGE	150pF, 330Ω, ± 20kV, 210points, 1 time/point	Operating

## 2. Optical characteristics

The optical characteristics shall be measured in the dark room or the space surrounded by the similar ambient setting.

Measuring equipment : TOPCON RD-80S, TOPCON SR-3, ELDIM EZ-Contrast

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast ratio (At the center of screen)		C/R		3000	4000	-		(1) SR-3
Response time	G-to-G	T <sub>g</sub>	T <sub>PAN,SUR</sub> =29.9°C	-	8	15	msec	(3) RD-80S
Luminance of white (At the center of screen)		Y <sub>L</sub>		320	360	-	cd/m <sup>2</sup>	(4) SR-3
Chromaticity (CIE 1931)	Red	R <sub>x</sub>	Normal q <sub>L</sub> ,R=0 q <sub>U</sub> ,D=0  Viewing Angle	TYP. -0.03	0.650	TYP. +0.03		(5),(6) SR-3
		R <sub>y</sub>			0.350			
	Green	G <sub>x</sub>			0.310			
		G <sub>y</sub>			0.600			
	Blue	B <sub>x</sub>			0.150			
		B <sub>y</sub>			0.060			
	White	W <sub>x</sub>			0.280			
		W <sub>y</sub>			0.290			
Color gamut		-		-	70	-	%	(5) SR-3
Color Temperature		-		7000	10000	13000	K	
Viewing Angle	Hor.	q <sub>L</sub>	C/R≥10:1	75	89	-	Degree	(6) SR-3 EZ-Contrast
		q <sub>R</sub>		75	89	-		
	Ver.	q <sub>U</sub>		75	89	-		
		q <sub>D</sub>		75	89	-		
Crosstalk		D <sub>SHA</sub>	101-255	-	-	5.0	%	(7) Over 40 gray (Max256)
			20-100			15.0		
			0 - 19			X		
Flicker		F		-	-	20		(8) RD-80S
				-	-	40		CA-210
Gamma		-		1.9	2.2	2.5		RD-80S (9)
Brightness uniformity (9 Points)		B <sub>uni</sub>		-	-	35	%	(2) SR-3 (1/6 Point)

\* Ta = 25 ± 2 °C, V<sub>DD</sub>=3.3V, f<sub>v</sub>= 60Hz, f<sub>DCLK</sub> = 69.3MHz, IF = 100% duty

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**Notice**

(a) Setup for test equipment

The measurement should be executed in a stable, windless, and dark room for 40min and 60min after operating the panel at the given temperature for stabilization of the standard light.  
 This measurement should be measured at the center of screen.  
 The environment condition:  $T_a = 25 \pm 2 \text{ }^\circ\text{C}$

Note (1) Definition of contrast ratio (C/R)

: The ratio of gray max (Gmax) & gray min (Gmin) at the center point ⑤ of the panel

$$C/R = \frac{G \text{ max}}{G \text{ min}}$$

Gmax : The luminance with all white pixels

Gmin : The luminance with all black pixels

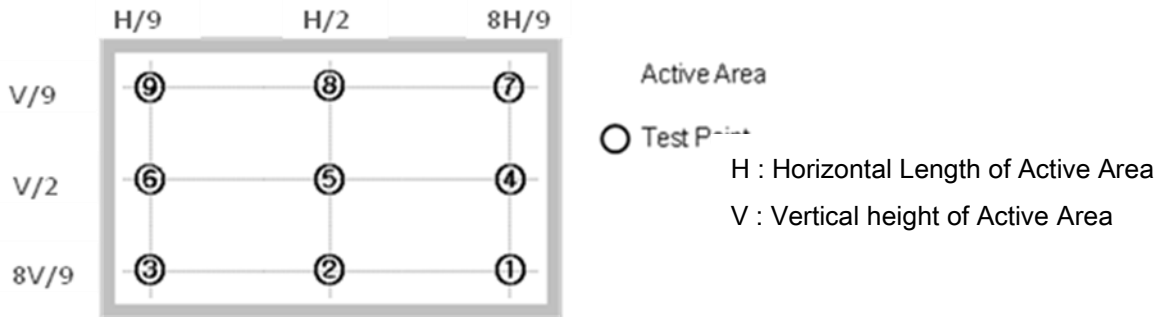
Note (2) Definition of the brightness uniformity of 9 points (Test pattern : The full white)

$$Buni = 100 * \frac{(B \text{ max} - B \text{ min})}{B \text{ max}}$$

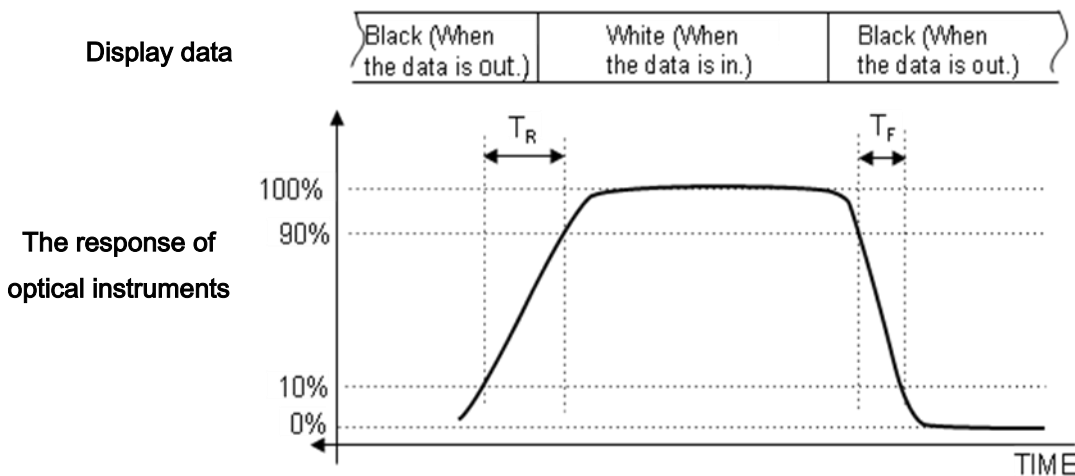
Bmax : The maximum brightness

Bmin : The minimum brightness

- Definition of test point



Note (3) Definition of response time : Sum of  $T_r$ ,  $T_f$



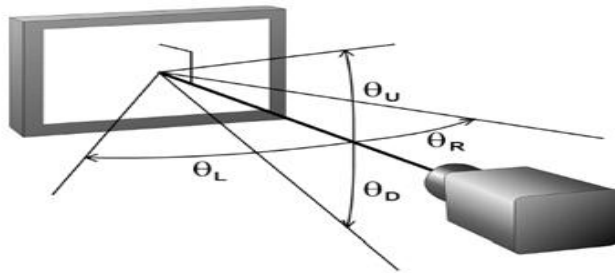
※ G-to-G: Average response time between the whole gray scale to the whole gray scale.



Note (4) The definition of luminance of white: The luminance of white at the center point ⑤

Note (5) The definition of chromaticity (CIE 1931)

The color coordinate of red, green, blue and white at the center point ⑤



Note (6) Definition of viewing angle: The range of viewing angle (C/R ≥ 10)

Note (7) The definition of crosstalk; (Cross modulation) (DSHA): The phenomenon, which the level of contrast ratio is declined by the interference of signals in pixels.

$$\text{Crosstalk Modulation Ratio}(D_{SHA}) = \frac{|Y_{normal} - Y_{abnormal}|}{Y_{normal}} \times 100(\%)$$

\* Measure the size of background pattern at the interval of 4 grays with excluding the size of white rectangle within the range from gray 1 to gray 64.

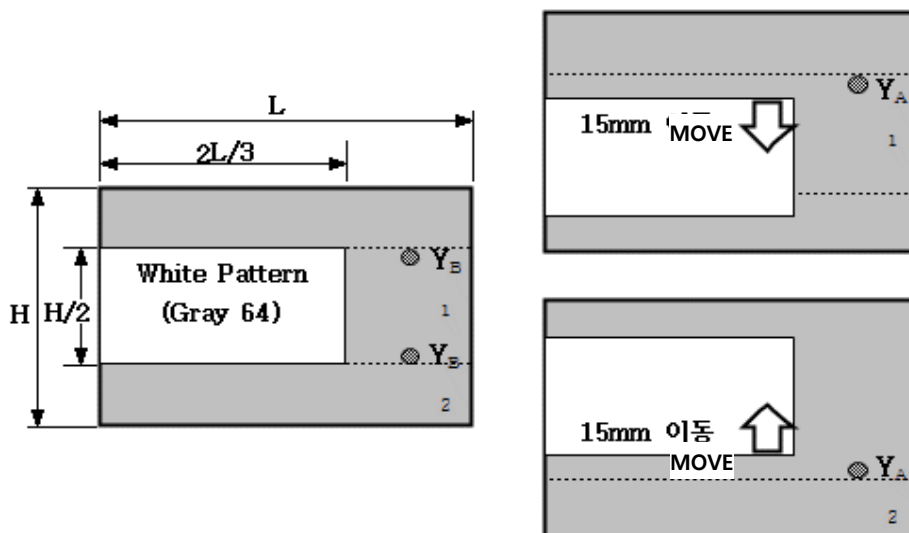
\* Measure the horizontal crosstalk and vertical crosstalk both.

\* The maximum value among measured values can be defined as a crosstalk.

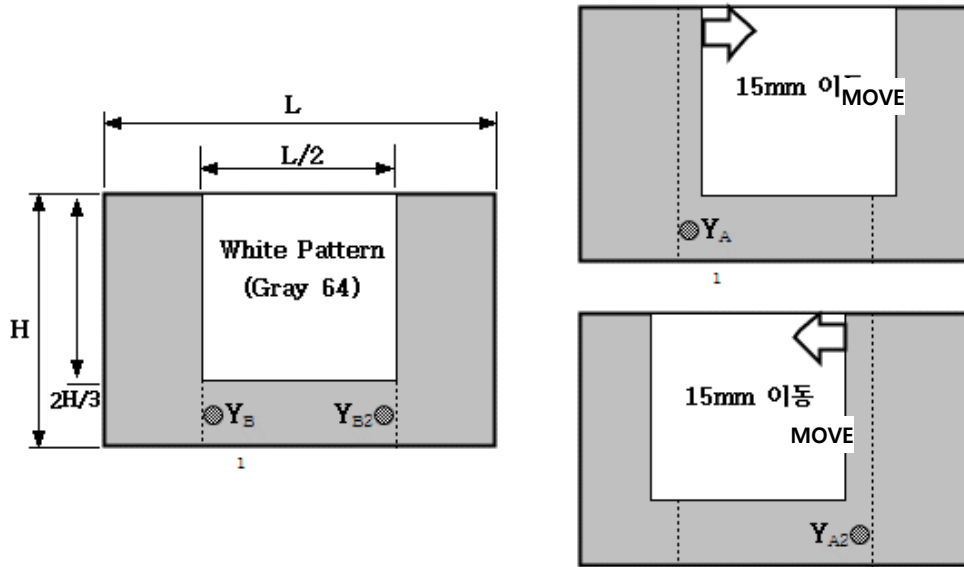
Reference: The color of rectangle for Gmin is black when the color of screen is white.

The color of rectangle for Gmax is white when the color of screen is black.

\* Pattern to measure the crosstalk and points to be measured



< Horizontal Crosstalk >



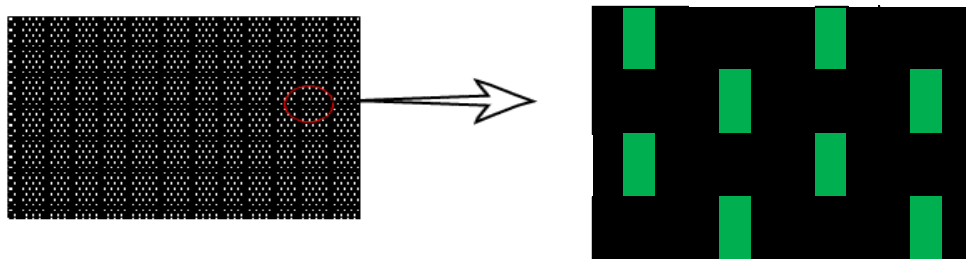
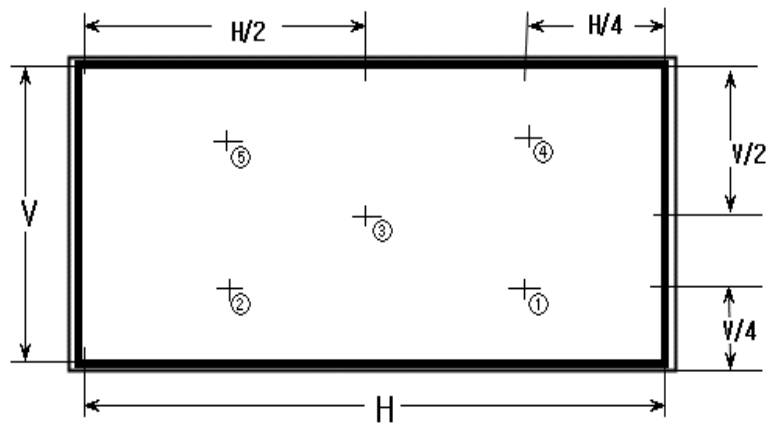
< Vertical Crosstalk >

Note (8)

The definition of terminology, flicker: The phenomenon, which the pixels on the screen of LCD panel blink.

- 1) Calculate the value of crosstalk with observing the standard for measuring the flicker.
- 2) The points to be measured

- The pattern to measure the flicker



< Green checker Inversion >

Note (9) Definition of Gamma

$$\text{Gamma} = \log(X_{lum} / 100) / \log(Y / 100)$$

$$X_{lum} = (Z - B_{min}) / (B_{max} - B_{min}) \times 100$$

Y: Measurement Level / Z: Measurement Brightness

B<sub>max</sub>: Maximum Brightness / B<sub>min</sub>: Minimum Brightness

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### 3. Electrical characteristics

#### 3.1 TFT\_LCD Module

The connector to transmit a display data and a timing signal shall be connected.

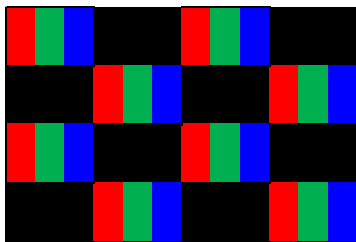
Ta = 25°C ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply	V <sub>DD</sub>	10.8	12.0	13.2	V	(1)
Current of Power Supply	(a) Black	-	510	-	mA	(2),(3)
	(b) White	-	490	-	mA	
	(c) N-PTN	-	670	-	mA	
Vsync Frequency	f <sub>V</sub>	48	60	62.5	Hz	
Hsync Frequency	f <sub>H</sub>	60	67.5	70	kHz	
Main Frequency	f <sub>DCLK</sub>	130	148.5	152.5	MHz	
Rush Current	I <sub>RUSH</sub>	-	-	4	A	(4)

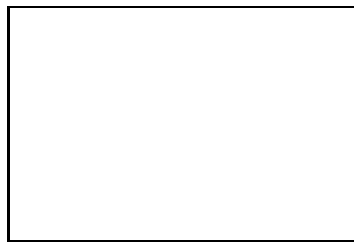
Note (1) The voltage for ripple shall be controlled under the range of fewer than 10% of V<sub>DD</sub> voltage.

(2) f<sub>V</sub>=60Hz, f<sub>DCLK</sub> =148.5MHz, V<sub>DD</sub> = 12.0V, DC Current.

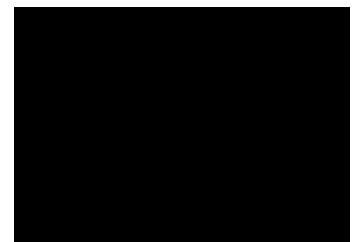
(3) The pattern for checking the power dissipation (LCD module only)



(a) checker pattern

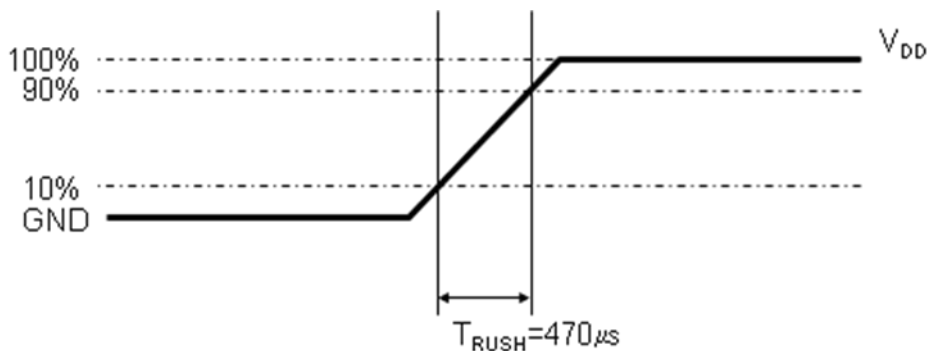


b) White pattern



c) Black Pattern

(4) Conditions for measurement

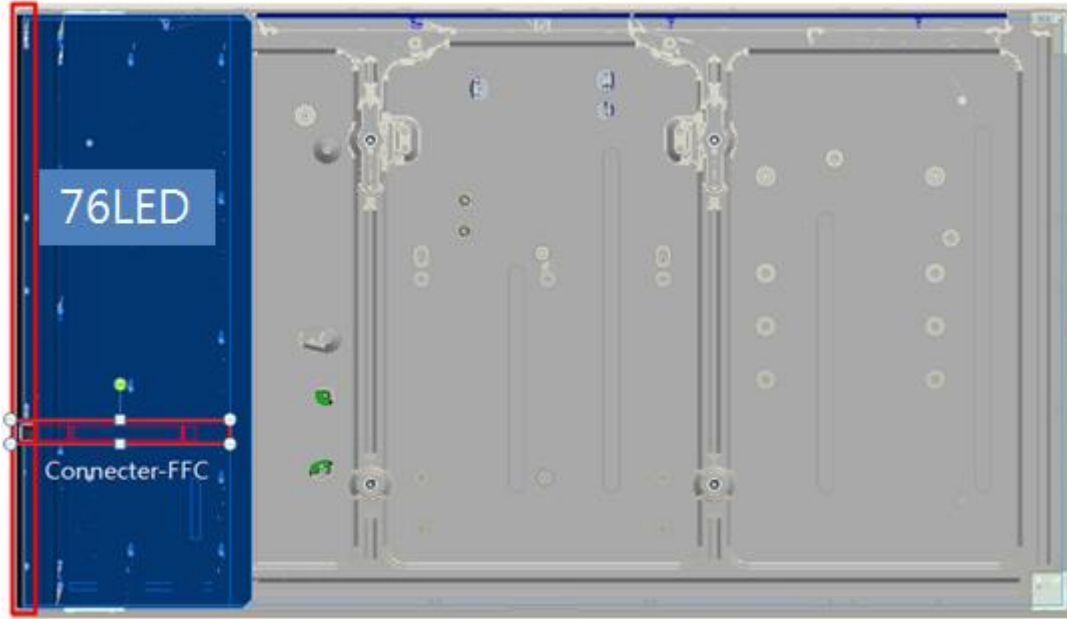


The rush current, I<sub>RUSH</sub> can be measured when T<sub>RUSH</sub> is 470µs.

\* The temperature range for component of the some major part of operating module

**3.2 BACK-LIGHT UNIT**

\* Back light unit is composed of 1-LED bars. (76 PCS of LEDs).



Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Temperature range	Top	-20	-	70	°C	
Storage Temperature range	Tstg	-30	-	85	°C	
Junction Temperature	Tj	-	-	145	°C	
LED Forward Current	IF	133	140	147	mA	Continuous operation @String (4 String/PCB) Operating Current 140mA
	IFP	-	-	252	mA	120Hz/Duty56%
LED Forward Voltage	VF	108.5	115.5	123.2	V	@140mA/string@ Tj 25°C
	VFP	-	-	130	V	120Hz/Duty56%
Thermal Resistance Junction to PCB	Rth, JS	-	-	25	K/W	
Power Consumption	P	60.7	64.7	69.0	W	IF X VF
Operating Life Time	Hr	30000	-	-	Hour	MTTF, 2D Only
LED Counts	Q	-	76	-	EA	

**3.3 The Condition & Specification of Converter Input (Ta = 25°C ± 2 °C)**

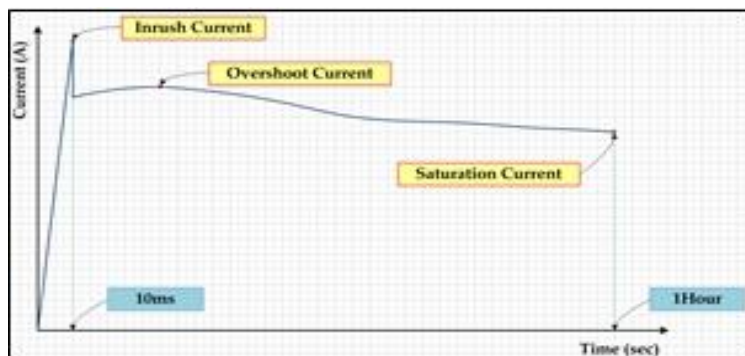
ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE	
Input Voltage	V <sub>IN</sub>		22	24	26	V		
Inrush Current Note(2)(3)	I <sub>INRUSH,N</sub>	V <sub>IN</sub> = 24V, Dim=Max 3D ENA=Off	-	-	3.57	A	Normal Mode	
	I <sub>INRUSH,3D</sub>	V <sub>IN</sub> = 24V, 3D ENA = On	-	-	8.20	A	3D Mode	
Output Current Note(1)	I <sub>LED,N</sub>	V <sub>IN</sub> = 24V, Dim=Max 3D ENA=Off	133	140	147	mA <sub>mean</sub>	Normal Mode @1 String	
	I <sub>LED,3D</sub>	V <sub>IN</sub> = 24V, 3D ENA = On	239	252	265	mAdc Note(5)	3D Mode Active High @1String	
Converter On/Off Control	ENA	Enable	2.4	-	5.25	V		
		Disable	-0.3	-	0.4			
INT_DIM	V <sub>INT_DIM</sub>	V <sub>IN</sub> = 24V	0	-	3.3	V	Note(*4)(*5) V <sub>EXT_DIM</sub> Pin(#14) : floating(N.C)	
	D <sub>INT_DIM</sub> (Duty)	V <sub>IN</sub> = 24V	1	-	100	%		
EXT_DIM	V <sub>EXT_DIM</sub>	High Level	2.4	-	5.25	V	Note(4)(5)(6) V <sub>INT_DIM</sub> pin(#13) = floating(N.C.)	
		Low Level	-0.3	-	0.4			
	D <sub>EXT_DIM</sub> (Duty)		1	-	100	%		
	F <sub>EXT_DIM</sub>	V <sub>IN</sub> = 24V	-	150	-	Hz Note(7)		
	T <sub>RISING</sub>		-	-	200	ns		
	T <sub>FALLING</sub>		-	-	200	ns		
V <sub>SYNC</sub>	V <sub>SYNC</sub>	High Level	2.4	-	3.6	V	Note(*5)(*6) INT_DIM Only	
		Low Level	-0.3	-	0.4			
	D <sub>SYNC</sub>		-	50	-	%		
	F <sub>SYNC</sub>	V <sub>IN</sub> = 24V		120	125	130		Hz V <sub>sync</sub> 50
				143	150	156		Hz V <sub>sync</sub> 60
	T <sub>RISING</sub>		-	-	200	ns		
T <sub>FALLING</sub>		-	-	200	ns			
3D Mode	3D ENA	Enable	2.4	-	3.6	V	Note(*5)(*6)	
		Disable	-0.3	-	0.4			
	3D PWM	V <sub>IN</sub> = 24V	High Level	2.4	-	3.6		V
			Low Level	-0.3	-	0.4		
	D <sub>3D_PWM</sub>	V <sub>IN</sub> = 24V		56		%		
	F <sub>3D_PWM</sub>	3D ENA = On		120		Hz		

Note (1) All data was approved after running 120 minutes.

Note (2) Inrush is measured within BLU on 10ms after leaving the BLU as it is at least 1hr or more at room temperature(25°C)

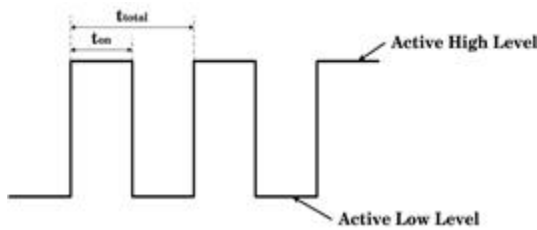
Note (3) Additional Appendix for Input current at room temperature(25°C)

ITEM	SYMBOL	CONDITION	SPECIFICATION			UNIT	NOTE
			MIN	TYP	MAX		
Input Current (Normal Mode)	I overshoot, N	Vin=24V, Dim=Max	-	3.09	3.18	A mean	Overshoot Current After Turn-on
	I saturation, N		-	3.06	3.15	A mean	Saturation current after 1hr aging
Input Current (3D Mode)	I overshoot, 3D	Vin=24V 3D PWM=56%	-	3.36	3.46	A mean	Overshoot Current After Turn-on
	I saturation, 3D		-	3.33	3.43	A mean	Saturation current after 1hr aging
	I overshoot, 3D		-	-	7.46	A max	Overshoot Current After Turn-on

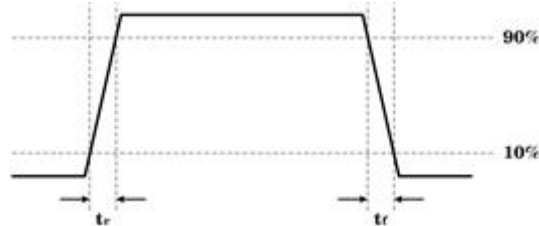


Note (4) Internal PWM mode and External PWM mode are not available at the same time. In other word, if one of the dimming control signal was input (connected), the other dimming control signal must be floating (No Connection)

Note (5) duty=ton/ttotal



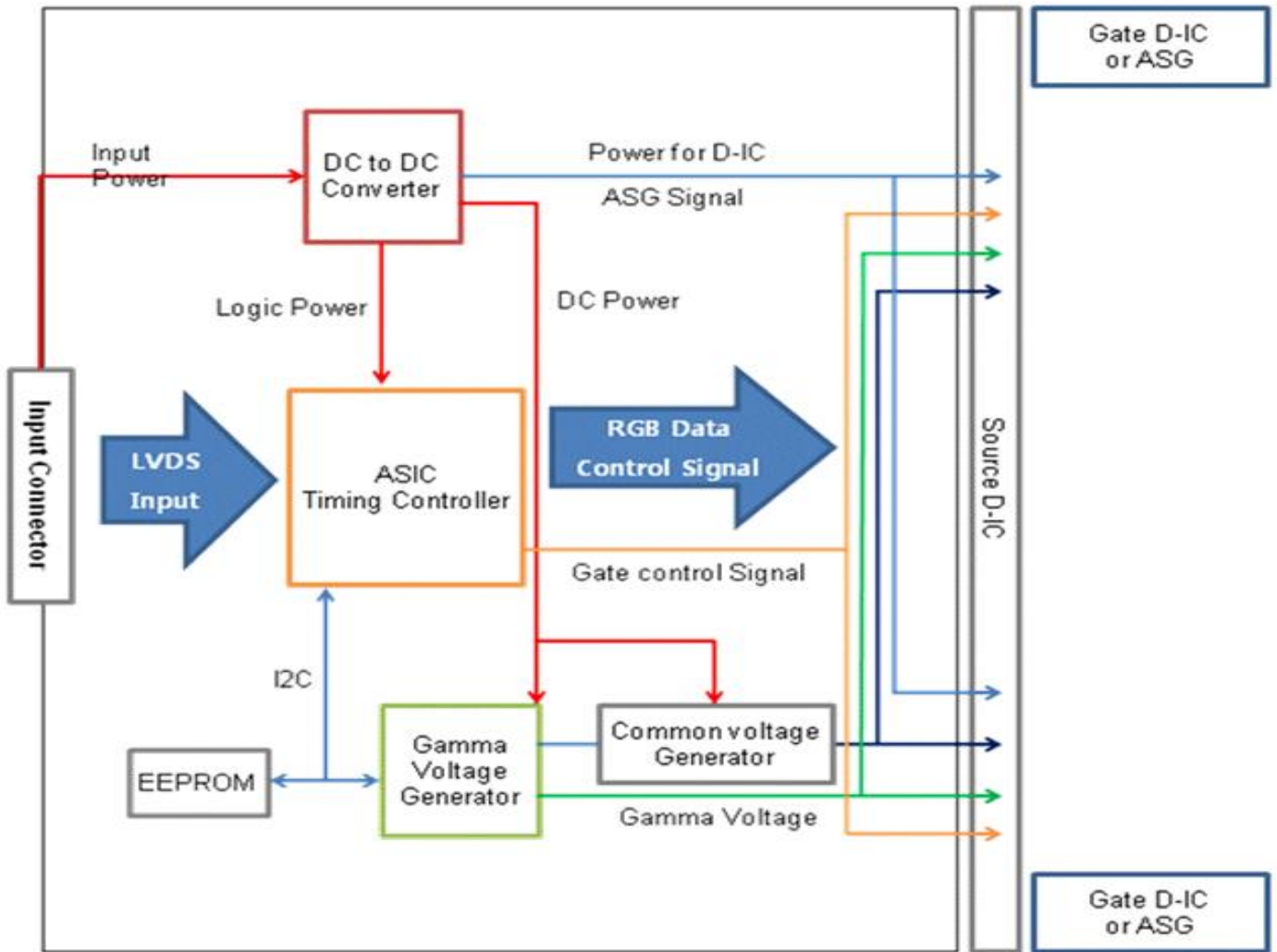
Note(6) Signal rising/falling time



Note (7) Use an external frequency which doesn't make a waterfall and a sound noise within this range.

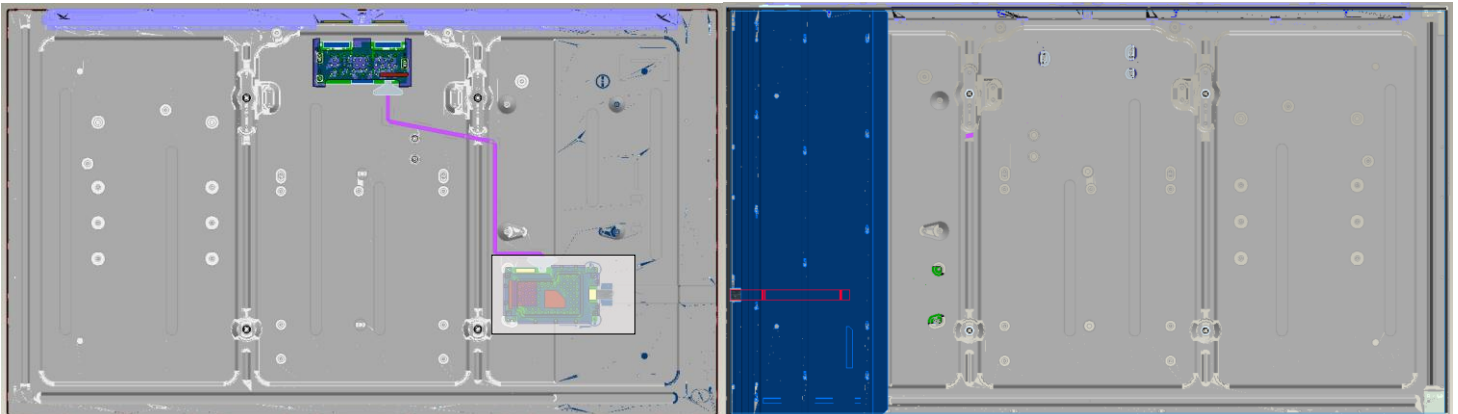
## 4. Block diagram

### 4.1 TFT LCD MODULE



### 4.2 Back Light

HOT : Built in converter



## 5. The Pin assignment in the input terminal

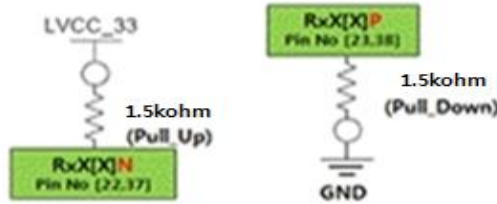
### 5.1 Input Signal & Power (Connector : IS100-L300-C23 (UJU, In-PCB Type))

Pin	Description	Pin	Description
1	Bus release	26	3D_EN signal
2	I2C SCL	27	Not Connect
3	I2C SDA	28	2nd, LVDS Signal - ( RX2[0]N )
4	3D_FORMAT0	29	2nd, LVDS Signal + ( RX2[0]P )
5	ShutterGlass sync output signal / 3D Sync_0	30	2nd, LVDS Signal - ( RX2[1]N )
6	3D_FORMAT1	31	2nd, LVDS Signal + ( RX2[1]P )
7	Not Connect/ LVDS_SEL	32	2nd, LVDS Signal - ( RX2[2]N )
8	Not Connect/TEMP_SEL0	33	2nd, LVDS Signal + ( RX2[2]P )
9	Not Connect /TEMP_SEL1	34	Ground
10	Not Connect	35	2nd, LVDS Clock - ( RX2CLKN )
11	Ground	36	2nd, LVDS Clock + ( RX2CLKP )
12	1st, LVDS Signal - ( RX1[0]N )	37	Ground
13	1st, LVDS Signal + ( RX1[0]P )	38	2nd, LVDS Signal - ( RX2[3]N )
14	1st, LVDS Signal - ( RX1[1]N )	39	2nd, LVDS Signal + ( RX2[3]P )
15	1st, LVDS Signal + ( RX1[1]P )	40	2nd, LVDS Signal - ( RX2[4]N ) *note (1)
16	1st, LVDS Signal - ( RX1[2]N )	41	2nd, LVDS Signal + ( RX2[4]P ) *note (1)
17	1st, LVDS Signal + ( RX1[2]P )	42	Not Connect
18	Ground	43	Not Connect
19	1st, LVDS Clock - ( RX1CLKN )	44	Ground
20	1st, LVDS Clock + ( RX1CLKP )	45	Ground
21	Ground	46	Ground
22	1st, LVDS Signal - ( RX1[3]N )	47	Not Connect
23	1st, LVDS Signal + ( RX1[3]P )	48	DC power supply
24	1st, LVDS Signal - ( RX1[4]N ) *note (1)	49	DC power supply
25	1st, LVDS Signal + ( RX1[4]P ) *note (1)	50	DC power supply
		51	DC power supply



Note(1) :

- Input Mode 8Bit Setting & 8bit input 시, ==> E\_Channel : Floating
- Input Mode 10bit Setting & 8bit input 시, ==> E\_Channel : Keep Level '0'
- PIN No.24 / Pin No.40 : Pull Up(3.3V) with 1.5k ohm resist
- PIN No. 25/Pin No. 41: Pull Down(GND) with 1.5k ohm resist
- \* Level of LVDS signals are base on LVDS CHARACTERISTICS(7-12)



Not Connected : This PINS are only used for SDC internal Operations

**Bus release, I2C SCL and I2C SDA shouldn't be communicated with I2C device whose output level is 5V.**

Sequence: On = Vdd (T1) ≥ LVDS Option ≥ Interface Signal (T2) / Off = interface Signal (T3) ≥ LVDS Option ≥ Vdd

Note (1) Pin number, which starts from the left side.

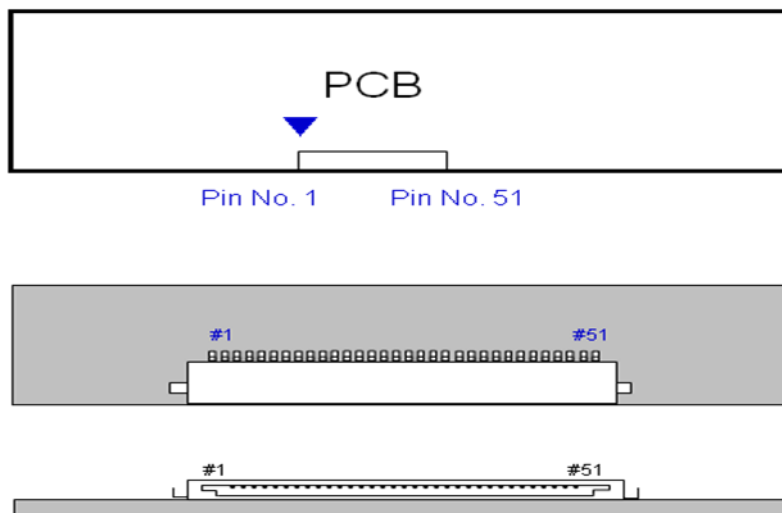


Fig . The diagram of connector

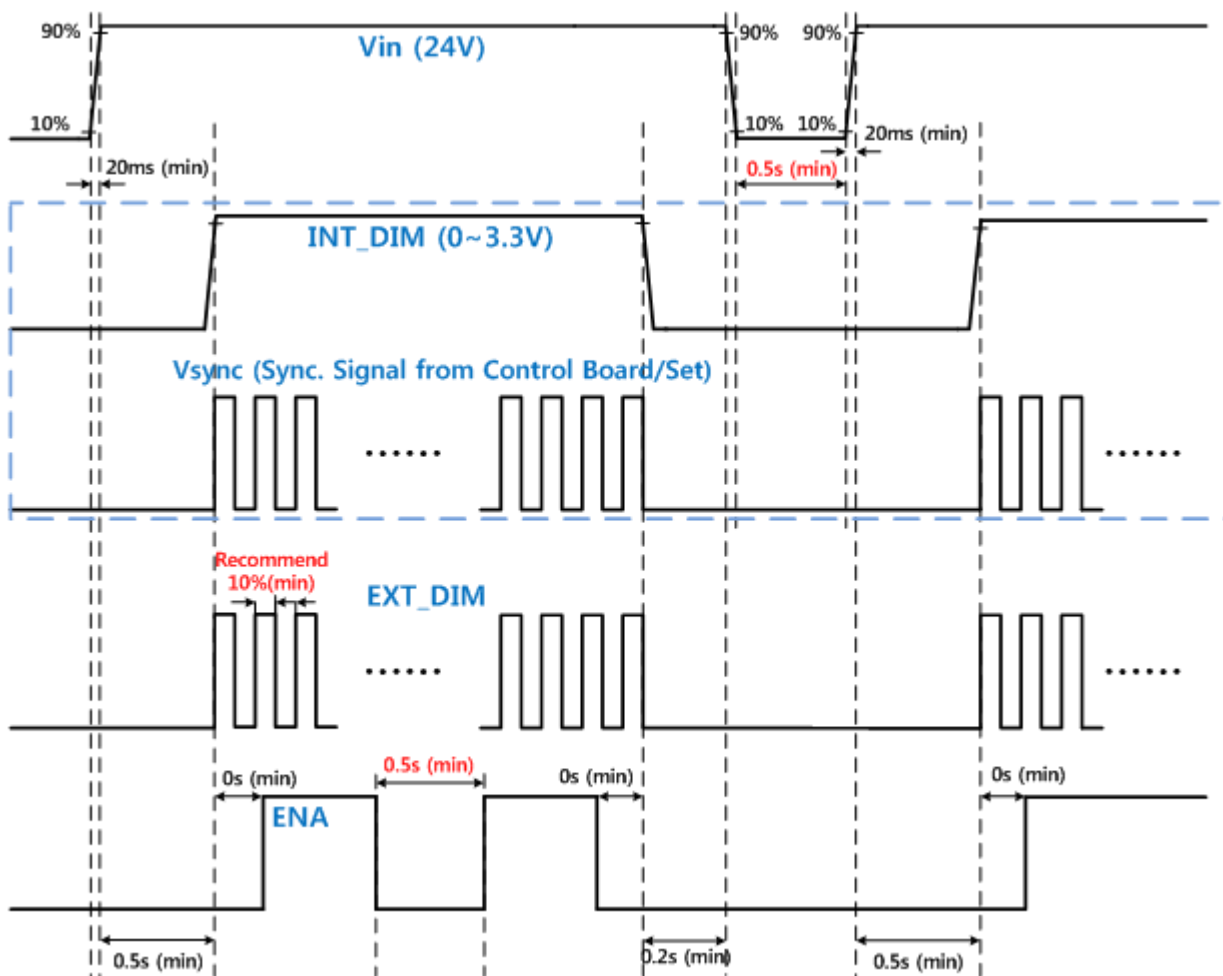
- a. Pins for power GND shall be connected to the LCD's metal chassis.
- b. All input pins for power shall be connected together.
- c. All NC pins shall be designed with being separated from other signal or power.

### 5.2 Configuration of Input pin of Converter

Input Connector Model No. : 22022WR-H14B2 (YEONHO) or Equivalent Connector

PIN NO	SYMBOL	REMARK
1,2,3,4,5	Vin	Power Supply DC 24V
6,7,8,9,10	GND	Ground
11	NC	No Connection
12	ENA	Converter On/Off Control Signal
13	INT_DIM	Internal Dimming Control Signal No Connection (In case of using EXT_DIM #14)
14	EXT_DIM	External Dimming Control Signal No Connection (In case of using INT_DIM #13)

### 5.3 The power sequence for inputting the Converter



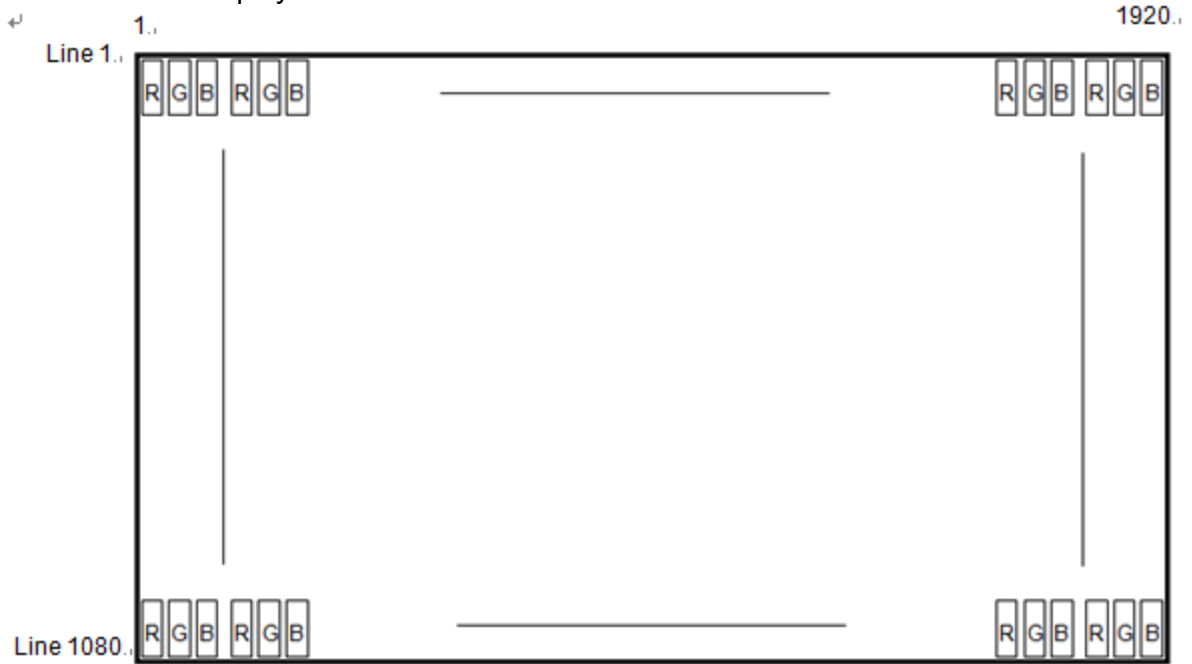
INT\_DIM mode and EXT\_DIM mode are not available at same time. In other word, if one of the dimming control signal was input (connected) the other dimming control signal must be floating. (No Connection)

**5.4 LVDS Interface ( LVDS Receiver : T-CON (merged) , Data Format(JEIDA Only )**

	LVDS pin	JEIDA -DATA
TxOUT/RxIN0	TxIN/RxOUT0	R4
	TxIN/RxOUT1	R5
	TxIN/RxOUT2	R6
	TxIN/RxOUT3	R7
	TxIN/RxOUT4	R8
	TxIN/RxOUT6	R9
	TxIN/RxOUT7	G4
TxOUT/RxIN1	TxIN/RxOUT8	G5
	TxIN/RxOUT9	G6
	TxIN/RxOUT12	G7
	TxIN/RxOUT13	G8
	TxIN/RxOUT14	G9
	TxIN/RxOUT15	B4
	TxIN/RxOUT18	B5
TxOUT/RxIN2	TxIN/RxOUT19	B6
	TxIN/RxOUT20	B7
	TxIN/RxOUT21	B8
	TxIN/RxOUT22	B9
	TxIN/RxOUT24	HSYNC
	TxIN/RxOUT25	VSYNC
	TxIN/RxOUT26	DEN
TxOUT/RxIN3	TxIN/RxOUT27	R2
	TxIN/RxOUT5	R3
	TxIN/RxOUT10	G2
	TxIN/RxOUT11	G3
	TxIN/RxOUT16	B2
	TxIN/RxOUT17	B3
	TxIN/RxOUT23	RESERVED
TxOUT/RxIN4	TxIN/RxOUT28	R0
	TxIN/RxOUT29	R1
	TxIN/RxOUT30	G0
	TxIN/RxOUT31	G1
	TxIN/RxOUT32	B0
	TxIN/RxOUT33	B1
	TxIN/RxOUT34	RESERVED



5.6 Pixel Format in the display



## 6. Interface timing

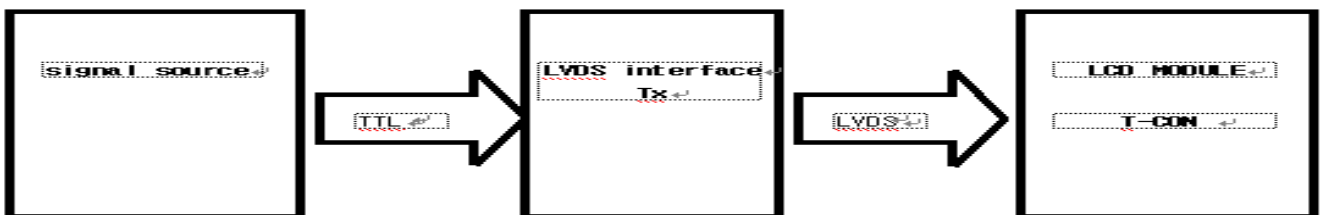
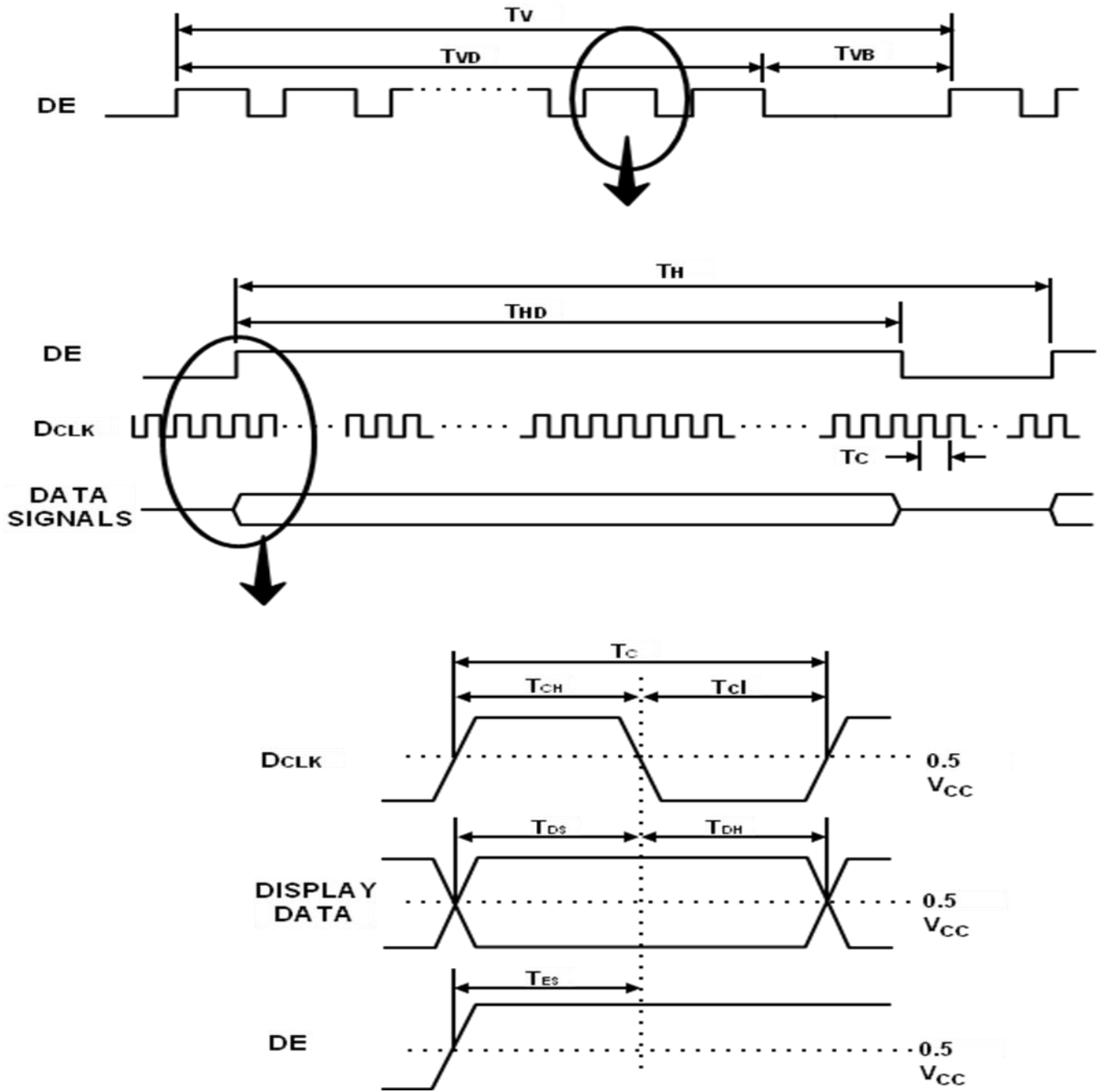
### 6.1 The parameters of timing ( DE mode )

SIGNAL	ITEM	SMBOL	MIN.	TYP.	MAX.	Unit	NOTE
Clock	Frequency	$1/T_C$	130	148.5	152.5	MHz	-
Hsync		$F_H$	60	67.5	70	KHz	-
Vsync		$F_V$	48	60	62.5	Hz	-
Term for the vertical display	Active display period	$T_{VD}$	-	1080	-	Lines	-
	Total vertical	$T_{VB}$	1110	1125	1400	Lines	-
Term for the horizontal display	Active display period	$T_{HD}$	-	1920	-	Clocks	-
	Total Horizontal	$T_H$	2092	2200	2348	clocks	-

Note) The signals of Hsync and Vsync must be inputted even though this T-con is operated at DE mode.

- (1) Test Point: TTL controls signal and CLK at LVDS Tx at the input terminal of system.
- (2) Internal VDD = 3.3V
- (3) The spread spectrum
  - The limit of spread spectrum's range of SET in which the LCD module is assembled should be within  $\pm 3\%$ .
  - Modulation frequency : max 300 kHz

6.2 Timing diagrams of interface signal (Only DE mode)

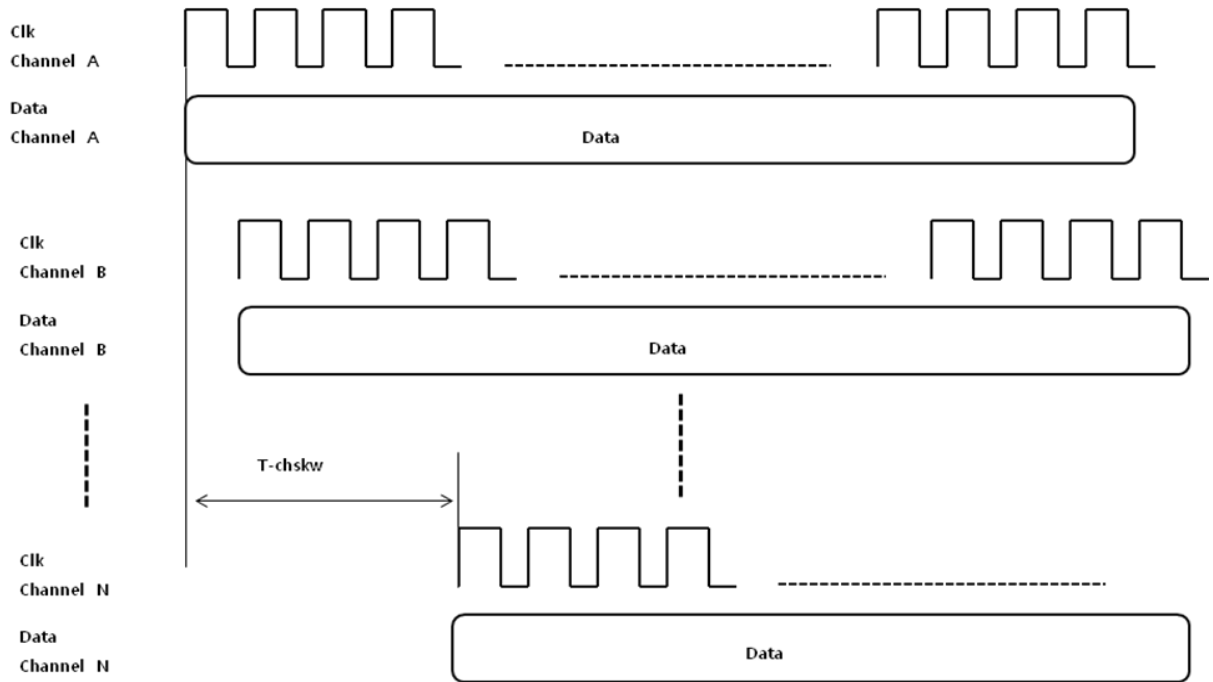


- LVDS Transmitter: DS90C385MTD (N/S) / THC63LVDM83A(THINE) : Recommend

LVDS Normal Interface Data Format

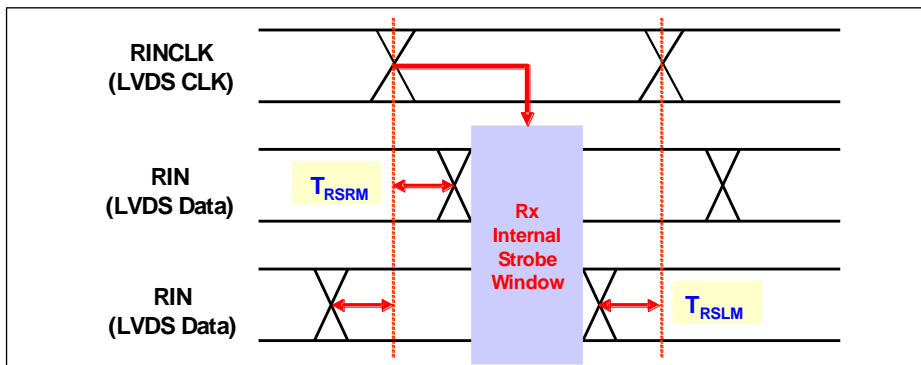
MODEL	LTA550HQ23-W	Doc. No		Page	23 / 39
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LVDS Channel to Channel Skew (T-chskw) in Multiple LVDS Channels



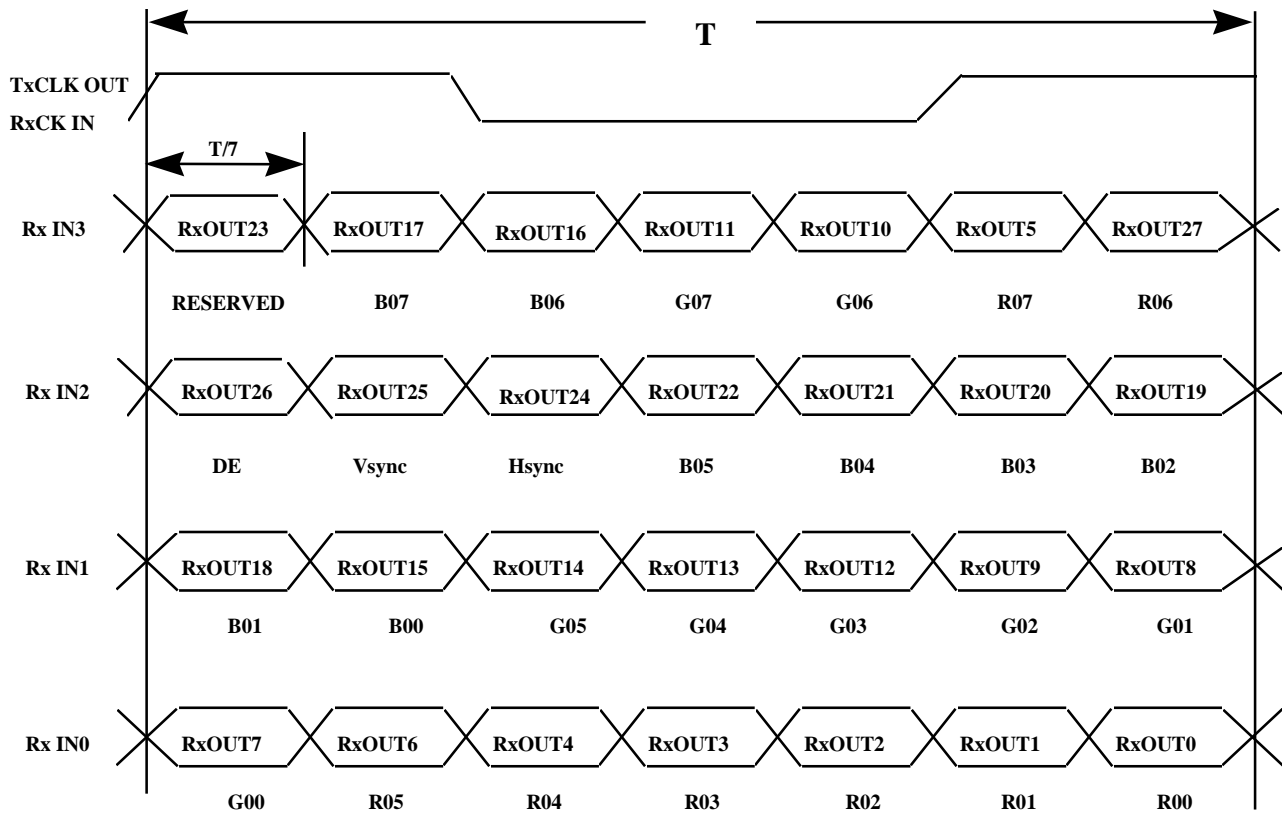
Note: DE should be synchronized with DE per each LVDS Channel and  $T\text{-chskw} < 16 * \text{LVDS Clock Period}$

LVDS Clock to Data Skew ( $T_{\text{RSRM}}$  &  $T_{\text{RSLM}}$ ) at each LVDS Channel



Symbol	Characteristics		Min.	Typ.	Max.	Unit
$T_{\text{RSRM}}$	Input Data Position	LVDS CLK = 85MHz			400	ps
		LVDS CLK = 78MHz			450	ps
		LVDS CLK = 75MHz			500	ps
$T_{\text{RSLM}}$	Input Data Position	LVDS CLK = 85MHz	400			ps
		LVDS CLK = 78MHz	450			ps
		LVDS CLK = 75MHz	500			ps




**RECOMMENDED TRANSMITTER INPUT CHARACTERISTICS**

SYMBOL	PARAMETER	MIN.	TPY.	MAX.	UNITS.
TCIT	TxCLK IN TRANSITION TIME (FIG2)	1.0	-	6.0	ns
TCIP	TxCLK IN PERIOD (FIG3)	11.76	T	50	ns
TCIH	TxCLK IN HIGH TIME (FIG3)	0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN LOW TIME (FIG3)	0.35T	0.5T	0.65T	ns
TXIT	TxCLK TRANSITION TIME	1.5	-	6.0	ns

**TRANSMITTER SWITCHING CHARACTERISTICS**

-OVER RECOMMENDED OPERATING SUPPLY AND TEMPERATURE RANGES UNLESS OTHERWISE SPECIFIED.

SYMBOL	PARAMETER	MIN.	TPY.	MAX.	UNITS.		
LLHT	LVDS LOW TO HIGH TRANSITION TIME (FIG1)	-	0.75	1.5	ns		
LHLT	LVDS HIGH TO LOW TRANSITION TIME (FIG1)	-	0.75	1.5	ns		
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	-0.25	0	0.25	ns		
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1	3.32	3.57	3.82	ns		
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2	6.89	7.14	7.39	ns		
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3	10.46	10.71	10.96	ns		
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4	14.04	14.29	14.54	ns		
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5	17.61	17.86	18.11	ns		
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6	21.18	21.43	21.68	ns		
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	-0.20	0	0.20	ns		
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1	2.00	2.20	2.40	ns		
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2	4.20	4.40	4.60	ns		
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3	6.39	6.59	6.79	ns		
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4	8.59	8.79	8.99	ns		
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5	10.79	10.99	11.19	ns		
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6	12.99	13.19	13.39	ns		
TPPos0	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 0 (FIG 7) NOTE 1	-0.20	0	0.20	ns		
TPPos1	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 1	1.48	1.68	1.88	ns		
TPPos2	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 2	3.16	3.36	3.56	ns		
TPPos3	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 3	4.84	5.04	5.24	ns		
TPPos4	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 4	6.52	6.72	6.92	ns		
TPPos5	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 5	8.20	8.40	8.60	ns		
TPPos6	TRANSMITTER OUTPUT PULSE POSITION FOR BIT 6	9.88	10.08	10.28	ns		
TSTC	TxIN SETUP TO TxCLK IN (FIG 3)	2.5	-	-	ns		
THTC	TxIN HOLD TO TxCLK IN (FIG 3)	0	-	-	ns		
TCCD	TxCLK IN TO TxCLK OUT DELAY (FIG4)	Ta = 25 °C, Vcc = 3.3 V		3.8	-	6.3	ns
	TxCLK IN TO TxCLK OUT DELAY (FIG4)	2.8	-	7.1		ns	
TJCC	TRANSMITTER JITTER CYCLE TO CYCLE (FIG 8,9)	F=85 MHZ	-	110	150	ps	
		F=65 MHZ	-	210	230	ps	
		F=40 MHZ	-	350	370	ps	
TPLLS	TRANSMITTER PHASE LOCK LOOP SET (FIG 5)	-	-	10		ms	
TPDD	TRANSMITTER POWER DOWN DELAY (FIG 6)	-	-	100		ns	

Note1) the minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges. This parameter is functionality tested only on automatic test equipment (ATE)

Note2) the limits are based on bench characterization of the device's jitter response over the power supply voltage range. output clock jitter is measured with a cycle to cycle jitter of  $\pm 3\text{ns}$  applied to the input clock signal while data inputs are switching (fig8,9).A jitter event of 3 ns, represents worse case jump in the clock edge from most graphics controller VGA Chips currently available. This parameter is used when calculating system margin as described in AN-1059

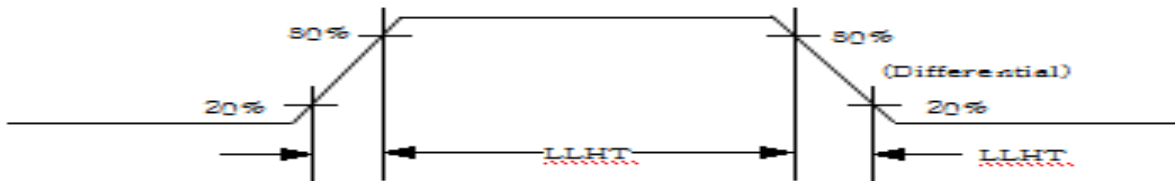


FIGURE 1. Transmitter LVDS Transition Times

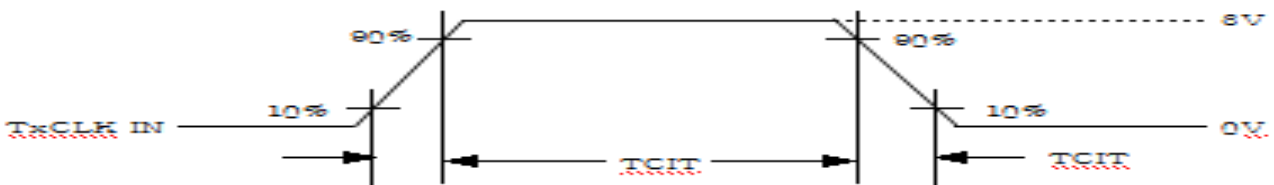


FIGURE 2. Transmitter Input Clock Transition Times

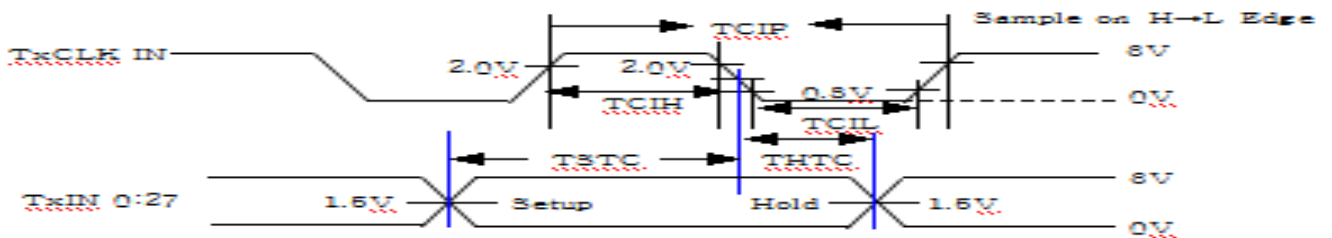


FIGURE 3. Transmitter Setup/Hold and High/Low Times (Falling Edge Strobe)

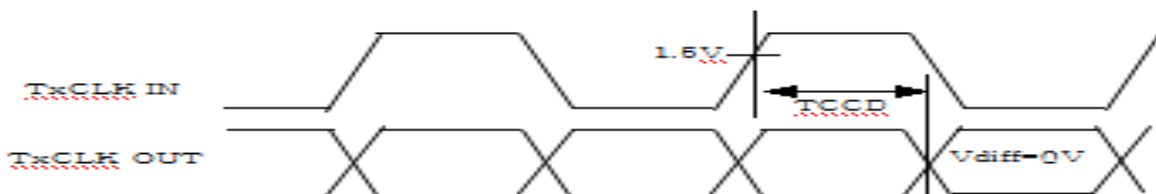


FIGURE 4. Transmitter Clock In to Clock Out Delay

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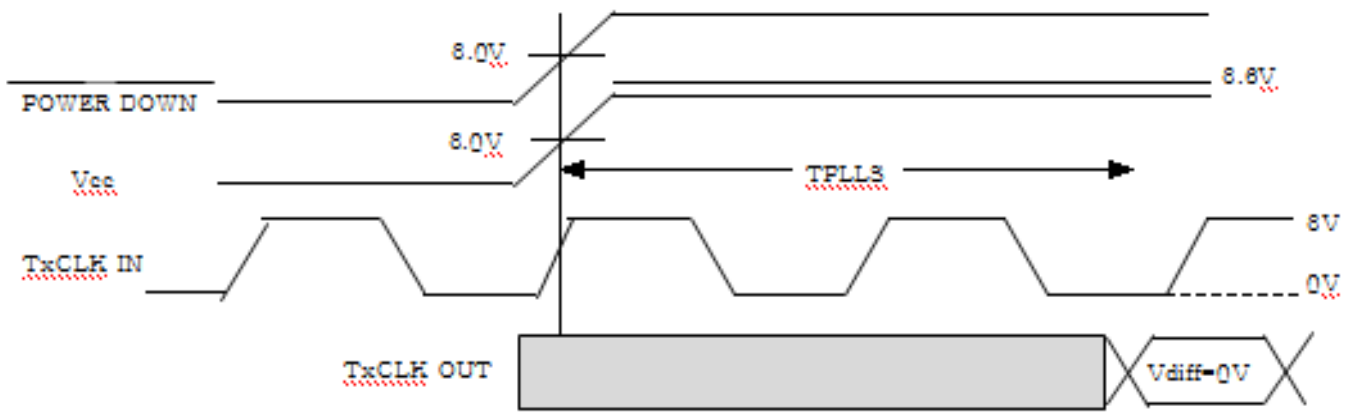


FIGURE 5, Transmitter Phase lock loop(PLL) SET-UP TIME

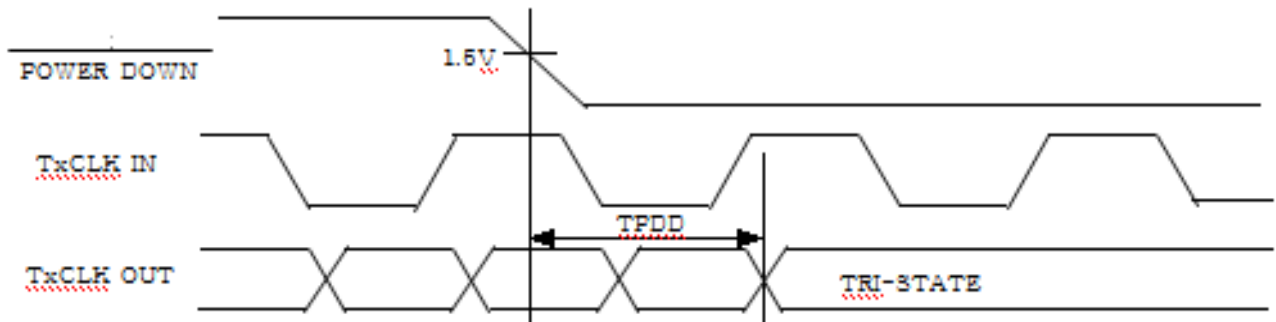


FIGURE 6, Transmitter Power down delay

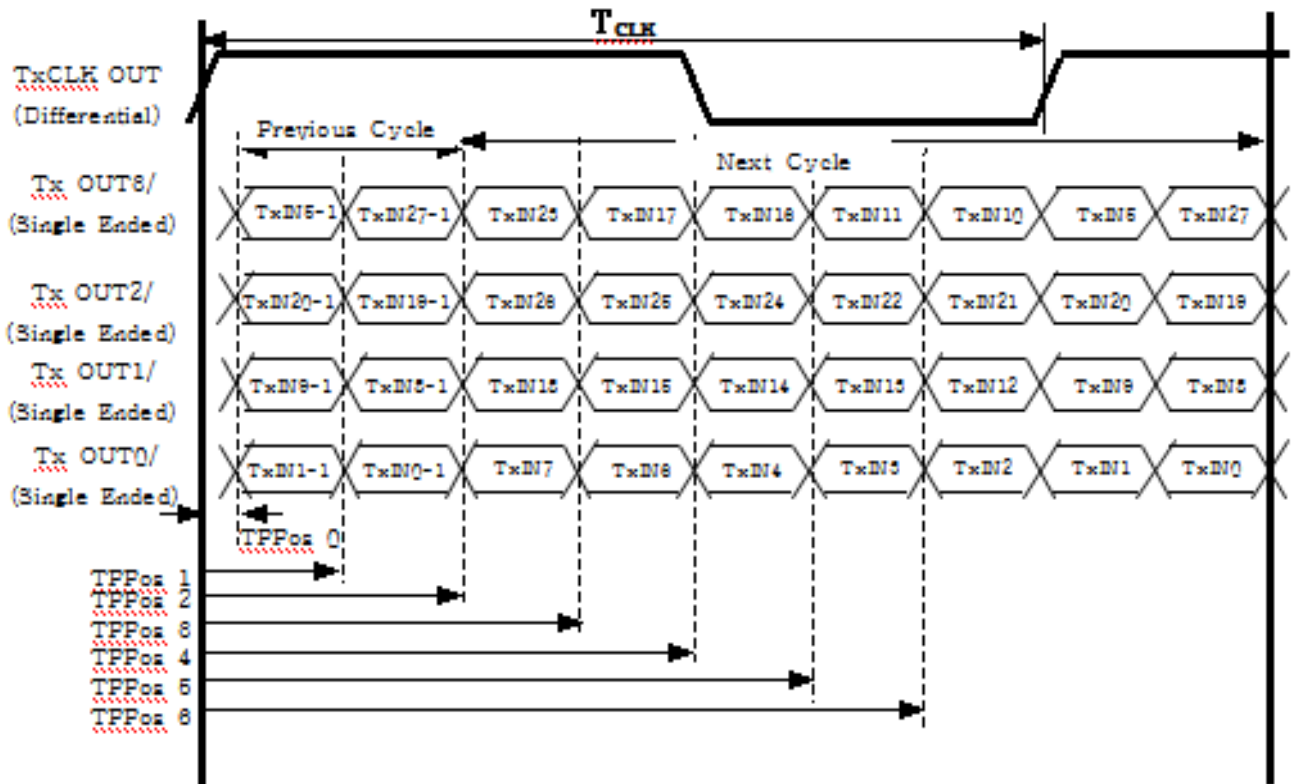


FIGURE 7, Transmitter LVDS OUTPUT PULSE POSITION MEASUREMENT

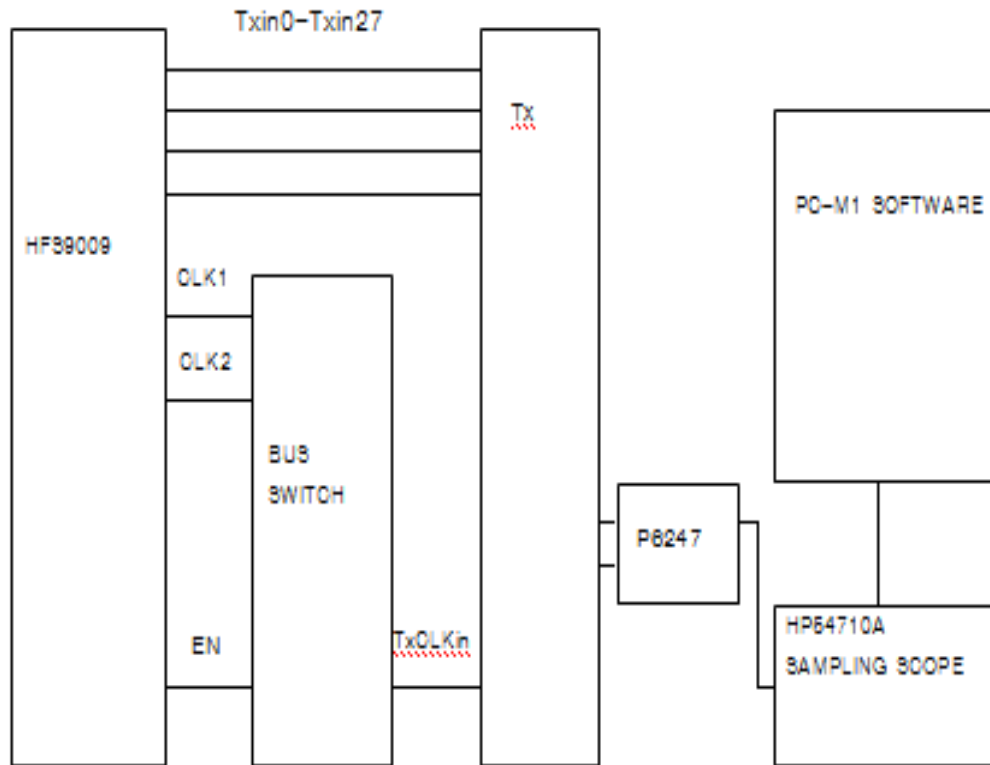


FIGURE 8. TJCC TEST SET-UP -DS90C385 SHOWN

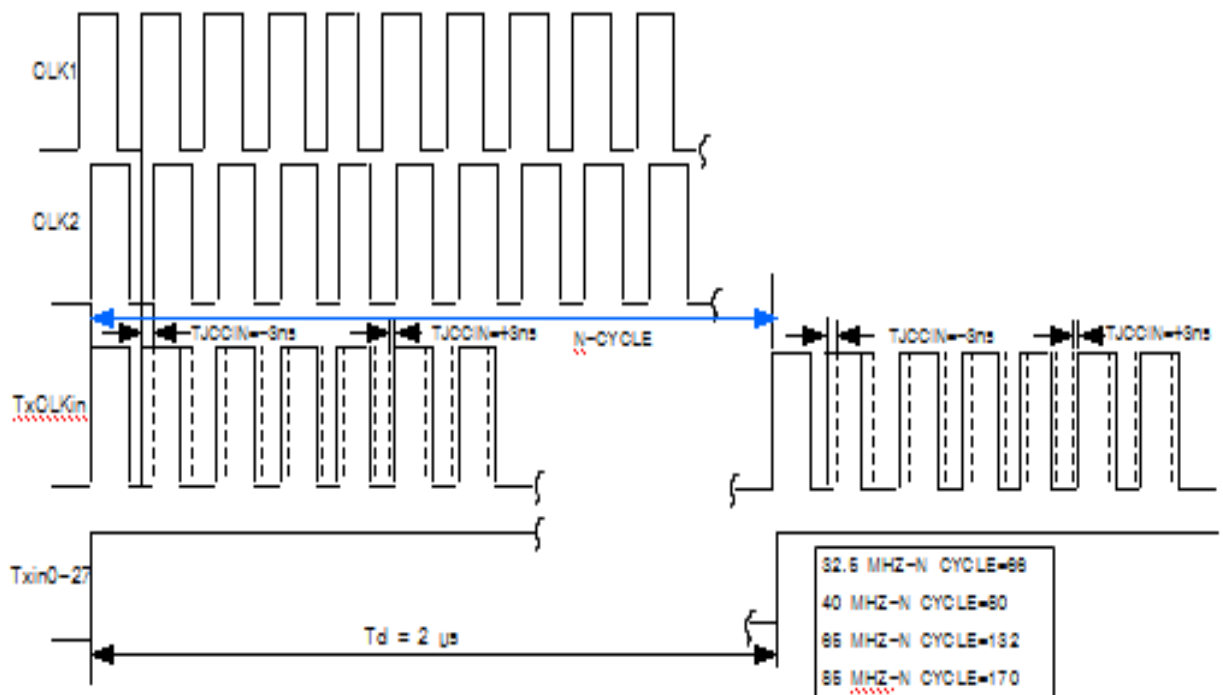


FIGURE 9. TIMING DIAGRAM OF THE INPUT CYCLE TO CYCLE CLOCK JITTER

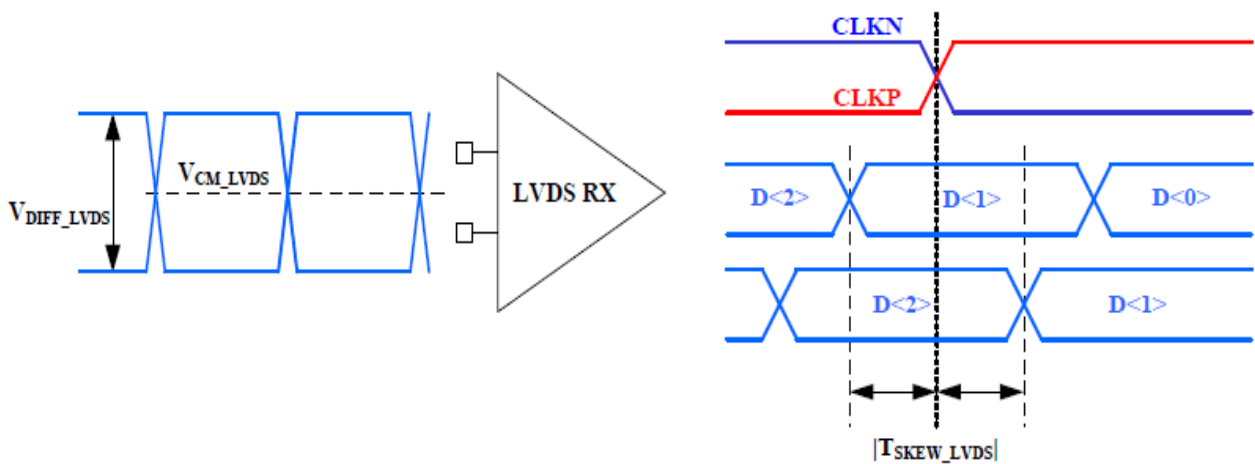
### 6.3 Characteristics of Input data of LVDS

#### (1) DC Specification

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$V_{DIFF\_LVDS}$	LVDS differential input	$V_{CM\_LVDS}=1.2V$		100		600	mv
$V_{CM\_LVDS}$	Input common level			VSSL +0.6	1.2	VDDL -0.6	V
$I_{DD\_LVDS}$	Dynamic current consumption	$V_{CM\_LVDS}=1.2V$ $V_{DIFF\_LVDS}=200mV$	Within One LOT	-10%	13	+10%	mA
			Within Total LOT	-20%	13	+20%	
$I_{DS\_LVDS}$	Static current consumption	$F_{CLK}=85MHz$	Within One LOT	-10%	13	+1-%	
			Within Total LOT	-20%	13	+20%	

#### (2) AC Specification

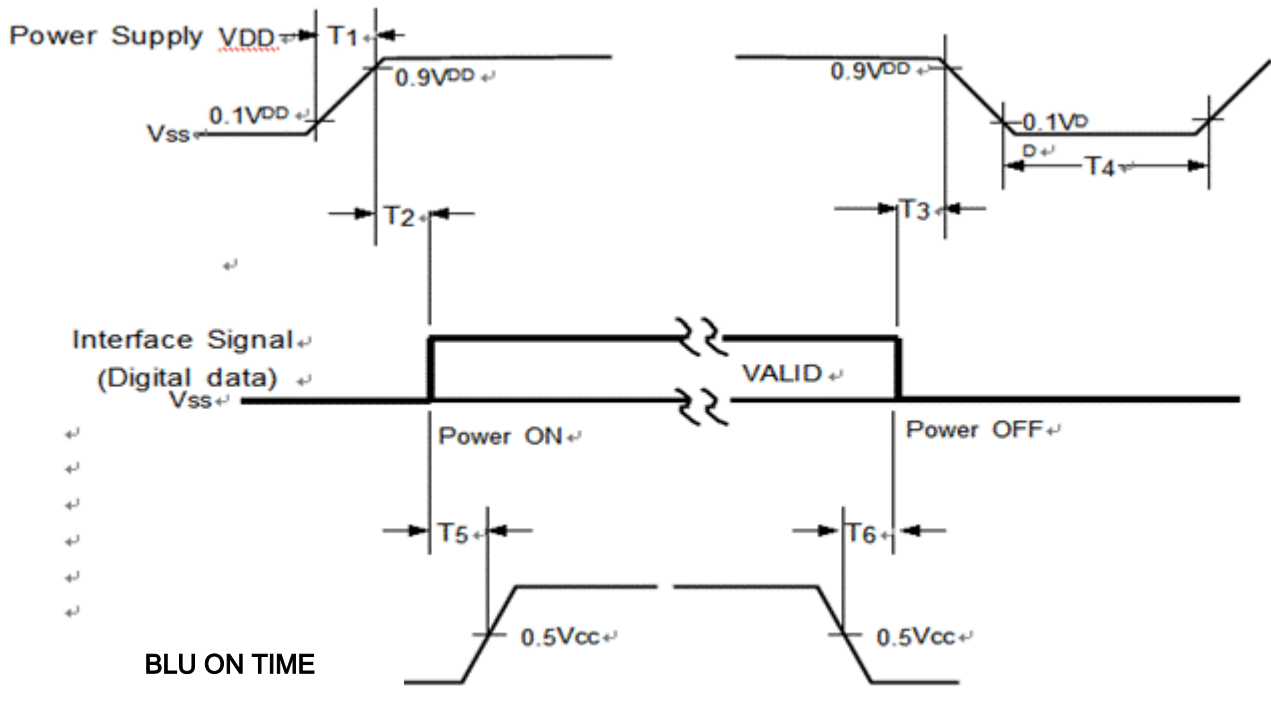
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{DIFF\_LVDS}$	LVDS differential input	$V_{CM\_LVDS}=1.2V$	100		600	mv
$V_{CM\_LVDS}$	Input common level		VSSL +0.6	1.2	VDDL -0.6	V
$F_{CLK}$			55	75	85	MHz
$T_{SKEW\_LVDS}$	CLOCK data skew margin	$F_{CLK}=85MHz$			400	pS



< Fig 10.1.1 > AC characteristic of LVDS

### 6.4 The sequence of power on and off

To prevent a latch-up phenomena or the DC operation of the LCD Module, the power on/off sequence should be accorded with the settings described in the diagram below.



T1 : 0.5 msec <math>T1 \le 10\text{msec}</math>

T2 : 10 msec <math>T2 \le 50\text{msec}</math>

T3 : 0msec <math>T3 \le 50\text{msec}</math>

T4 : 1000msec <math>\le T4</math>

T5: 1000msec <math>\le T5</math> (BLU ON TIME : Converter ENA Signal(ON))

T6 : 100msec <math>\le T6</math> (BLU OFF TIME : Converter ENA Signal(OFF))

T1 : The time, during which the level of  $V_{DD}$  is rising from 10% to 90%.

T2 : The change for the time, during which the  $V_{DD}$  start rising the level above 90% until the valid data of signal started coming in.

T3 : The change for the time, during which the valid data of signal started coming until the  $V_{DD}$  started coming out.

T4 : The time, during which the  $V_{DD}$  start coming out to restart the Windows.

T5 : The time, during which the valid data starts coming in until the power of B/L exceed 50%.

T6 : The time, during which the level of B/L's power falls below 50% until the valid data of signal starts coming out.

- The inputted  $V_{DD}$ 's value for supply voltage, BLU, and signal to the external system of the module shall be computed in observance of the former mentioned value.
- The method to apply the voltage to the lamp within the range, which the LCD operates. When the back-light is turned on before the LCD is operated or the power of LCD is turned off before the back-light is turned off, the abnormal display on the screen may be shown momentarily.
- Please keep the level of input signal low or keep the level of impedance high when the  $V_{DD}$  is off.
- The value shall be measured after the module has been fully discharged between the periods when the power is on and off during the T4.

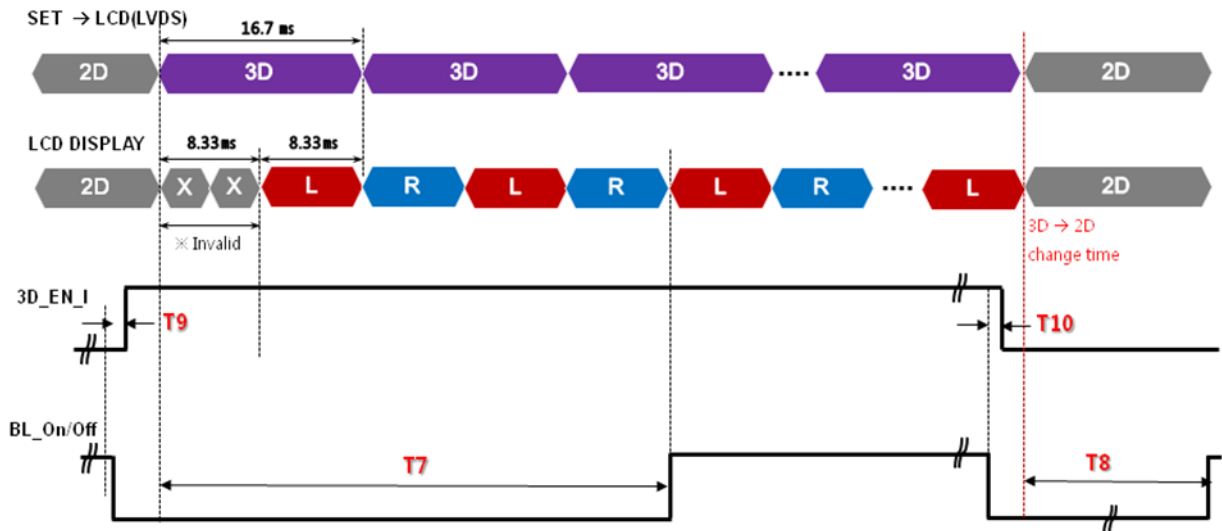
- 3D Input Source Definitions

For the 3D operating of the Model, 3D drive Source of the 60Hz Frame sequential method must be input.  
3D operating cannot support 3D drive Source of another Format.

3D Input Pin Definitions

Pin Number	Pin name	Remark
26	3D_EN	If Voltage Level of 3D_EN Signal is High(3.3V), 3D MODE operate.
5	3D_SYNC_O	This Pin is L/R Sync output signal of Shutter Glass
4,6	3D_Format 0 3D_Format 1	3D input format selection FORMATI[1:0] : 2'b0x = Line interleave , 2'b10 = side/side, 2'b11 = top/bottom

- VNB 60++ 3D Timing

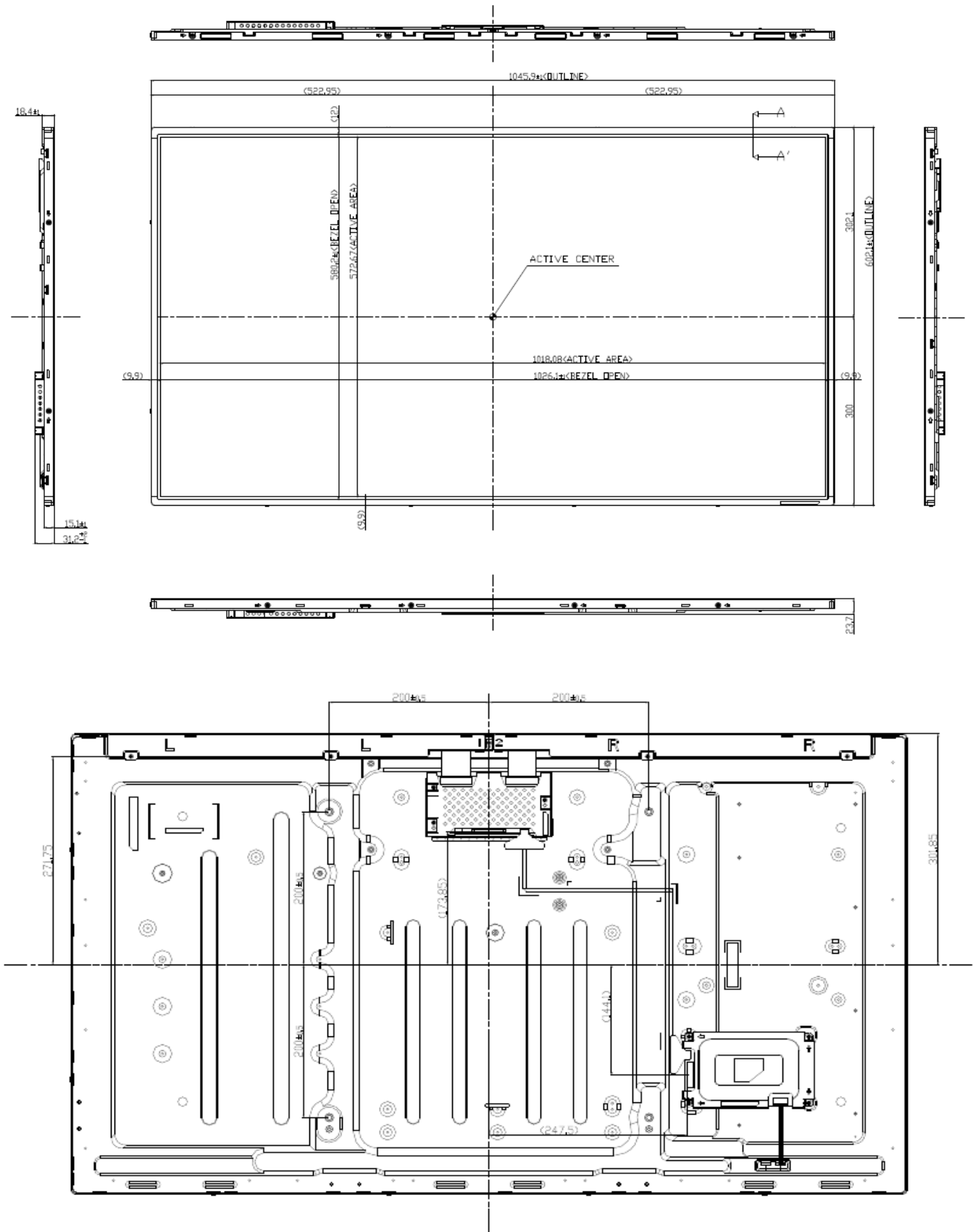


	Spec (ms)			Description
	Min.	Typ	Max	
T7	≥42 msec	-	-	Backlight should be on after 10 frame when 3D signal input from SET
T8	≥30 msec	-	-	Backlight should be off after 7 frame when 3D signal change to 2D signal from SET
T9	≥ 0			
T10	≥ 0			

※ 1 frame (=4.17ms / 240Hz)



7. Outline dimension



## 8. Reliability test

Items to be evaluated	Condition for the evaluation	Quantity	Standard for evaluation
HTOL	50 °C	4	
	60 °C	8	
LTOL	-5°C	4	
THB	Evaluate the whole cell in the panel when examining the panel, which is over 32" at 50°C and 90 %RH.*	10	
Margin on the operation of ASG at a low temperature. (Optional)	Check the temperature when the noise occurs under the conditions, the max. frequency and between the -40°C and 25°C.	Each cell	Applied to products with ASG only.
Margin on the operation of ASG at a high temperature. (Optional)	Examine the panel operated under the conditions, the min. frequency and the 60°C for 96hrs.	Each cell	Applied to products with ASG only.
Residual image at a normal temp.	Repeat the exam. to examine the mosaic pattern(9"*10") of panel at 25 °C for 12hrs followed by the exam for the rolling pattern at 25 °C for 12hrs three times.	8	
New decompression	Examine the panel, which is in the temp. range of -40°C to 50°C between the 0m(0ft) and 13,700m(45,000ft) for 72 and half hrs.	4	
HTS	Store at the 70 °C.	4	
LTS	Store at the -25 °C.	4	
Residual image at the high temperature (optional)	Examine the mosaic pattern(9"*10") of DID at 50°C for 336hrs.	8	Only for DID product
Evaluation for the panel on the pallet	Dropping(20cm)->Set the temp. and humidity(-30°C~60°C / 40°C~90%RH)->Pressurizing-> Vibrating(Vibrate the panel within the frequency range between 5hz and 200hz for 2hrs at the sine wave of 1.05 g.)->Dropping(20cm)	1 Pallet	
Vibration	Vibrate the panel within the frequency range between 10hz and 300hz for 10min at the sine wave at 1.5G Vibrate the panel in the direction of X, Y, and Z axis for 30min.	3	
Shock	If the screen size of panel is below 40", drop the panel with applying the 50G one time toward the direction of ±X, Y, and Z axis from the spot where the panel is placed respectively for 11mSDC. (±XYZ), If the screen size is 46", apply the 40G for ±X and Y axis or the 30G for ±Z. If the screen size is over 52", apply the 30G.	3	
TSS	Test the TV between the -20°C and 65°C 440 times. Test the DID between the -20°C and 65°C 220 times.	4	
WHTS	Store the module at 60 °C and 75 %RH.	4	
TS	Execute the exam for TV at -20°C for 30 min. and at 60°C for 30min 100 times. / Execute the exam for the DID at -20°C for 30 min. and at 60°C for 30min 200 times.	4	
Dust	Execute the test to observe the status of falling dust for 5 min. after spraying the dust in the air for 5 SDC. at a normal temperature and normal humidity for 5 hrs. Turn the panel on and off at the interval of 10 min. Execute the test for the DID for 10hrs.	2	

Twist	Examine the 52"-sized module by pushing the one point of panel by 10 degrees forward and backward with fixing other three points for 0.9s 500 times respectively., Examine the 46"-sized module by pushing the one point of panel by 10 degrees forward and backward with fixing other three points for 0.7s 500 times respectively. Examine the 40"-sized module by pushing the one point of panel by 20 degrees forward and backward with fixing other three points for 0.85s 250 times respectively., Examine the 32"-sized module by pushing the one point of panel by 20 degrees forward and backward with fixing other three points for 0.7s 250 times respectively. Examine the 26"-sized module by pushing the one point of panel by 20 degrees forward and backward with fixing other three points for 0.6s 250 times respectively.	4	
Noise	Noise occurred when the frame of instrument is expanded as the operating module emits the heat.: Max 50dB (Below the 10 times when the level of sound is over 36dB.)	2	
Noise	Noise from machine : Under the 23dB on average.	2	
The new compound stress	Repeat the exam, which stresses the panel under the temp. range of -20°C to 60°C and the humidity range of 0%RH to 90%RH two times.	4	
ESD	Shoot the ESD with the measuring gun, which is operated at ±10 kV to the 210 points with contacting the panel.	3	
	Shoot the ESD with the measuring gun, which is operated at ±20 kV to the 210 points without contacting the panel.	3	
	Input pin for inverter and converter (optional): Apply ±15kV three times.	3	Only for the attached part of inverter and converter.

**[Criteria on evaluation]**

The components of product, which may affect to the function of display shall not be changed when the display quality test is executed under the normal operating condition.

- \* HTOL/ LTOL : The operating at the high and low temperature\*
- \* THB : The slant of temperature and humidity
- \* HTS/ LTS : The storage at the high and low temperature
- \* WHTS : The storage condition at the high temperature with the high humidity

## 9. General precautions

### 9.1 Handling

- (a) When assembling, attach the panel kit and BLU kit to the system firmly by combining all mounting holes. Be careful not to give any adverse effects to the panel kit and the BLU kit.
- (b) Be careful not to give any adverse effects to the panel and BLU kit when designing the set.
- (c) Be cautious not to give any strong, adverse shocks and/or any forces to the panel kit.  
Applying any forces to the panel may cause the panel kit and the back-light kit to operate abnormally or to be damaged.
- (d) Refrain from applying any forces to the source PBA and the drive IC while handling or installing them to the set. Any forces applied to the sets may cause damage or a malfunction to the panel kit.
- (e) Refrain from applying any forces which causes a constant shock to the back side of panel kit, the set design and BLU kit. Any forces applied to the products may cause an abnormal display, a functional failure and etc.
- (f) Note that polarizer could be damaged easily.  
Do not press or scratch the bare surface with the material which is harder than a lead of HB pencil.
- (g) Wipe off water droplets or oil immediately. If you leave the droplets on the product for a long time, a staining or the discoloration may occur.
- (h) If the surface of the polarizer is dirty, clean it using the absorbent cotton or the soft cloth.
- (i) Desirable cleaners are water or IPA (Isopropyl Alcohol).  
Do not use Kenton type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. These solutions may cause the permanent damage to the polarizer by the chemical reaction.
- (j) If the liquid crystal leaks from the panel, it is recommended to keep it away from the eyes or mouth. If the user's hands, legs, or clothes contacts with the liquid crystal, it is recommended to wash your applied area with soap thoroughly and see a doctor for the medical examination.
- (k) Protect the panel kit and a BLU Kit from the static electricity. Otherwise, the circuit IC could be damaged.

- Reference: Process for controlling the standard of SDC

No.	Item	Standard for control
1	Ionizer	All equipment shall be controlled under 150V.(Typ. 100V)
2	Carrying Roller	The roller for carrying shall be controlled under 200V.
3	Resistance for grounding of equipment	All resistances for grounding of equipment shall be less than 1ohm.

- (l) Remove the stains with wearing finger-stalls on the top of soft gloves in order to keep the display clean in the process of the incoming inspection and the assembly process.
- (m) Do not pull or fold the source drive IC which connects to the source PBA and the panel or the gate drive IC.
- (n) Be cautious not to pull, fold or bend the source drive IC and the gate drive IC in any processes.  
Being bent one time on the source drive IC is allowed while assembling the panel Kit and the BLU Kit.
- (o) Don't change a figure for the variable resistor located on the panel kit and BLU kit except when inputting the changed figure for the flicker.

- (p) Do not touch pins on the interface connector directly with bare hands.
- (q) Be cautious the protection film not to be peeled off.

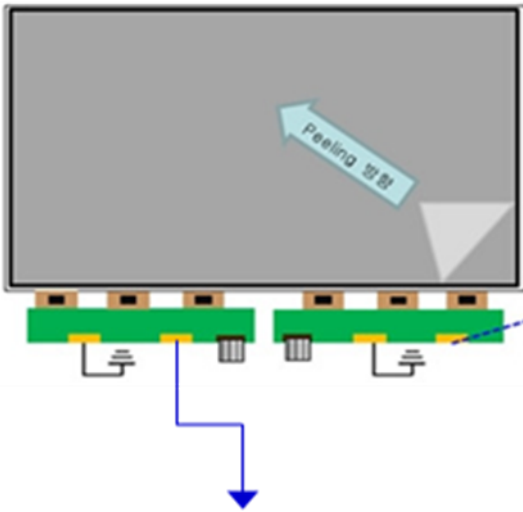


Fig. GND SR-Open Pattern – Be sure to be contacted to the ground while peeling of the protection film

- Make sure to peel the protection film off slowly.  
(It is recommended to peel it off at the speed of more than 8SDC. constantly.)
- The direction for peeling is shown at the left fig.
- Instruct the worker to follow the adequate instructions such as wearing the antistatic wrist band.
- Make sure the source PBA to be grounded while peeling the protection film.
- The Ionized air should be injected while peeling.
- The protection film shall not be contacted to the source drive IC.
- If the adhesive marks are remained on the polarizer after peeling the protection film off, it is recommended to remove marks with isopropyl-alcohol liquid.

- (r) Peel the protection film for the polarizer off on the panel kit slowly just before using it in order for the effect by the electrostatic charge to be minimized.
- (s) The panel kit and the BLU kit have circuits with a high frequency. The set manufacturers shall suppress the EMI sufficiently.
- (t) The set which the panel is assembled shall not be twisted. The twisted set may cause the damage.
- (u) The S D-IC chip must be contacted with the top chassis.

**9.2 Storage**

ITEM	Unit	Min.	Max.
Storage Temperature	(°C)	5	40
Storage Humidity	(%rH)	35	75
Storage life	12 months		
Storage Condition	<ul style="list-style-type: none"> <li>- The storage room shall be equipped with a good ventilation facility, which has a temperature controlling system.</li> <li>- Products shall be placed on the pallet, which is away from the wall not on the floor.</li> <li>- Prevent products from being exposed to the direct sunlight, moisture, and water.; Be cautious not to pile the products up.</li> <li>- Avoid storing products in the environment where other hazardous material is placed.</li> <li>- If products are delivered or kept in the storage facility more than 3 months, we recommend you to leave products under the condition including a 20°C temperature and a humidity of 50% for 24 hours.</li> </ul>		

**9.3 Operation**

- (1) Do not connect or disconnect the cable to the module at the "Power On" condition.
- (2) The power shall be always turned on/off by the item 6.4. "Power on/off sequence"
- (3) The module has a circuit with a high frequency. The electromagnetic interference shall be suppressed by system manufacturers sufficiently. The method to ground and shield is important to minimize the interference.
- (4) Design the length of cable to connect between the connector for back-light and the inverter as short as possible and the shorter cable shall be connected directly.

The cable between the back light connector and its converter power supply should be connected directly with a minimized length. A longer cable between the back light and the converter may cause lower luminance of LED package and may require higher startup voltage(Vs).

9.4 Operation condition guide

(a) The LCD product shall be operated under normal conditions.

The normal condition is defined as below;

- Temperature: 20±15°C
- Humidity: 55±20%
- Display pattern: continually changing pattern (Not stationary)

(b) If the product will be used under extreme conditions such as under the high temperature, humidity, display patterns or the operation time etc., it is strongly recommended to contact SDC for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.-

9.5 Others

- (a) The ultra-violet ray filter is necessary for the outdoor operation.
- (b) Avoid the condensation of water which may result in the improper operation of product or the disconnection of electrode.
- (c) Do not exceed the limit on the absolute maximum rating. (For example, the supply voltage variation, the input voltage variation, the variation in content of parts and environmental temperature, and so on) If not, the module may be damaged.
- (d) If the module keeps displaying the same pattern for a long period of time, the image may be remained to the screen. To avoid the image sticking, it is recommended to use a screen saver.
- (e) This module has its circuitry of PCB's on the rear side and should be handled carefully in order for a force not to be applied.
- (f) Please contact the SDC in advance when the same pattern is displayed for a long time.

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