

# Programmable Micropower Hex Translator/ Receiver/Driver

## FEATURES

- Efficiently Translate Voltage Levels
- Internal Hysteresis for Noise Immunity
- Output Latches Included
- Three-State Outputs
- Programmable Power/Speed
- Power Can Be Completely Shut Off
- $\pm 50V$  on Inputs with External 100k Limit Resistor
- $1.2\mu s$  Response at  $100\mu A$  Supply Current

## APPLICATIONS

- TTL/CMOS to  $\pm 5V$  Analog Switch Drive
- TTL to CMOS (3V to 15V  $V_{CC}$ )
- ECL to CMOS (3V to 15V  $V_{CC}$ )
- Ground Isolation Buffer
- Low Power RS232 Line Receiver

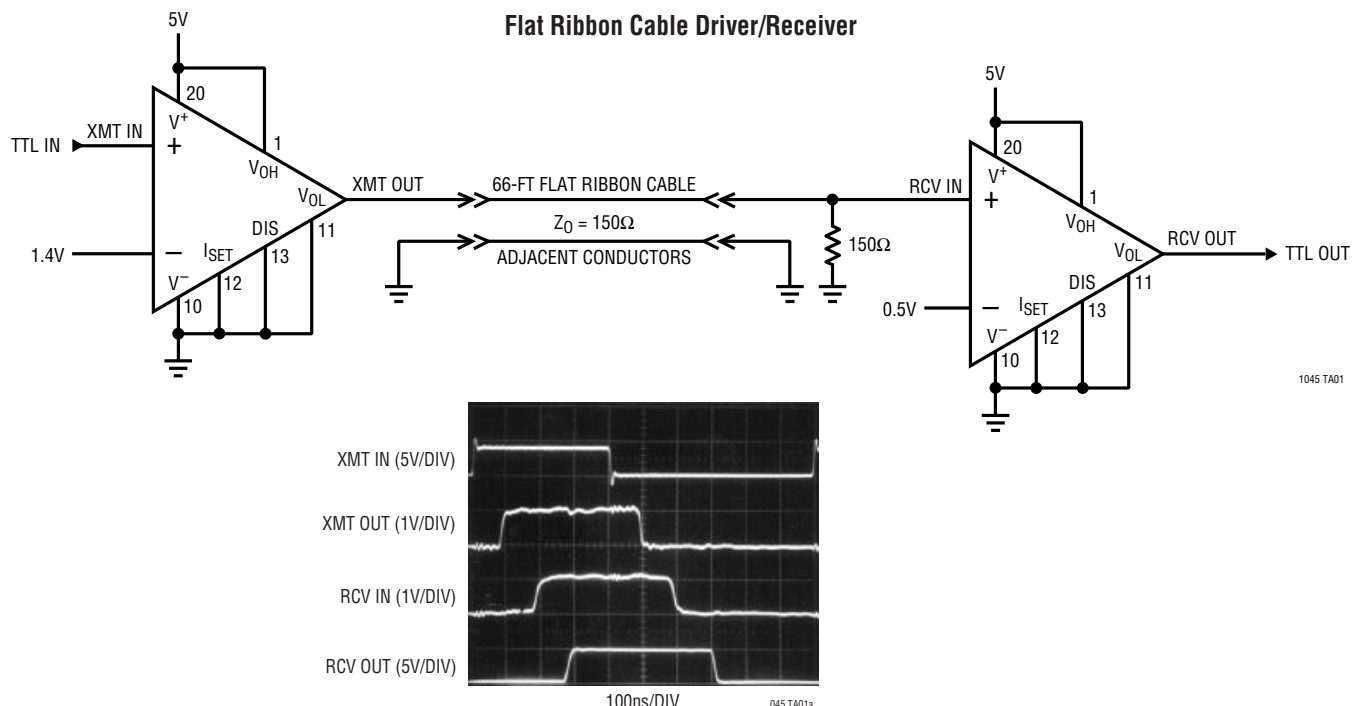
## DESCRIPTION

The LTC<sup>®</sup>1045 is a hex level translator manufactured using Linear Technology's enhanced LTCMOS<sup>™</sup> silicon gate process. It consists of six high speed comparators with output latches and three-state capability. Each comparator's plus input is brought out separately. The minus inputs of comparators 1 to 4 are tied to  $V_{TRIP1}$  while 5 and 6 are tied to  $V_{TRIP2}$ .

The  $I_{SET}$  pin has several functions. When taken to  $V^+$  the outputs are latched and power is completely shut off. Power/speed can be programmed by connecting  $I_{SET}$  to  $V^-$  through an external resistor.

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## TYPICAL APPLICATION



## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Total Supply Voltage ( $V^+$ , $V_{OH}$ to $V^-$ , $V_{OL}$ )	18V
Output High Voltage ( $V_{OH}$ )	$\leq V^+$
Input Voltage	18V to ( $V^- - 0.3V$ )
Output Short-Circuit Duration ( $V_{OH} - V_{OL} \leq 10V$ )	Continuous
ESD (MIL-STD-883, Method 3015)	2000V
Operating Temperature Range	$-40^\circ\text{C}$ to $85^\circ\text{C}$
Storage Temperature Range	$-55^\circ\text{C}$ to $150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	$300^\circ\text{C}$

## PACKAGE/ORDER INFORMATION

<p>N PACKAGE 20-LEAD PDIP SW PACKAGE 20-LEAD SO WIDE <math>T_{JMAX} = 110^\circ\text{C}</math>, <math>\theta_{JA} = 90^\circ\text{C/W}</math> (N) <math>T_{JMAX} = 110^\circ\text{C}</math>, <math>\theta_{JA} = 90^\circ\text{C/W}</math> (SW)</p> <p>J PACKAGE 20-LEAD CERDIP <math>T_{JMAX} = 150^\circ\text{C}</math>, <math>\theta_{JA} = 70^\circ\text{C/W}</math> (J)</p> <p><b>OBSOLETE PACKAGE</b> Consider N Package for Alternate Source</p>	ORDER PART NUMBER
	LTC1045CN LTC1045CSW

LTC1045CJ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = V_{OH} = 5V$ ,  $V^- = V_{OL} = 0V$  unless otherwise specified. (Note 3).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$I_B$	Input Bias Current	$V^- \leq V_{IN} \leq V^+$	●	$\pm 1$	0.5	nA $\mu\text{A}$
	Trip Voltage Range (Pins 8, 9)		●	$V^-$	$V^+ - 2$	V
$I_S$	$V^+$ to $V^-$ Supply Current	DISABLE = $V^+$ , $R_{SET} = 10k$	●	2.5	3.5 4.5	mA mA
	$V^+$ to $V^-$ Supply Current in Shutdown	DISABLE = $I_{SET} = V^+$	●	10	1	nA $\mu\text{A}$
$V_{REF}$	Voltage on $I_{SET}$ (Pin 12)	$R_{SET} = 10k$	●	0.6	0.9 1.25	V V
	$V_{OH}$	TTL Output High Voltage	●	2.4	4.4	V
$V_{OL}$	TTL Output Low Voltage	●		0.2	0.4	V
$I_{SINK}$	Output Short-Circuit Sink Current	$V_{IN} = V_{TRIP} - 100mV$ , $V_{OUT} = V^+$	●	7.5 5.5	15	mA mA
	Output Short-Circuit Source Current	$V_{IN} = V_{TRIP} + 100mV$ , $V_{OUT} = V^-$	●	4.0 3.2	8.0	mA mA
$I_{OZ}$	Three-State Leakage Current	DISABLE = $V^+$ , $V_{OL} \leq V_{OUT} \leq V_{OH}$	●	0.005	1	$\mu\text{A}$ $\mu\text{A}$
	$R_{OH}$	Output Resistance to $V_{OH}$	●		260 475 600	$\Omega$ $\Omega$ $\Omega$
$R_{OL}$		Output Resistance to $V_{OL}$	●		100 180 250	$\Omega$ $\Omega$ $\Omega$
		$I_{SET}$ Voltage for Shutdown	●	$V^+ - 0.5$		V
$V_{IH}$ $V_{IL}$	DISABLE Input Logic Levels	$V^+ = 4.5V$ , $V^- = 0V$ $V^+ = 5.5V$ , $V^- = 0V$	● ●	2.0	0.8	V V
	Input Supply Differential ( $V^+ - V^-$ ) (Note 3)		●	4.5	15	V
	Output Supply Differential ( $V_{OH} - V_{OL}$ ) (Note 3)		●	3	15	V

1045fc

**AC ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = V_{OH} = 5\text{V}$ ,  $V^- = V_{OL} = 0\text{V}$ , unless otherwise specified.

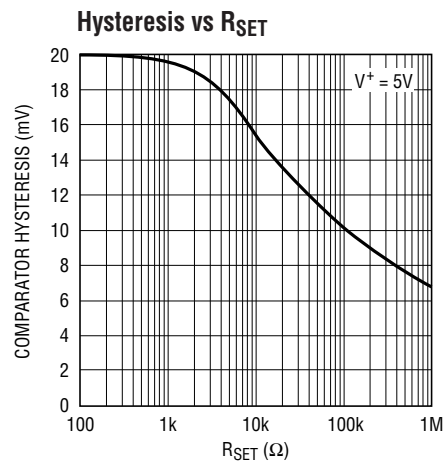
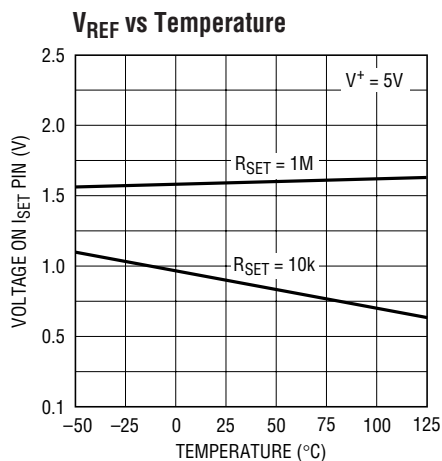
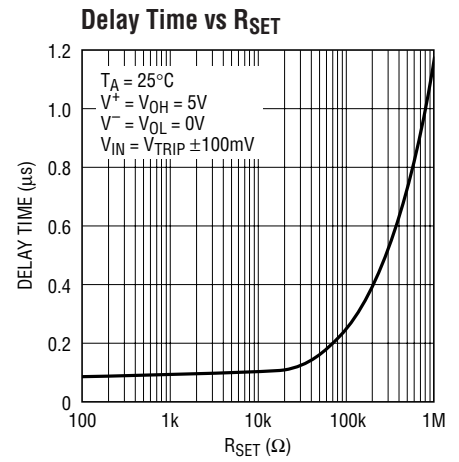
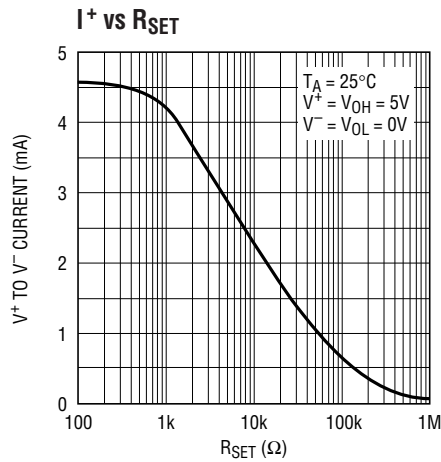
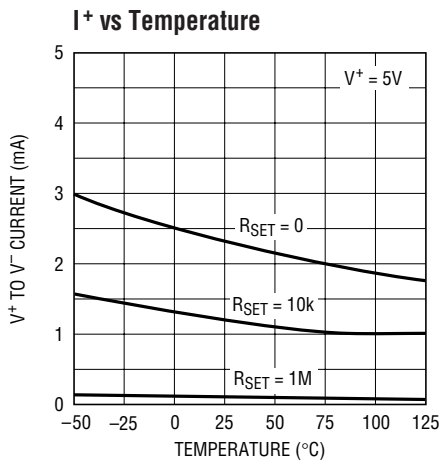
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_d$	Response Time	Test Circuit Figure 1 $R_{SET} = 10\text{k}$ , $\pm 100\text{mV}$ Drive			250 350	ns
$t_{SETUP}$	Time Before Rising Edge of $I_{SET}$ that Data Must Be Present	Test Circuit Figure 2		80		ns
$t_{HOLD}$	Time After Rising Edge of $I_{SET}$ that Data Must Be Present	Test Circuit Figure 2		0		ns
$t_{ACC}$	Falling Edge of DISABLE to Logic Level (from Hi-Z State)	Test Circuit Figure 3		165		ns
$t_{IH}, t_{OH}$	Rising Edge of DISABLE to Hi-Z State	Test Circuit Figure 3		200		ns

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The maximum differential voltage between any two power pins ( $V^+$ ,  $V^-$ ,  $V_{OH}$  and  $V_{OL}$ ) must not exceed 18V. The maximum recommended operating differential is 15V.

**Note 3:** During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple or ground noise; any of these conditions must not cause a supply differential to exceed the absolute maximum rating.

**TYPICAL PERFORMANCE CHARACTERISTICS**



## PIN FUNCTIONS

**V<sub>OH</sub> (Pin 1):** High Level to which the Output Switches.

**IN1 to IN7 (Pins 2 to 7):** Six Comparator Inputs; Voltage Range = V<sup>-</sup> to V<sup>+</sup> + 18V.

**V<sub>TRIP2</sub> (Pin 8):** Trip Point for Last Two Comparators (Inputs 5,6); Voltage Range = V<sup>-</sup> to V<sup>+</sup> - 2V.

**V<sub>TRIP1</sub> (Pin 9):** Trip Point for First Four Comparators (Inputs 1 to 4); Voltage Range = V<sup>-</sup> to V<sup>+</sup> - 2V.

**V<sup>-</sup> (Pin 10):** Comparator Negative Supply.

**V<sub>OL</sub> (Pin 11):** Low Level to which the Output Switches.

**I<sub>SET</sub> (Pin 12):** This has three functions: 1) R<sub>SET</sub> from this pin to V<sup>-</sup> sets bias current, 2) when forced to V<sup>+</sup> power is shut off completely and 3) when forced to V<sup>+</sup> outputs are latched.

**DISABLE (Pin 13):** When high, outputs are Hi-Z.

**OUT6 to OUT1 (Pins 14 to 19):** Six Driver Outputs.

**V<sup>+</sup> (Pin 20):** Comparator Positive Supply.

## TEST CIRCUITS

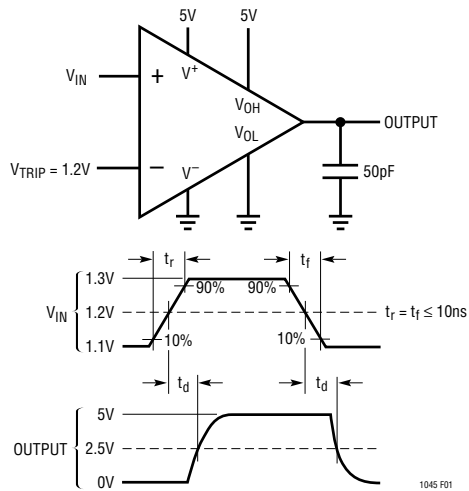


Figure 1. Response Time Test Circuit

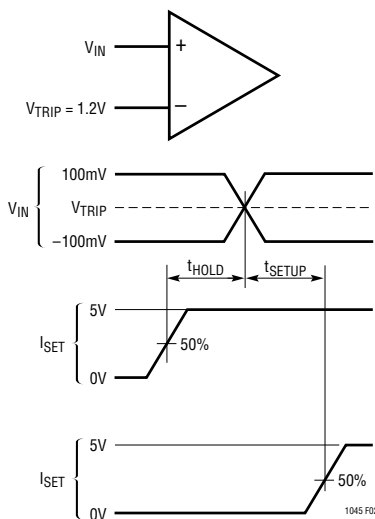


Figure 2. Latch Test Circuit

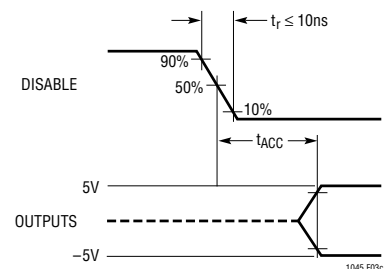
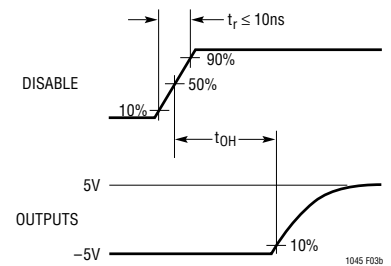
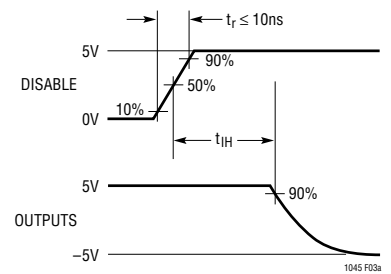
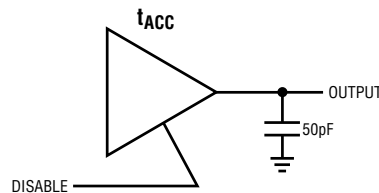
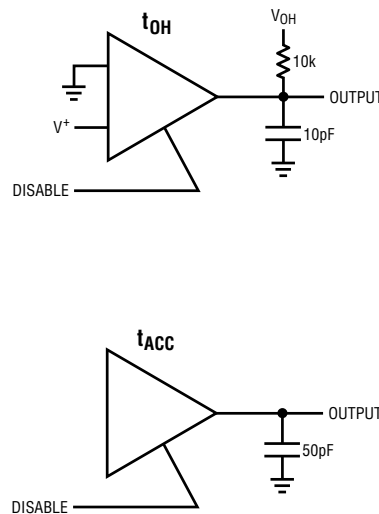
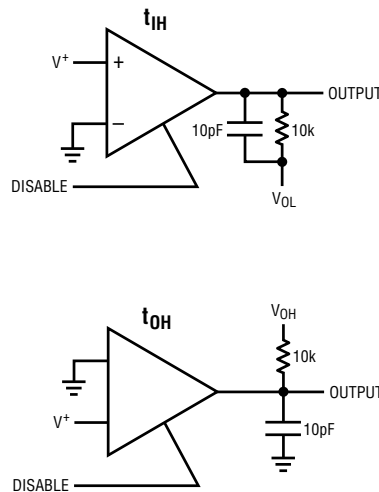
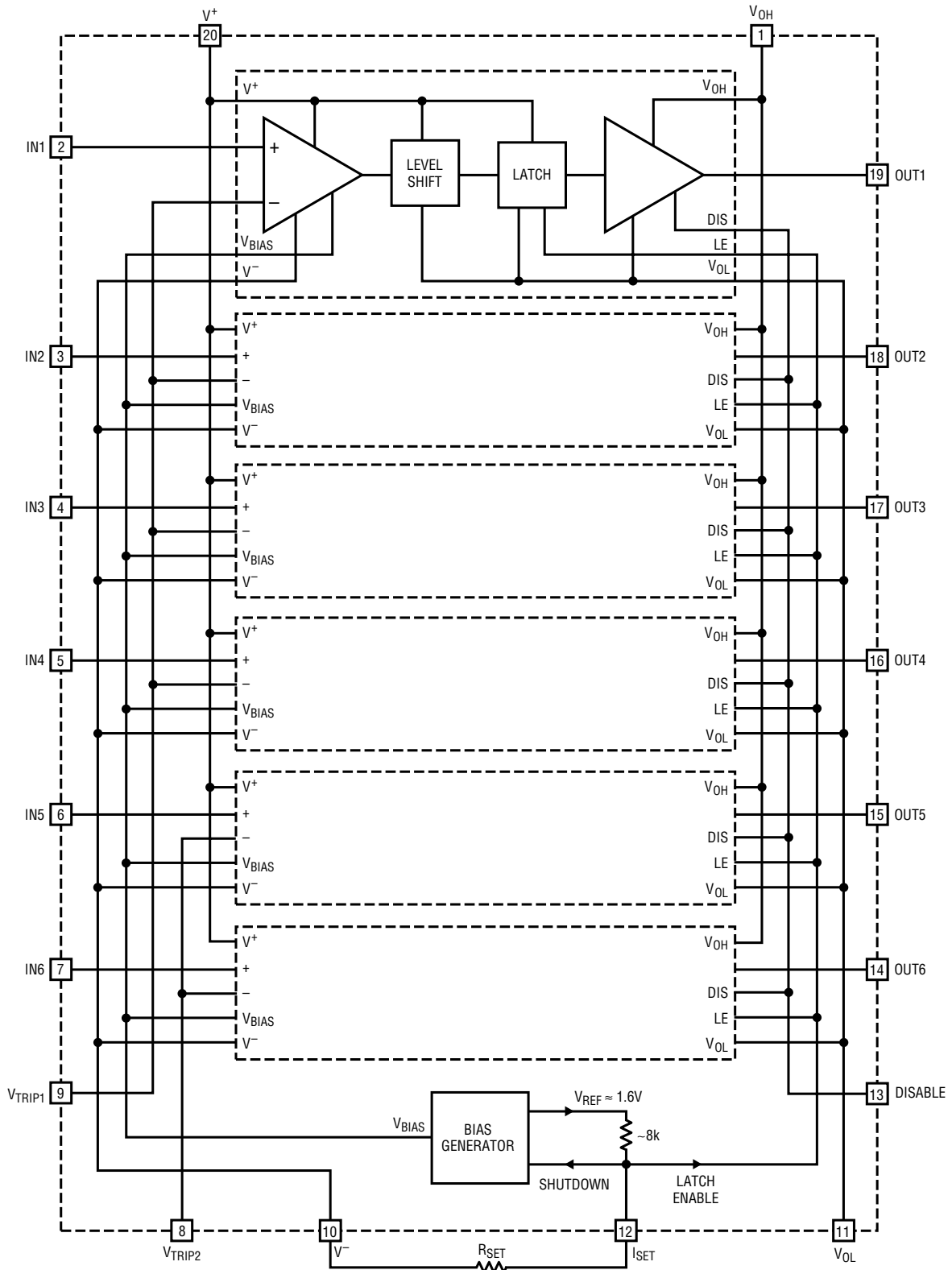


Figure 3. Three-State Output Test Circuit  
Conditions: V<sup>+</sup> = V<sub>OH</sub> = 5V, V<sup>-</sup> = V<sub>OL</sub> = 0V

# BLOCK DIAGRAM



1045 BD

## APPLICATIONS INFORMATION

The LTC1045 consists of six voltage translators and associated control circuitry (see Block Diagram). Each translator has a linear comparator input stage with the positive input brought out separately. The negative inputs of the first four comparators are tied in common to  $V_{TRIP1}$  and the negative inputs of the last two comparators are tied in common to  $V_{TRIP2}$ . With these inputs the switching point of the comparators can be set anywhere within the common mode range of  $V^-$  to  $V^+ - 2V$ . To improve noise immunity each comparator has a small built-in hysteresis. Hysteresis varies with bias current from 7mV at low bias current to 20mV at high bias current (see typical curve of Hysteresis vs  $R_{SET}$ ).

### Setting the Bias Current

Unlike CMOS logic, any linear CMOS circuit must draw some quiescent current. The bias generator (Block Diagram) allows the quiescent current of the comparators to be varied. Bias current is programmed with an external resistor (see typical curve of  $I^+$  vs  $R_{SET}$ ). As the bias current is decreased, the LTC1045 slows down (see typical curve of Delay Time vs  $R_{SET}$ ).

### Shutting Power Off and Latching the Outputs

In addition to setting the bias current, the  $I_{SET}$  pin shuts power completely off and latches the translator outputs. To do this, the  $I_{SET}$  pin must be forced to  $V^+ - 0.5V$ . As shown in Figure 4, a CMOS gate or a TTL gate with a resistor pull-up does this quite nicely. Even though power

is turned off to the linear circuitry, the CMOS output logic is powered and maintains the output state. With no DC load on the output, power dissipation, for all practical purposes, is zero.

Latching the output is fast—typically 80ns from the rising edge of  $I_{SET}$ . Going from the latched to flow-through state is much slower—typically 1.5 $\mu$ s from the falling edge of  $I_{SET}$ . This time is set by the comparator’s power-up time. During the power-up time, the output can assume false states. To avoid problems, the output should not be considered valid until 2 $\mu$ s to 5 $\mu$ s after the falling edge of  $I_{SET}$ .

### Putting the Outputs in Hi-Z State

A DISABLE input sets the six outputs to a high impedance state. This allows the LTC1045 to be interfaced to a data bus. When DISABLE = “1” the outputs are high impedance and when DISABLE = “0” they are active. With TTL supplies,  $V^+ = 4.5V$  to 5.5V and  $V^- = GND$ , the DISABLE input is TTL compatible.

### Power Supplies

There are four power supplies on the LTC1045:  $V^+$ ,  $V^-$ ,  $V_{OH}$  and  $V_{OL}$ . They can be connected almost arbitrarily, but there are a few restrictions. A minimum differential must exist between  $V^+$  and  $V^-$  and  $V_{OH}$  and  $V_{OL}$ . The  $V^+$  to  $V^-$  differential must be at least 4.5V and the  $V_{OH}$  to  $V_{OL}$  differential must be at least 3V. Another restriction is caused by the internal parasitic diode D1 (see Figure 5).

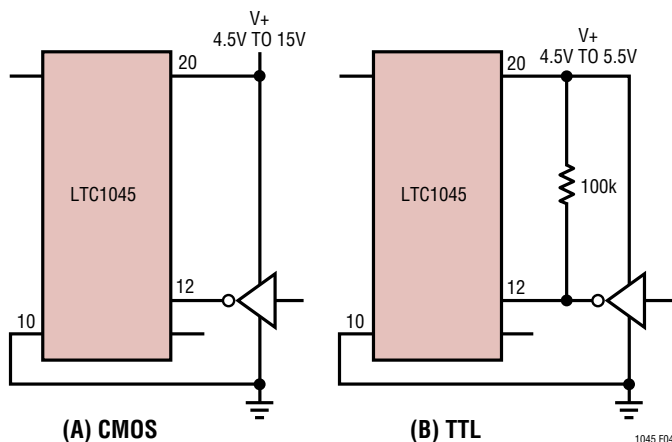


Figure 4. Driving the  $I_{SET}$  Pin with Logic

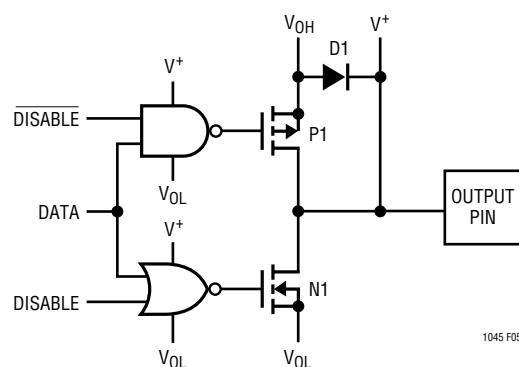


Figure 5. Output Driver

## APPLICATIONS INFORMATION

Because of this diode,  $V_{OH}$  must not be greater than  $V^+$ . Lastly, the maximum voltage between any two power supply pins must not exceed 15V operating or 18V absolute maximum. For example, if  $V^+ = 5V$ ,  $V^-$  or  $V_{OL}$  should be no more negative than  $-10V$ . Note that  $V_{OL}$  should not be more negative than  $-10V$  even if the  $V_{OH}$  to  $V_{OL}$  differential does not exceed the 15V maximum. In this case the  $V^+$  to  $V_{OL}$  differential sets the limit.

### Input Voltage

The LTC1045 has no upper clamp diodes as do conventional CMOS circuits. This allows the inputs to exceed the  $V^+$  supply. The inputs will break down approximately 30V above the  $V^-$  supply. If the input current is limited with  $100k\Omega$ , the input voltage can be driven to at least  $\pm 50V$  with no adverse effects for any combination of allowed

power supply voltages. Output levels will be correct even under these conditions (i.e., if the input voltage is above the trip point, the output will be high and if it is below, the output will be low).

### Output Drive

Output drive characteristics of the LTC1045 will vary with the power supply voltages that are chosen. Output impedance is affected by  $V^+$ ,  $V_{OH}$  and  $V_{OL}$ .  $V^-$  has no effect on output impedance. Guaranteed drive characteristics are specified in the table of electrical characteristics for  $V^+ = V_{OH} = 5V$  and  $V^- = V_{OL} = 0V$ . Figures 6 and 7 show relative output impedance for other supply combinations. In general, output impedance is minimized if  $V^+$  to  $V_{OH}$  is minimized and  $V_{OH}$  to  $V_{OL}$  is maximized.

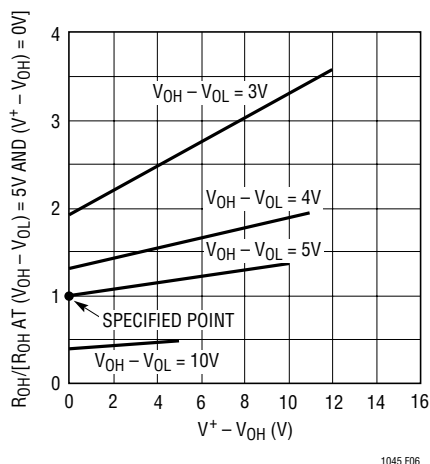


Figure 6. Relative Output Sourcing Resistance ( $R_{OH}$ ) vs  $V^+ - V_{OH}$

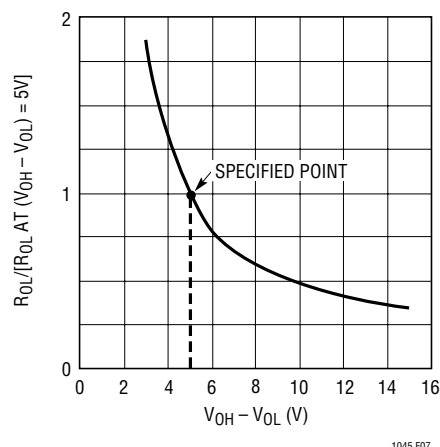
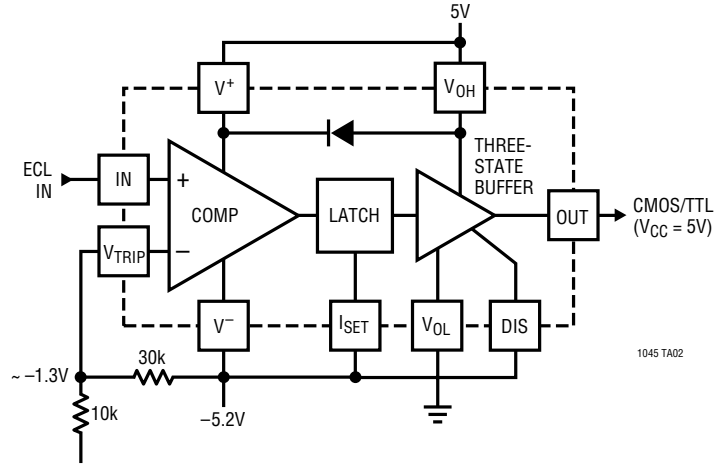


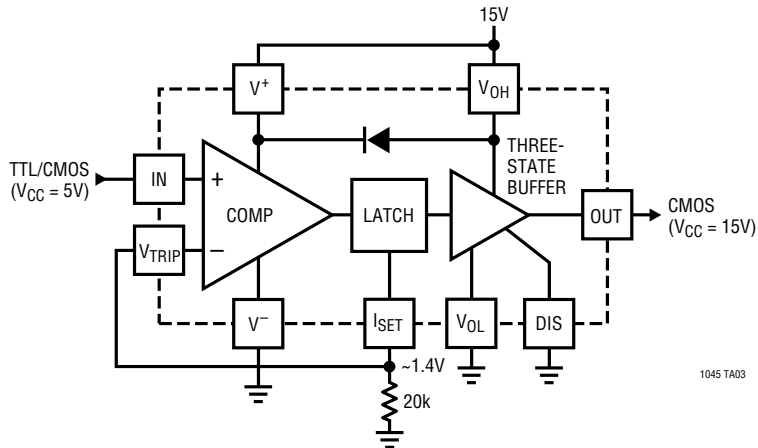
Figure 7. Relative Output Sinking Resistance ( $R_{OL}$ ) vs  $V_{OH} - V_{OL}$

TYPICAL APPLICATIONS

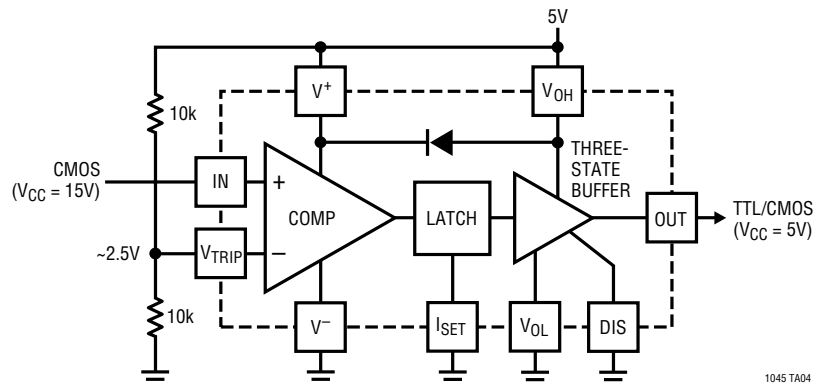
ECL to CMOS/TTL Logic



TTL/CMOS ( $V_{CC} = 5V$ ) to High Voltage CMOS ( $V_{CC} = 15V$ )



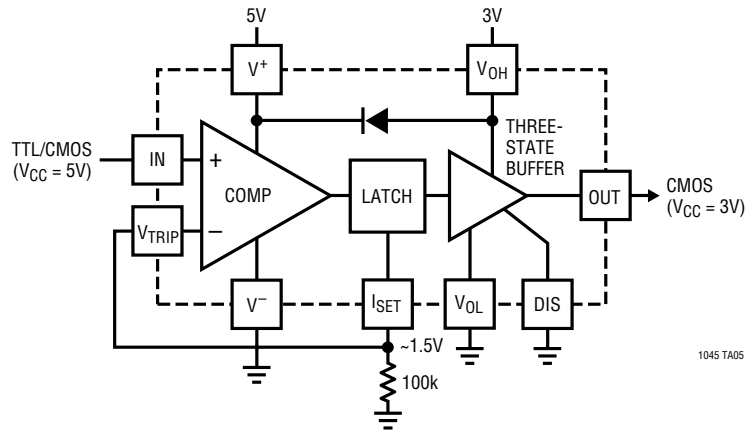
High Voltage CMOS ( $V_{CC} = 15V$ ) to TTL/CMOS ( $V_{CC} = 5V$ )





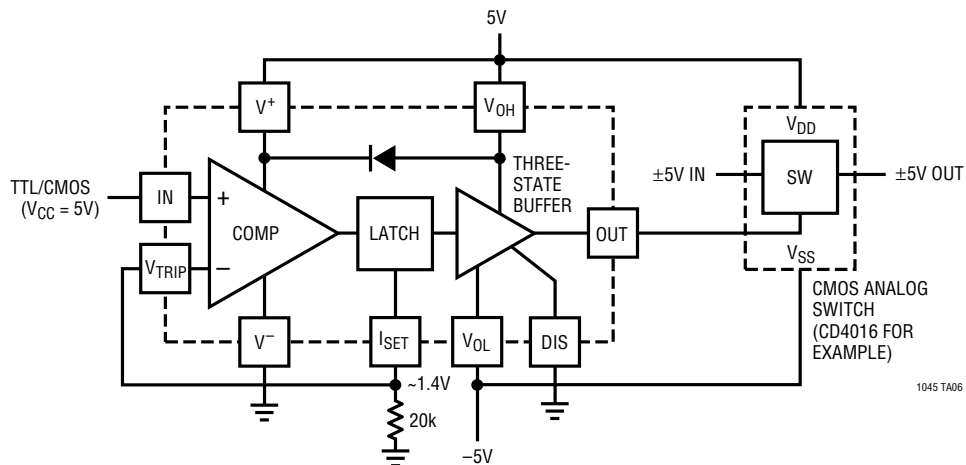
# TYPICAL APPLICATIONS

TTL/CMOS ( $V_{CC} = 5V$ ) to Low Voltage CMOS ( $V_{CC} = 3V$ )



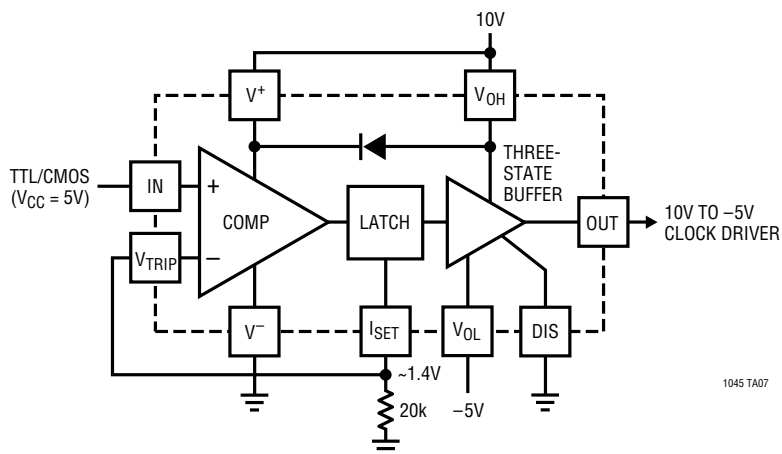
1045 TA05

TTL/CMOS Logic Levels to  $\pm 5V$  Analog Switch Driver



1045 TA06

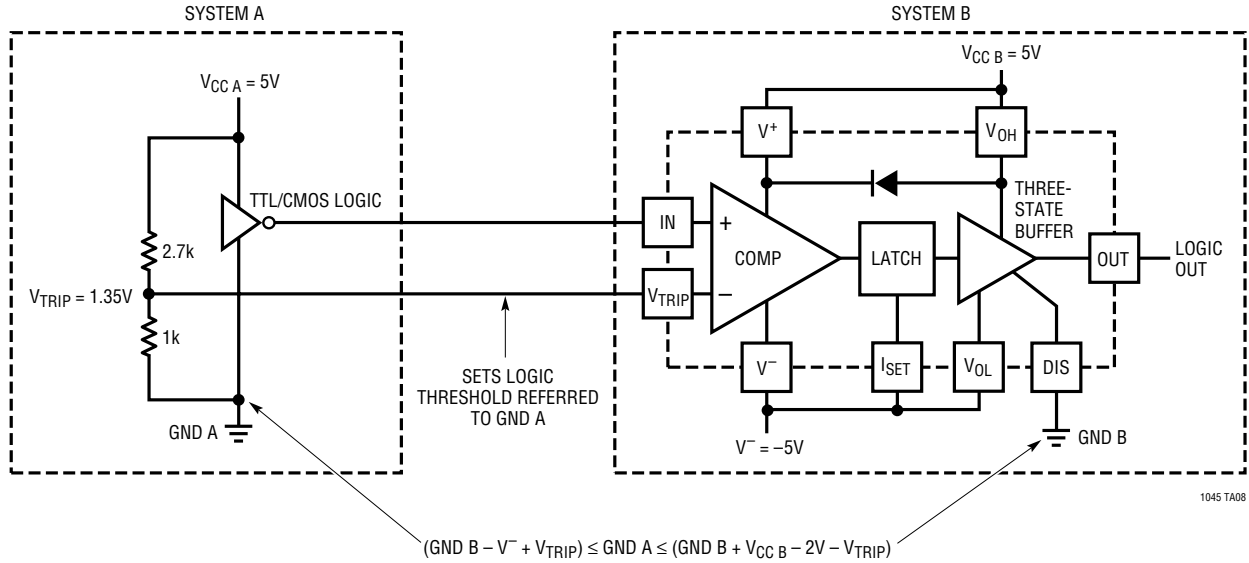
TTL/CMOS ( $V_{CC} = 5V$ ) to 10V/-5V Clock Driver



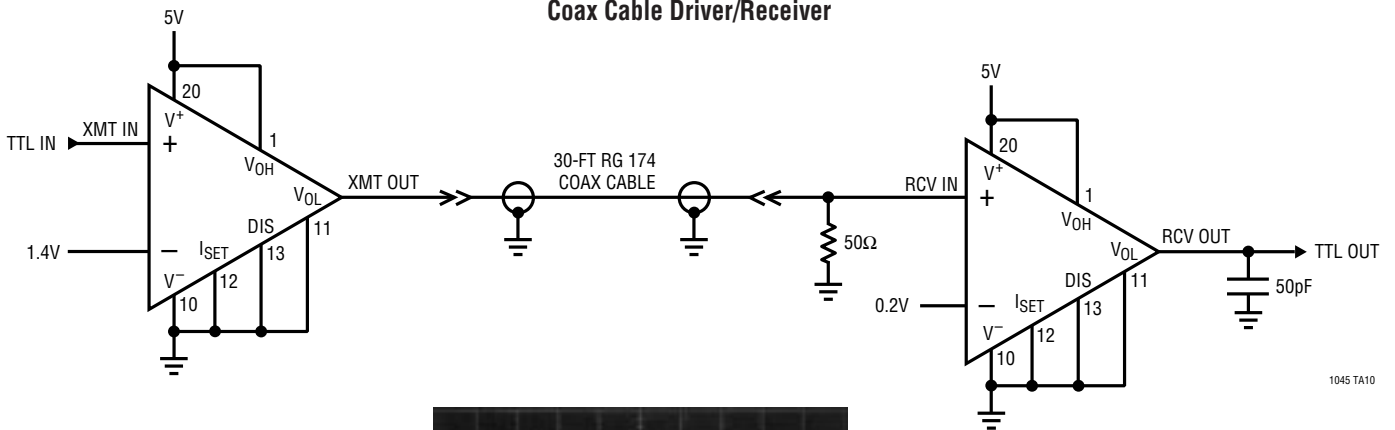
1045 TA07

# TYPICAL APPLICATIONS

Logic Ground Isolation when Two Grounds are within LTC1045 Common Mode Range

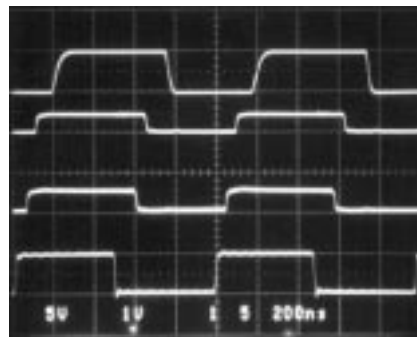


Coax Cable Driver/Receiver



1045 TA10

RCV OUT (5V/DIV)  
 RCV IN (1V/DIV)  
 XMT OUT (1V/DIV)  
 XMT IN (5V/DIV)

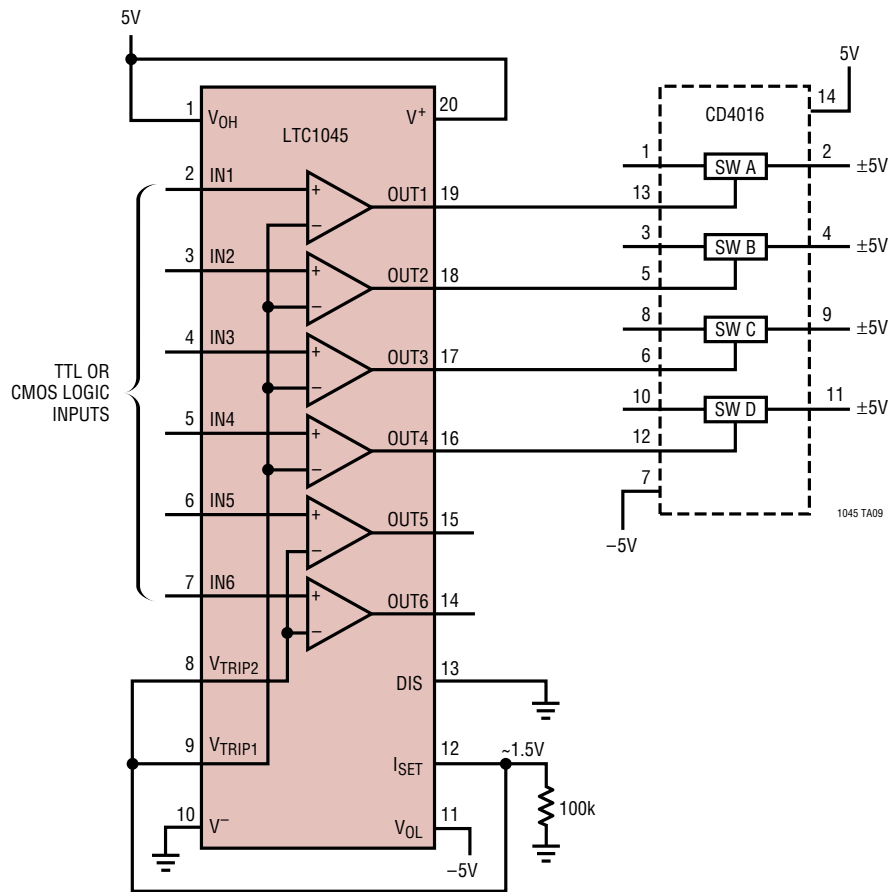


200ns/DIV

1045 TA10a

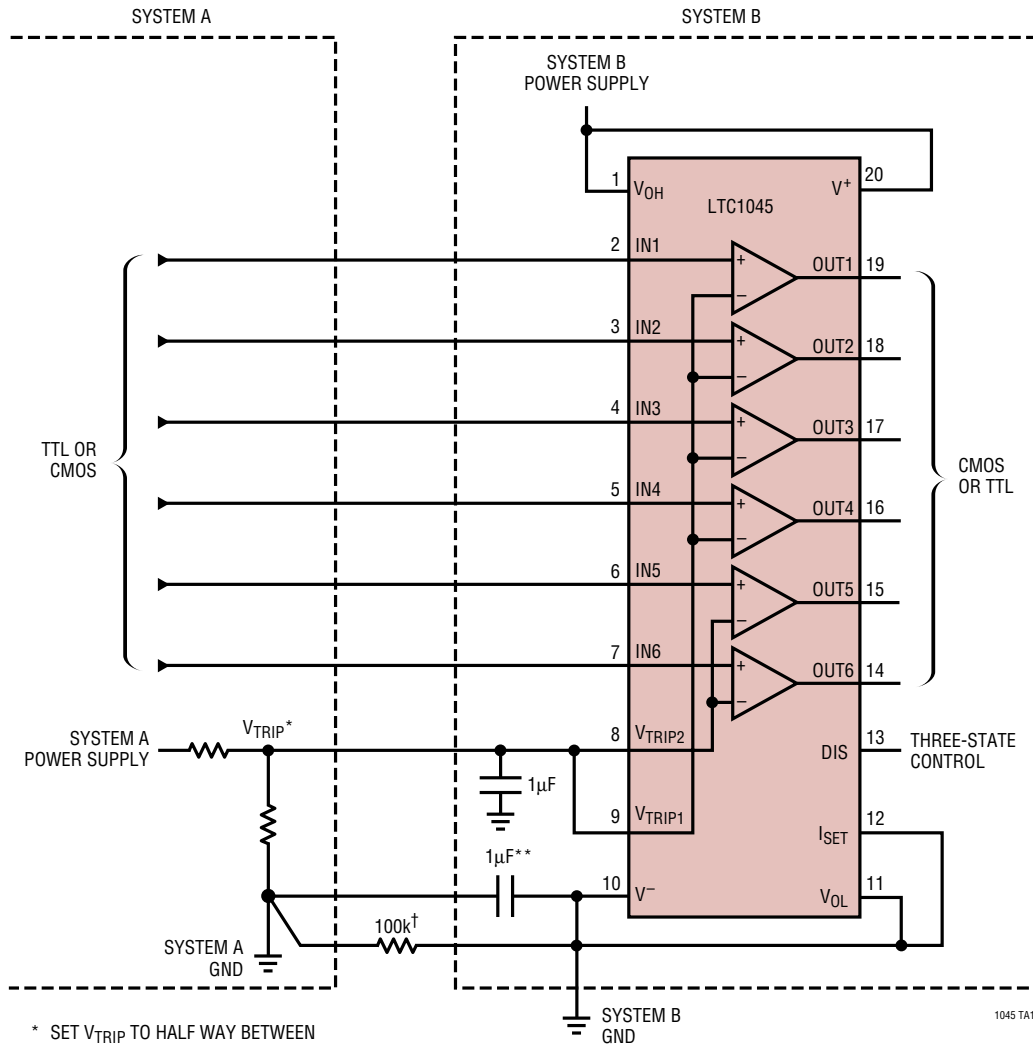
TYPICAL APPLICATIONS

±5V Analog Switch Driver



TYPICAL APPLICATIONS

Logic Systems DC Isolation

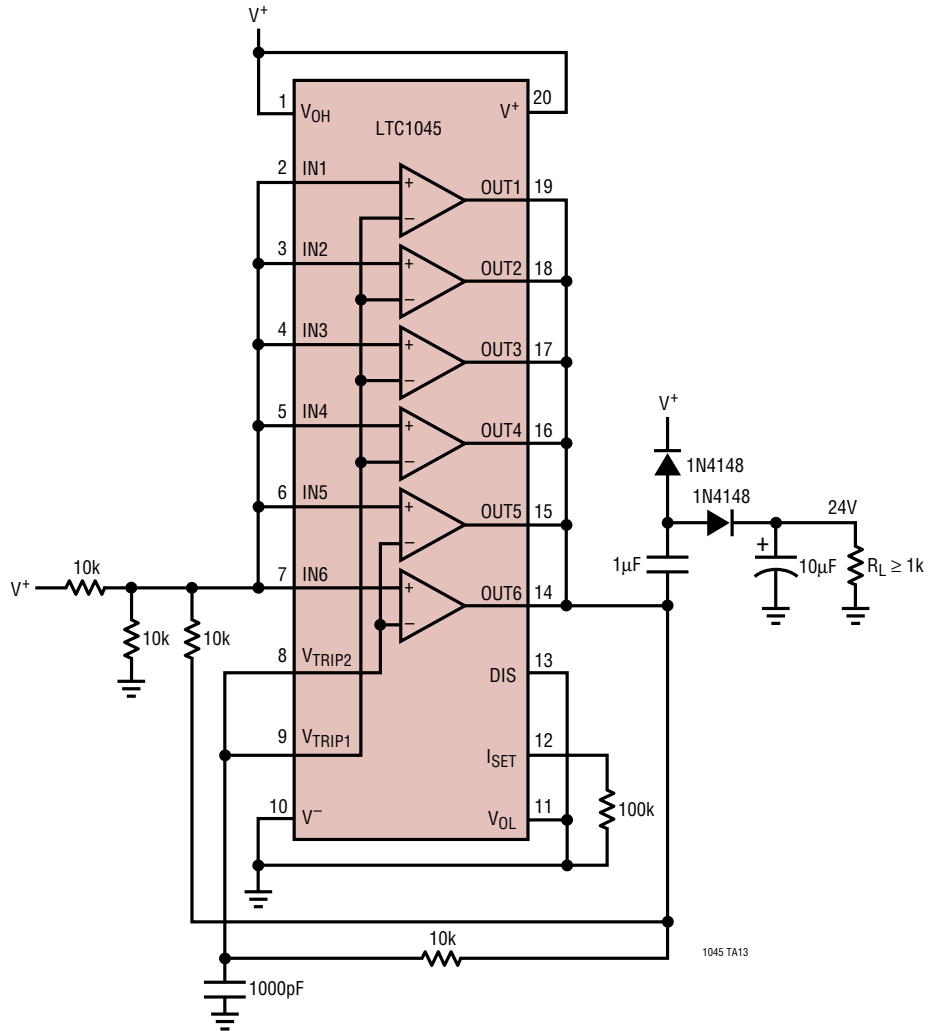


- \* SET  $V_{TRIP}$  TO HALF WAY BETWEEN  $V_{OH}$  AND  $V_{OL}$  OF SYSTEM A
- \*\* SHUNTS COMMON MODE SIGNAL
- † PROVIDES LEAKAGE PATH FOR TOTALLY ISOLATED SYSTEMS

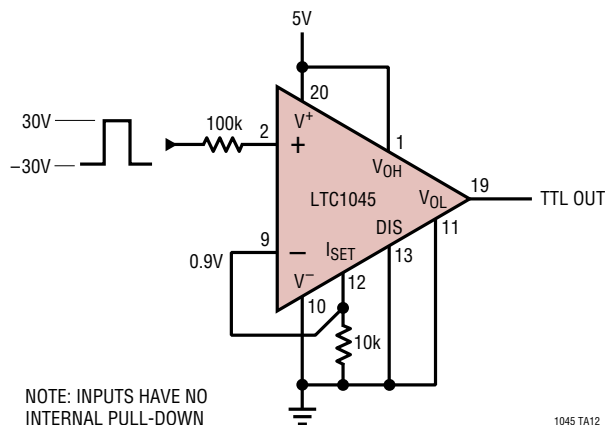
1045 TA11

# TYPICAL APPLICATIONS

24V Relay Supply from 12V/15V Supply

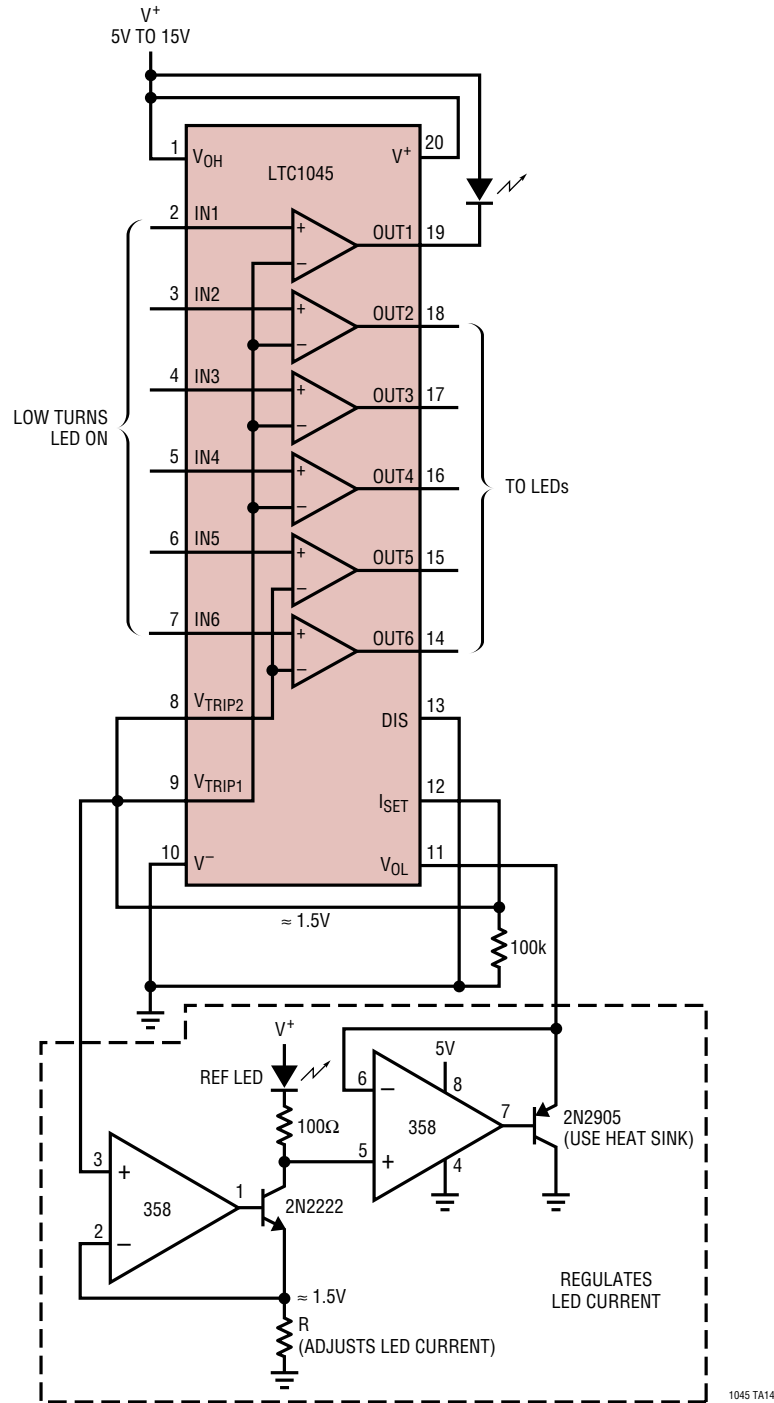


RS232 Receiver



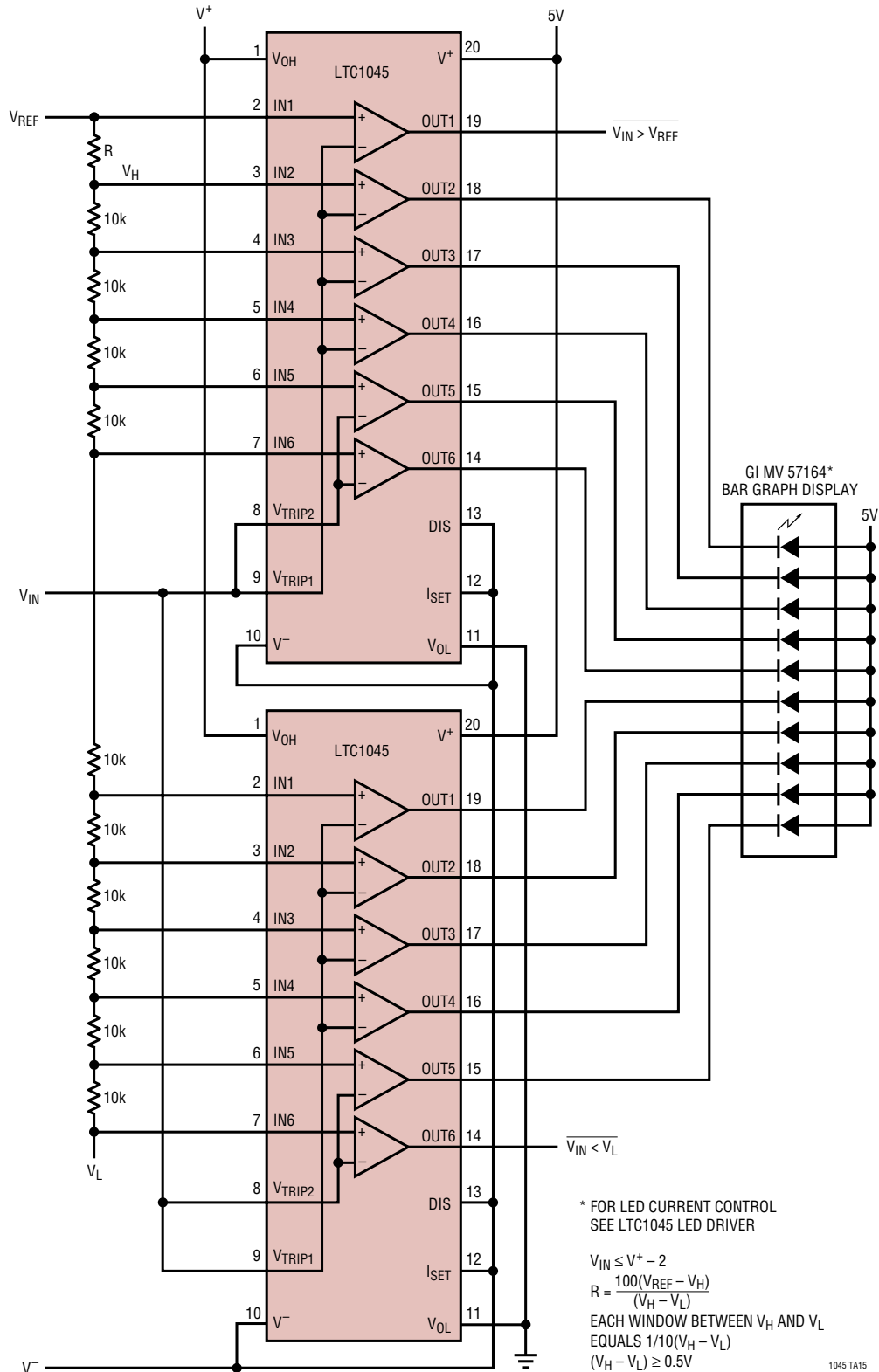
TYPICAL APPLICATIONS

LED Driver



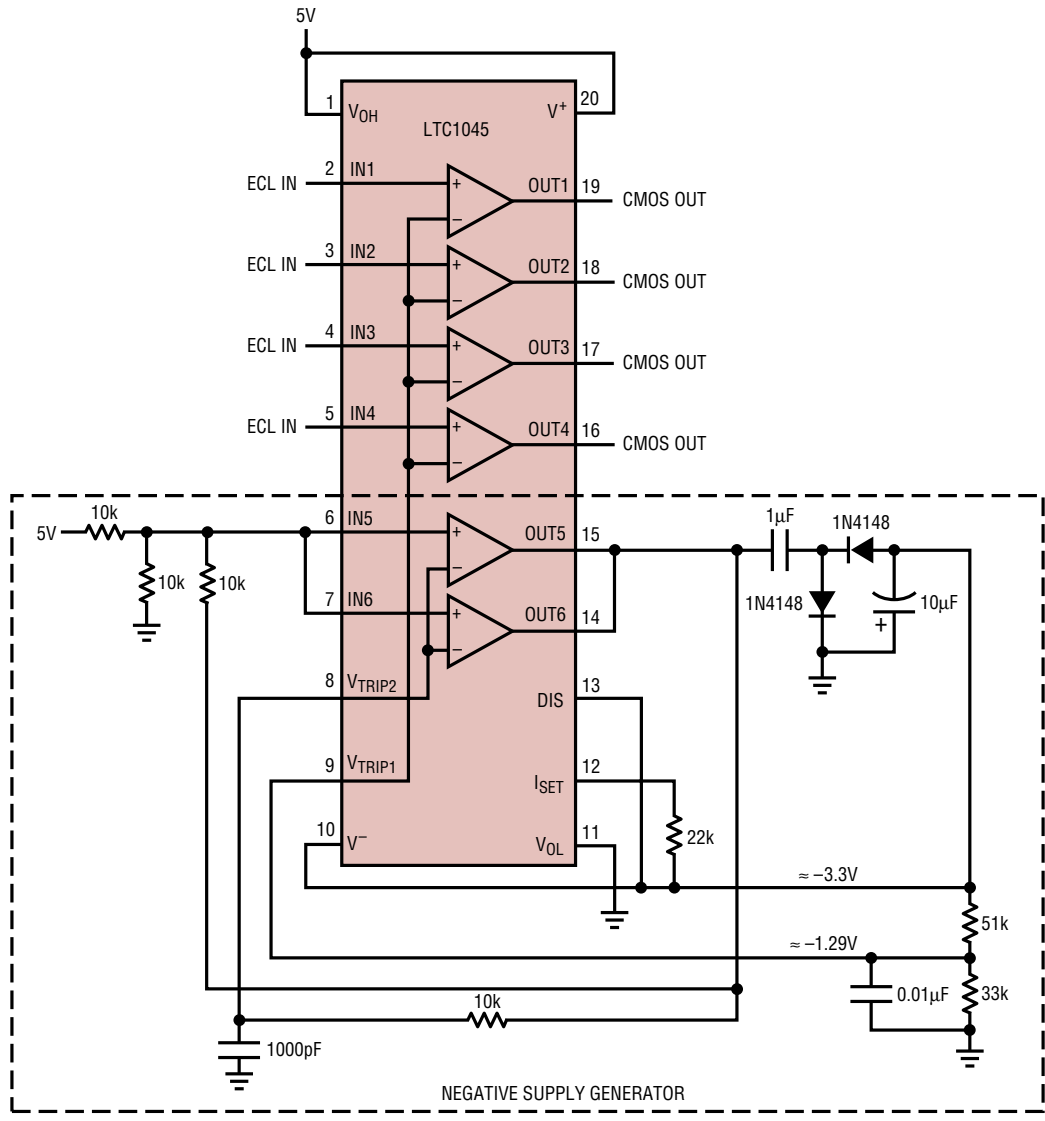
# TYPICAL APPLICATIONS

## Multiwindow Comparator and Display



TYPICAL APPLICATIONS

ECL to CMOS from Single 5V Supply

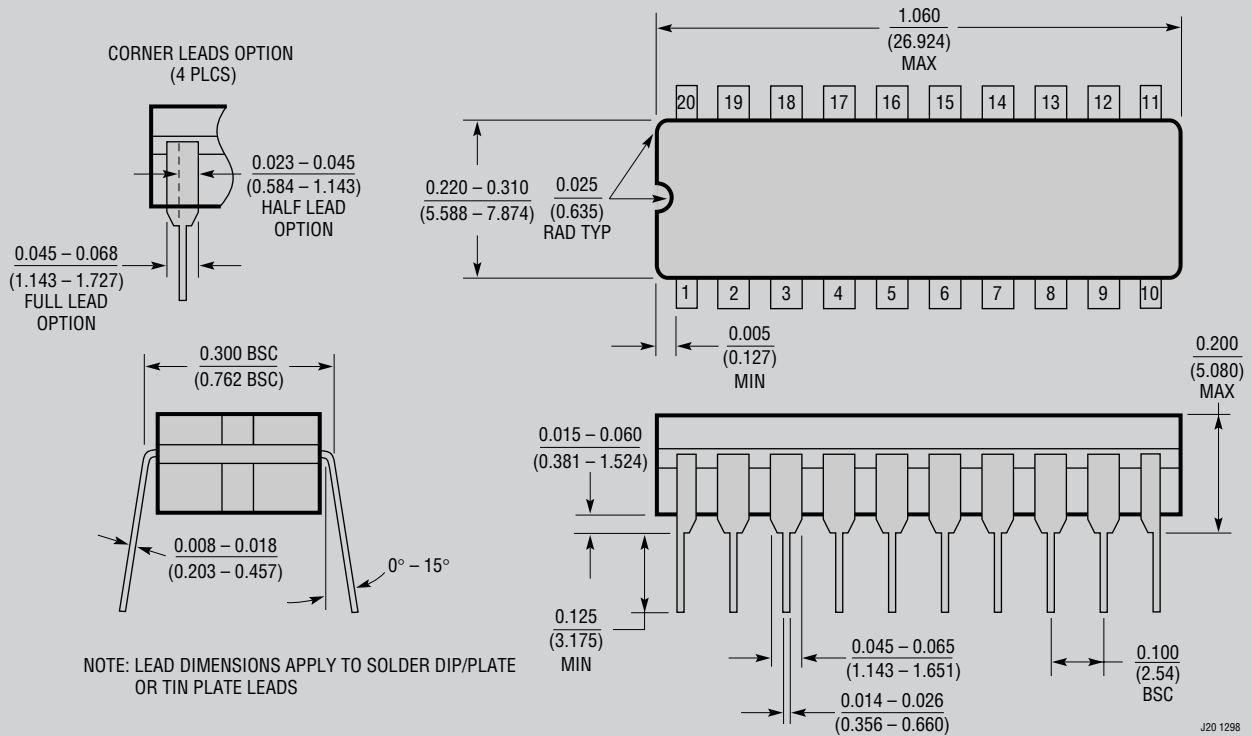


1045 TA16



**PACKAGE DESCRIPTION**

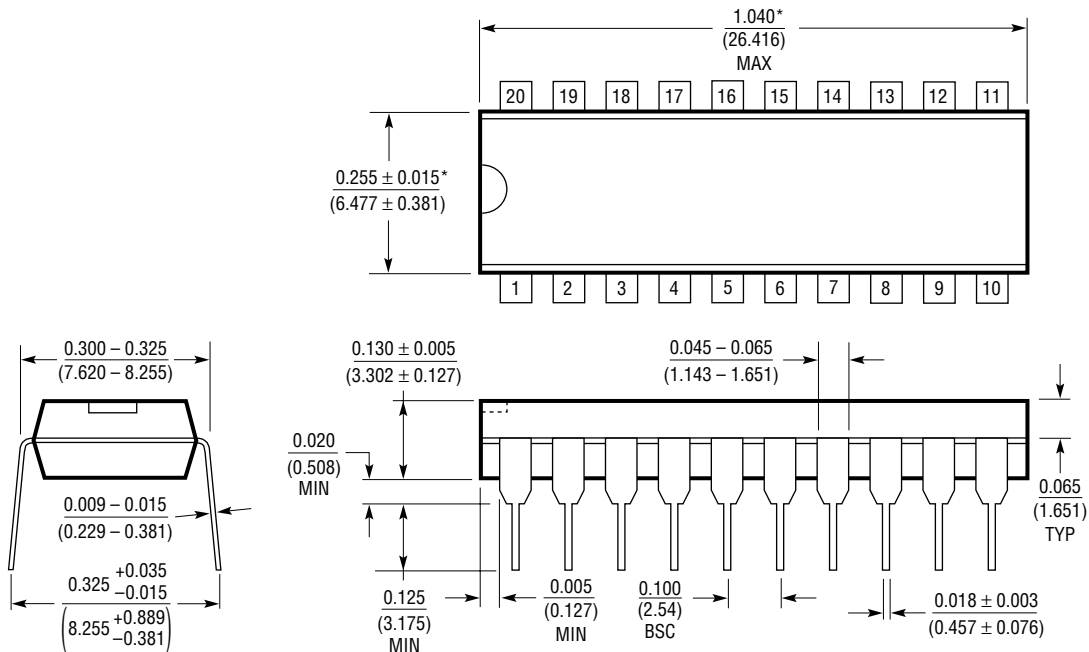
**J Package**  
**20-Lead CERDIP (Narrow .300 Inch, Hermetic)**  
 (Reference LTC DWG # 05-08-1110)



**OBSOLETE PACKAGE**

**PACKAGE DESCRIPTION**

**N Package**  
**20-Lead PDIP (Narrow .300 Inch)**  
 (Reference LTC DWG # 05-08-1510)

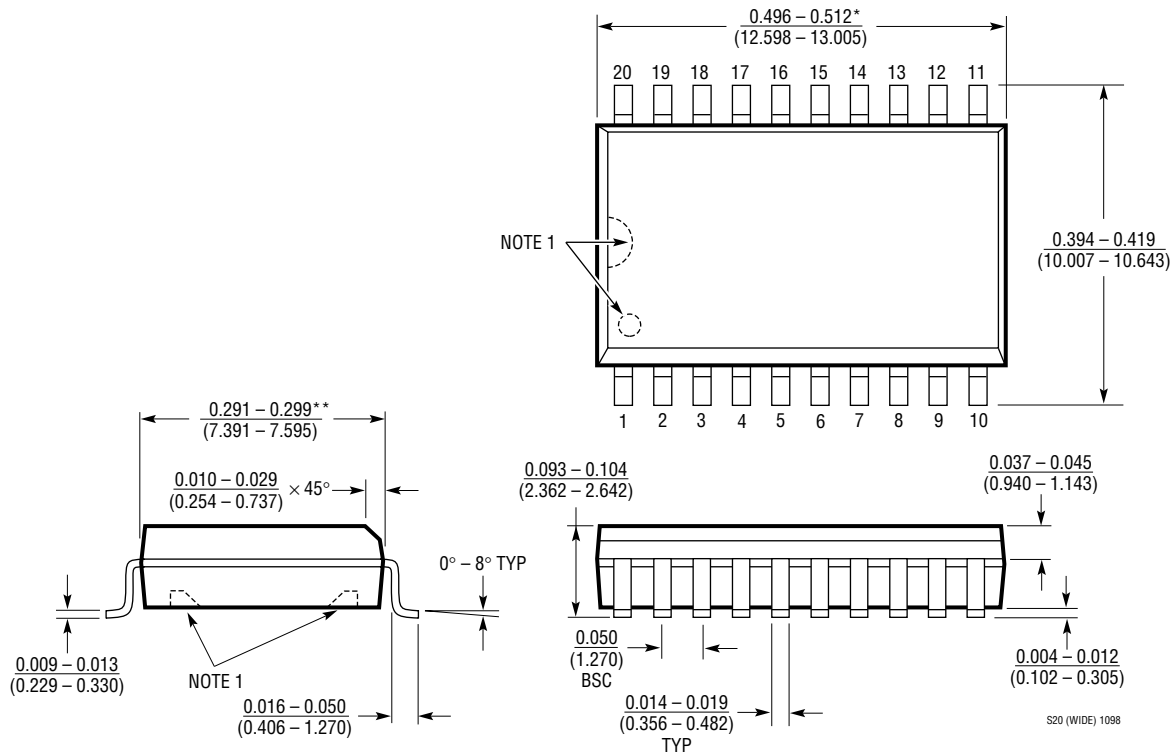


\*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.  
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N20 1098

**PACKAGE DESCRIPTION**

**SW Package**  
**20-Lead Plastic Small Outline (Wide .300 Inch)**  
 (Reference LTC DWG # 05-08-1620)



NOTE:  
 1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.  
 THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS  
 \*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

