Low Power, Linear Phase 8th Order Lowpass Filter

FEATURES

- Better Than Bessel Roll-Off
- f_{CUTOFF} up to 20kHz, Single 5V Supply
- I_{SUPPLY} = 2.5mA (Typ), Single 5V Supply
- 75dB THD + Noise with Single 5V Supply
- Phase and Group Delay Response Fully Tested
- Transient Response with No Ringing
- Wide Dynamic Range
- No External Components Needed

APPLICATIONS

- Data Communication Filters
- Time Delay Networks
- Phase Matched Filters

DESCRIPTION

The LTC1164-7 is a low power, clock-tunable monolithic 8th order lowpass filter with linear passband phase and flat group delay. The amplitude response approximates a maximally flat passband and exhibits steeper roll-off than an equivalent 8th order Bessel filter. For instance, at twice the cutoff frequency the filter attains 34dB attenuation (vs12dB for Bessel), while at three times the cutoff frequency the filter attains 68dB attenuation (vs 30dB for Bessel). The cutoff frequency of the LTC1164-7 is tuned via an external TTL or CMOS clock.

Low power is achieved without sacrificing dynamic range. With single 5V supply, the S/N + THD is up to 75dB. Optimum 91dB S/N is obtained with ±7.5V supplies.

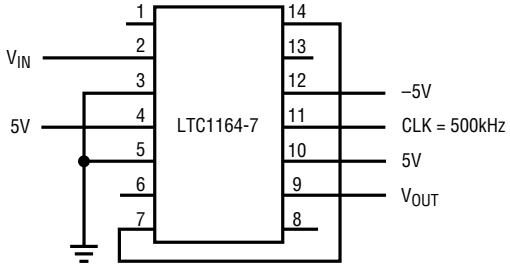
The clock-to-cutoff frequency ratio of the LTC1164-7 can be set to 50:1 (pin 10 to V^+) or 100:1 (pin 10 to V^-).

When the filter operates at the clock-to-cutoff frequency ratio of 50:1, the input is double-sampled to lower the risk of aliasing.

The LTC1164-7 is pin-compatible with the LTC1064-X series and LTC1264-7.

TYPICAL APPLICATION

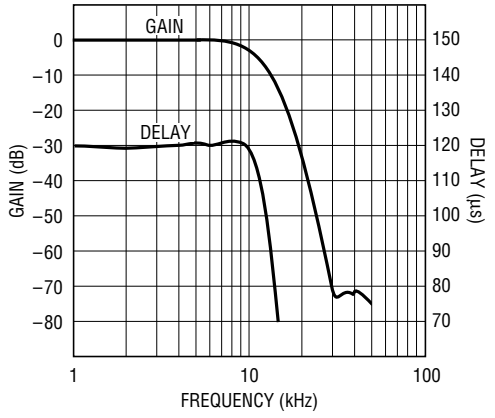
10kHz Linear Phase Lowpass Filter



NOTE: THE POWER SUPPLIES SHOULD BE BYPASSED BY A 0.1µF CAPACITOR CLOSE TO THE PACKAGE AND ANY PRINTED CIRCUIT BOARD ASSEMBLY SHOULD MAINTAIN A DISTANCE OF AT LEAST 0.2 INCHES BETWEEN ANY OUTPUT OR INPUT PIN AND THE f_{CLK} LINE.

1164-7 TA01

Frequency Response



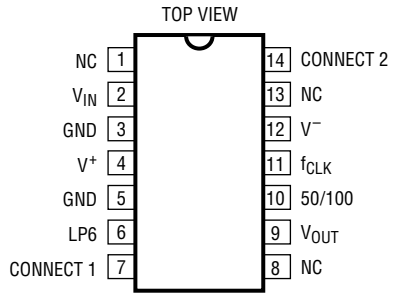
1164-7 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16V
Power Dissipation 400mW
Burn-In Voltage 16V
Voltage at Any Input ..... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Storage Temperature Range ..... –65°C to 150°C

Operating Temperature Range
LTC1164-7C ..... –40°C to 85°C
LTC1164-7M ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



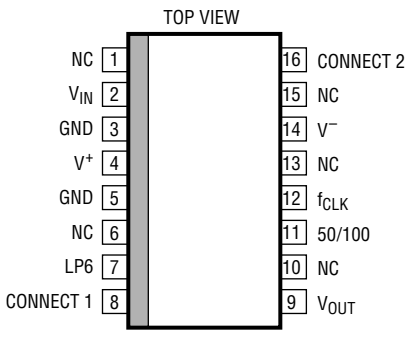
J PACKAGE
14-LEAD CERAMIC DIP

N PACKAGE
14-LEAD PLASTIC DIP

T_{JMAX} = 150°C, θ_{JA} = 65°C/W (J)
T_{JMAX} = 110°C, θ_{JA} = 65°C/W (N)

ORDER PART NUMBER

LTC1164-7CN
LTC1164-7CJ
LTC1164-7MJ



S PACKAGE
16-LEAD PLASTIC SOL

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1164-7CS

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 8kHz or 4kHz, f_{CLK} = 400kHz, TTL or CMOS level and all gain measurements are referenced to passband gain, unless otherwise specified. (Maximum clock rise or fall time ≤ 1μs)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Gain	0.1Hz ≤ f ≤ 0.25 f_{CUTOFF}					
	f_{TEST} = 2kHz, (f_{CLK}/f_C) = 50:1 (Note 4)	●	–0.50	–0.10	0.30	dB
Gain at 0.50 f_{CUTOFF} (Note 3)	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1	●	–0.50	–0.20	0.30	dB
	f_{TEST} = 2kHz, (f_{CLK}/f_C) = 100:1	●	–0.85	–0.65	0.15	dB
Gain at 0.75 f_{CUTOFF}	f_{TEST} = 6kHz, (f_{CLK}/f_C) = 50:1	●	–1.2	–1.1	0.1	dB
Gain at f_{CUTOFF}	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1	●	–4.1	–3.4	–1.9	dB
	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 100:1	●	–5.5	–5.2	–2.5	dB
Gain at 2.0 f_{CUTOFF}	f_{TEST} = 16kHz, (f_{CLK}/f_C) = 50:1	●	–37	–34	–30	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 100:1	●	–38	–34	–30	dB
Gain with f_{CLK} = 20kHz	f_{TEST} = 200Hz, (f_{CLK}/f_C) = 100:1		–5.7	–5.2	–2.5	dB
Gain with f_{CLK} = 400kHz, V_S = ±2.375V	f_{TEST} = 4kHz, (f_{CLK}/f_C) = 50:1		–0.50	–0.2	0.2	dB
	f_{TEST} = 8kHz, (f_{CLK}/f_C) = 50:1		–3.75	–3.4	–2.5	dB
Phase Factor (F)	0.1Hz ≤ f ≤ f_{CUTOFF}					
Phase = 180° – F (f/f_C)	(f_{CLK}/f_C) = 50:1			435 ± 2		Deg
(Note 1)	(f_{CLK}/f_C) = 100:1			428 ± 2		Deg
	(f_{CLK}/f_C) = 50:1	●	430		442	Deg
	(f_{CLK}/f_C) = 100:1	●	423		434	Deg
Phase Nonlinearity	(f_{CLK}/f_C) = 50:1			±1.0		%
(Note 1)	(f_{CLK}/f_C) = 100:1			±1.0		%
	(f_{CLK}/f_C) = 50:1	●			±2.0	%
	(f_{CLK}/f_C) = 100:1	●			±2.5	%

ELECTRICAL CHARACTERISTICS

V_S = ±7.5V, R_L = 10k, T_A = 25°C, f_{CUTOFF} = 8kHz or 4kHz, f_{CLK} = 400kHz, TTL or CMOS level and all gain measurements are referenced to passband gain, unless otherwise specified. (Maximum clock rise or fall time ≤ 1µs)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Group Delay (t_d) $t_d = (1/360)(f/f_C)$ (Note 2)	(f_{CLK}/f_C) = 50:1, f ≥ f_{CUTOFF}			151.0 ± 1		µs
	(f_{CLK}/f_C) = 100:1, f ≥ f_{CUTOFF}			297.2 ± 1		µs
	(f_{CLK}/f_C) = 50:1, f ≥ f_{CUTOFF}	●	149.3		153.5	µs
	(f_{CLK}/f_C) = 100:1, f ≥ f_{CUTOFF}	●	293.8		301.4	µs
Group Delay Deviation (Note 2)	(f_{CLK}/f_C) = 50:1, f ≥ f_{CUTOFF}			±1.0		%
	(f_{CLK}/f_C) = 100:1, f ≥ f_{CUTOFF}			±1.0		%
	(f_{CLK}/f_C) = 50:1, f ≥ f_{CUTOFF}	●			±2.0	%
	(f_{CLK}/f_C) = 100:1, f ≥ f_{CUTOFF}	●			±2.5	%
Input Frequency Range (Table 9)	(f_{CLK}/f_C) = 50:1			< f_{CLK}		kHz
	(f_{CLK}/f_C) = 100:1			< f_{CLK}/2		kHz
Maximum f_{CLK}	V_S = Single 5V (Pins 3 and 5 at 2V)			1		MHz
	V_S = ±5V			1		MHz
	V_S = ±7.5V			1		MHz
Clock Feedthrough (f = f_{CLK})	50:1, ±5V, Input at GND			100		μV_{RMS}
Wideband Noise (1Hz ≤ f < f_{CLK})	V_S = ±2.5V			95 ± 5%		μV_{RMS}
	V_S = ±5V			105 ± 5%		μV_{RMS}
	V_S = ±7.5V			115 ± 5%		μV_{RMS}
Input Impedance			35	55	90	kΩ
Output DC Voltage Swing (Note 4)	V_S = ±2.375V		±1.25	±1.4		V
	V_S = ±5V	●	±3.70	±3.9		V
	V_S = ±7.5V	●	±5.40	±6.1		V
Output DC Offset	50:1, V_S = ±5V			±100	±220	mV
	100:1, V_S = ±5V			±100		mV
Output DC Offset TempCo	50:1, V_S = ±5V			±200		µV/°C
	100:1, V_S = ±5V			±200		µV/°C
Power Supply Current	V_S = ±2.375V, T_A = 25°C			2.5	4.0	mA
		●			4.5	mA
	V_S = ±5V, T_A = 25°C			4.5	7.0	mA
		●			8.0	mA
	V_S = ±7.5V, T_A = 25°C			7.0	11.0	mA
		●			12.5	mA
Power Supply Range			±2.375		±8	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Input frequencies, f, are linearly phase shifted through the filter as long as f ≤ f_C; f_C = cutoff frequency.

Figure 1 curve shows the typical phase response of an LTC1164-7 operating at f_{CLK} = 400kHz, f_C = 8kHz and it closely matches an ideal straight line. The phase shift is described by: phase shift = 180° – F (f/f_C); f ≤ f_C.

F is arbitrarily called the "phase factor" expressed in degrees. The phase factor together with the specified deviation from the ideal straight line allows the calculation of the phase at a given frequency. Example: The phase shift at 7kHz of the LTC1164-7 shown in Figure 1 is: phase shift = 180° – 434° (7kHz/10kHz) ± nonlinearity = –123.8° ± 1% or –123.9° ± 1.24°.

Note 2: Group delay and group delay deviation are calculated from the measured phase factor and phase deviation specifications.

Note 3: The filter cutoff frequency is abbreviated as f_{CUTOFF} or f_C.

Note 4: The AC swing is typically $11V_{P-P}$, $7V_{P-P}$, $2.8V_{P-P}$ for ±7.5V, ±5V, ±2.5V supply respectively. For more information refer to the THD + Noise vs Input graphs.

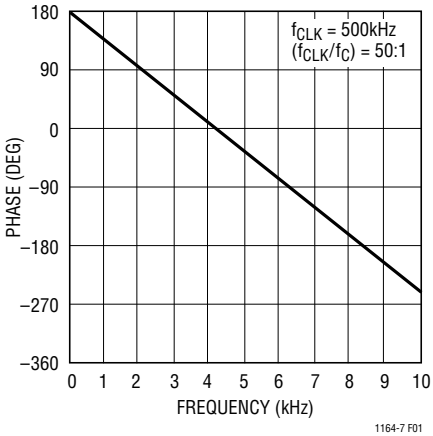
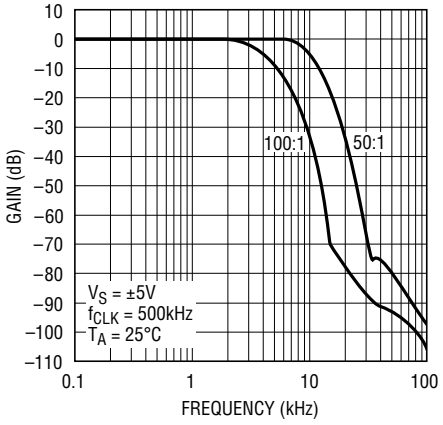


Figure 1. Phase Response in the Passband (Note 1)

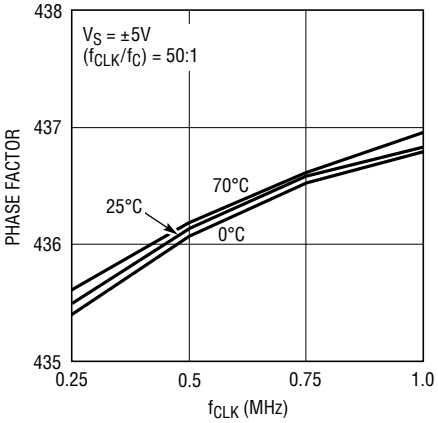
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



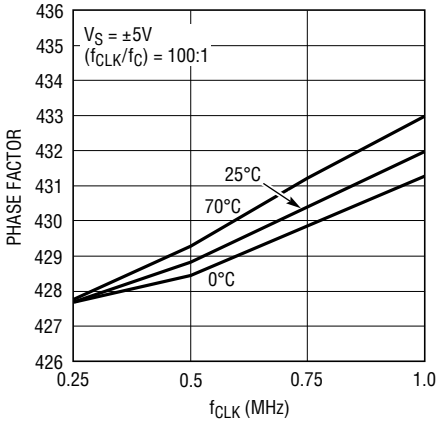
1264-7 G01

Phase Factor vs f_{CLK} (Typical Unit)



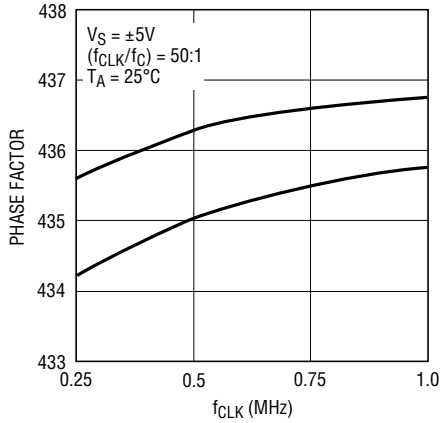
1164-7 G02

Phase Factor vs f_{CLK} (Typical Unit)



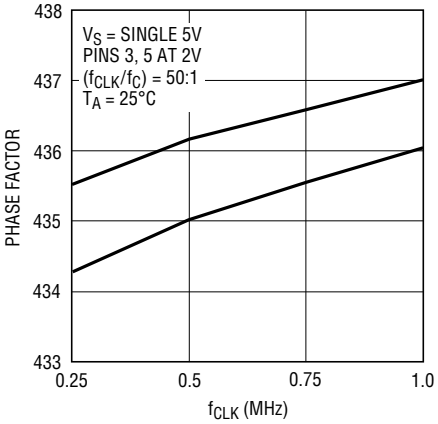
1164-7 G03

Phase Factor vs f_{CLK} (Min and Max Representative Units)



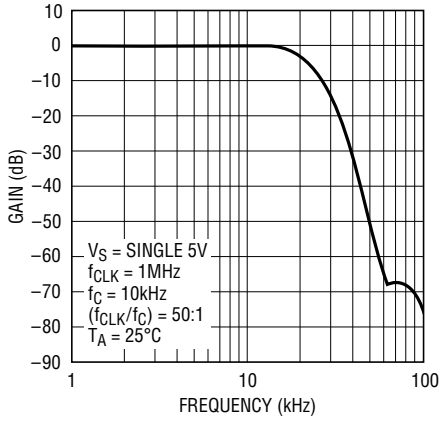
1164-7 G04

Phase Factor vs f_{CLK} (Min and Max Representative Units)



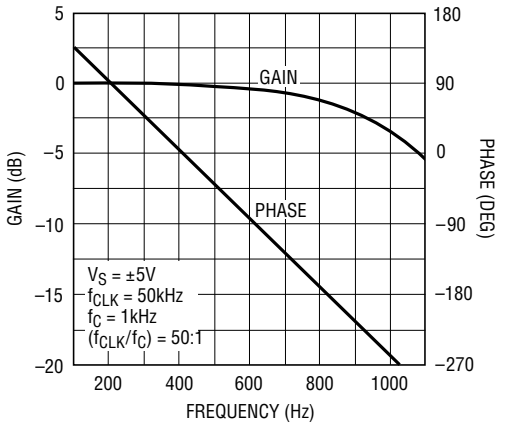
1164-7 G05

Gain vs Frequency



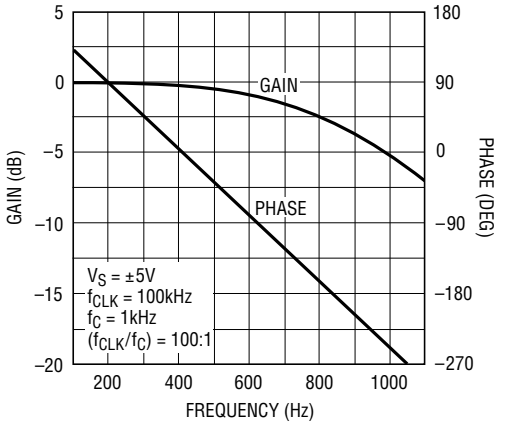
1164-7 G06

Passband Gain and Phase



1164-7 G07

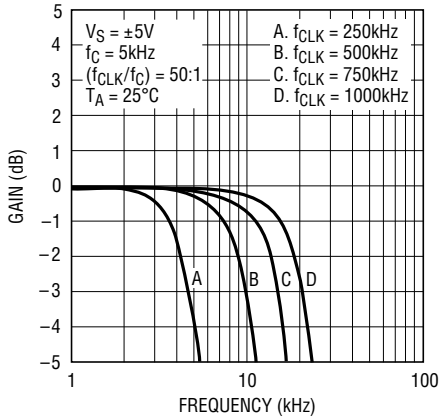
Passband Gain and Phase



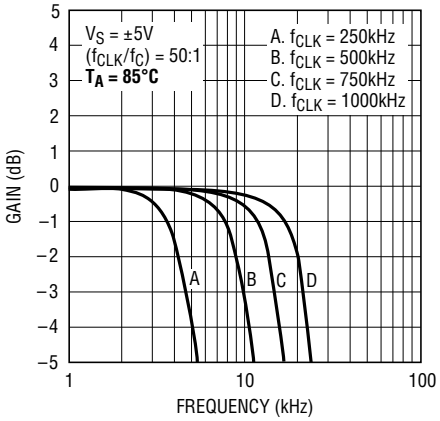
1164-7 G08

TYPICAL PERFORMANCE CHARACTERISTICS

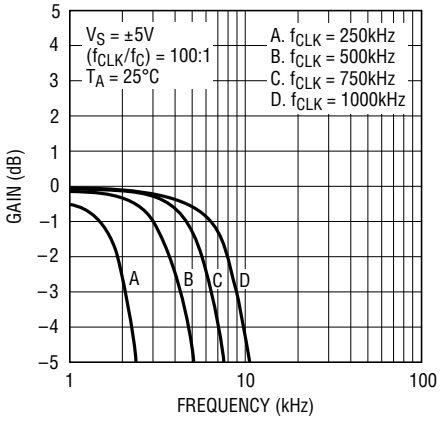
Passband Gain vs Frequency and f_{CLK}



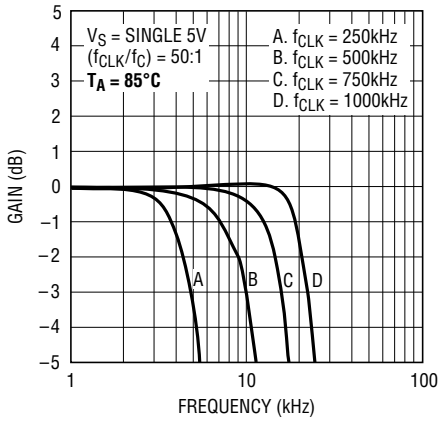
Passband Gain vs Frequency and f_{CLK}



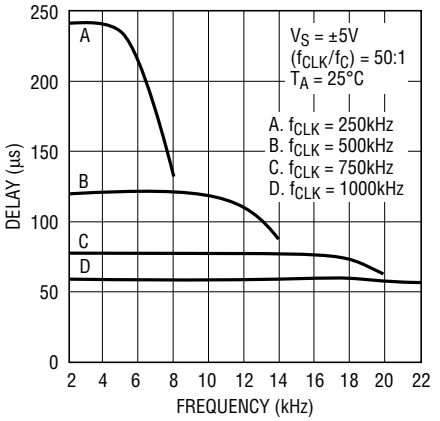
Passband Gain vs Frequency and f_{CLK}



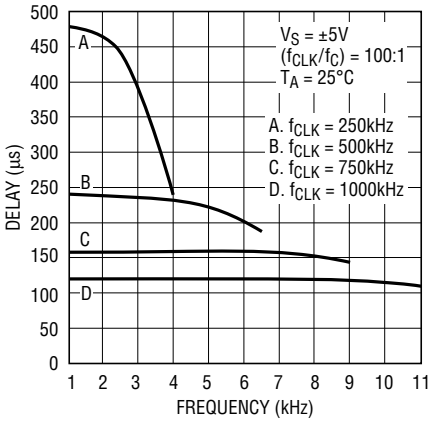
Passband Gain vs Frequency and f_{CLK}



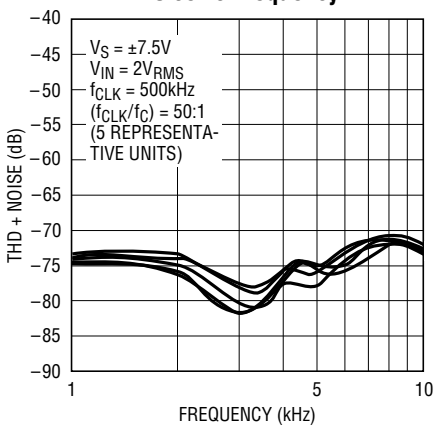
Delay vs Frequency and f_{CLK}



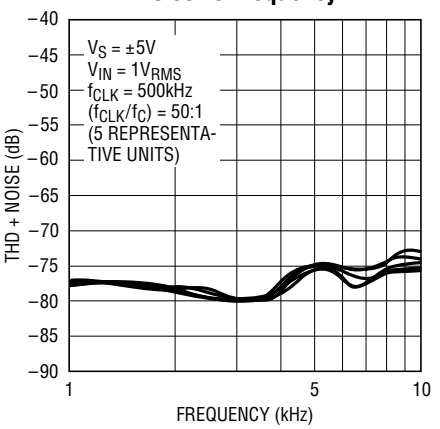
Delay vs Frequency and f_{CLK}



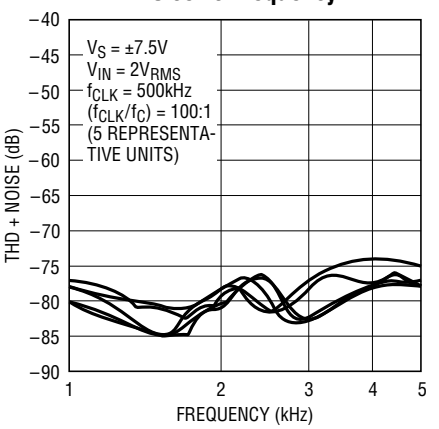
THD + Noise vs Frequency



THD + Noise vs Frequency

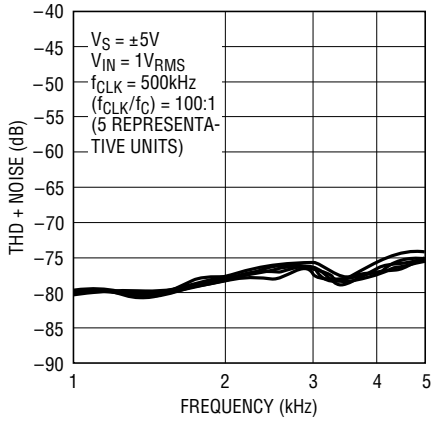


THD + Noise vs Frequency

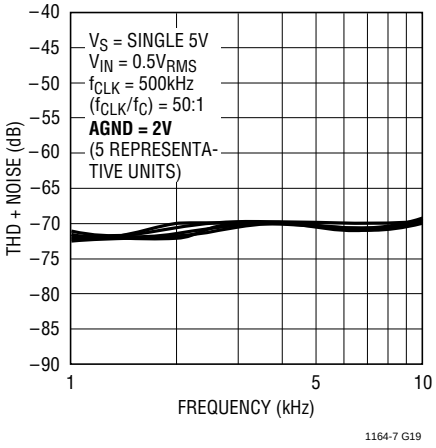


TYPICAL PERFORMANCE CHARACTERISTICS

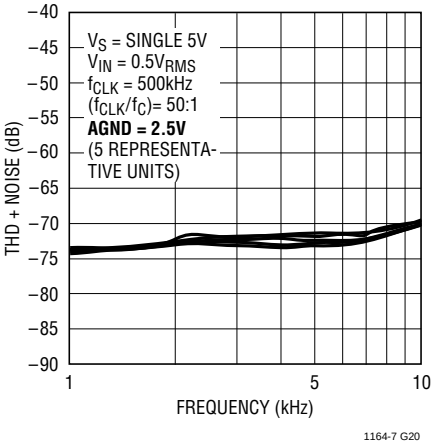
THD + Noise vs Frequency



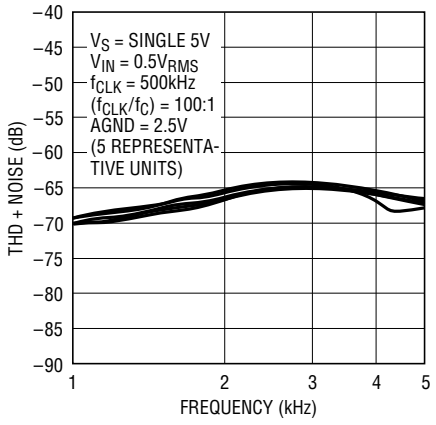
THD + Noise vs Frequency



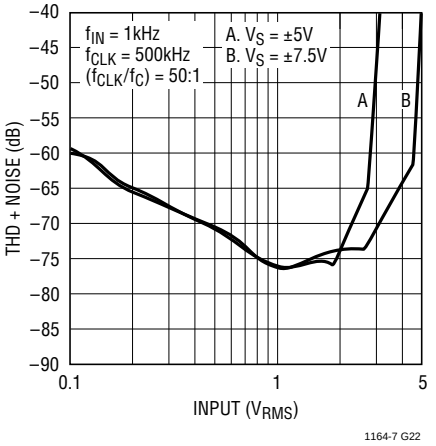
THD + Noise vs Frequency



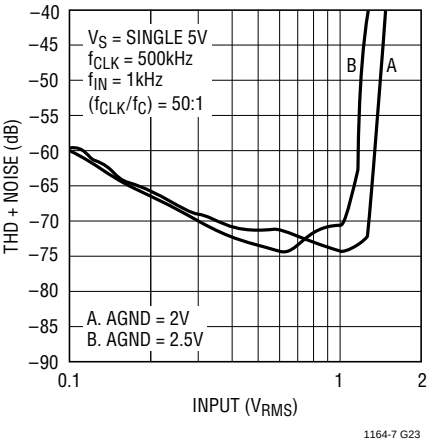
THD + Noise vs Frequency



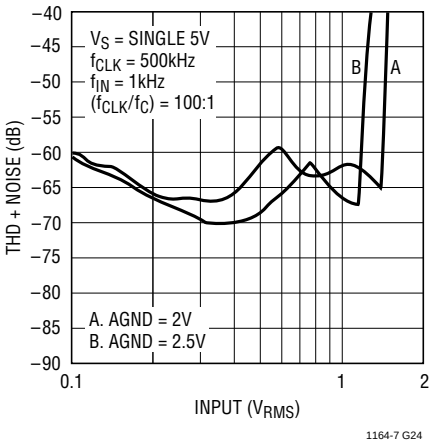
THD + Noise vs Input



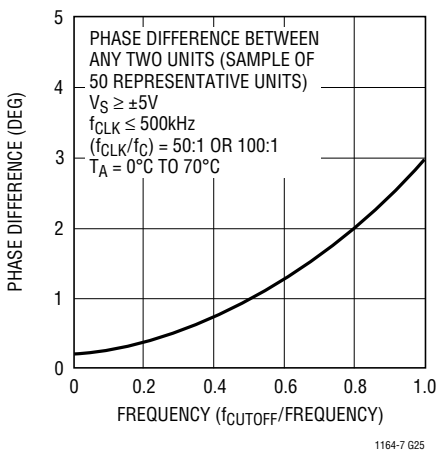
THD + Noise vs Input



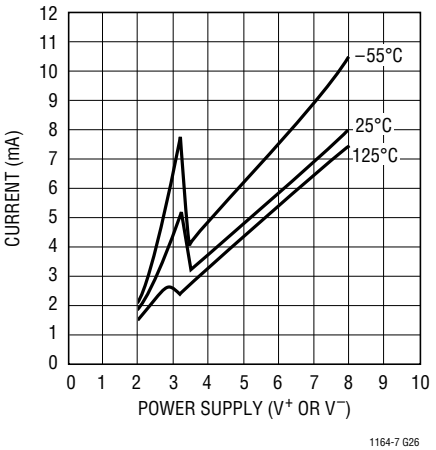
THD + Noise vs Input



Phase Matching vs Frequency



Power Supply Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

Table 1. Passband Gain and Phase
V_S = ±7.5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.085	180.00
1.250	–0.085	71.51
2.500	–0.261	–37.31
3.750	–1.092	–146.38
5.000	–3.647	–255.45
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.091	180.00
2.500	–0.091	71.36
5.000	–0.251	–37.57
7.500	–1.028	–146.78
10.000	–3.488	–256.16
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.106	180.00
3.750	–0.106	71.26
7.500	–0.264	–37.65
11.250	–0.943	–146.88
15.000	–3.206	–256.58
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.131	180.00
5.000	–0.131	71.11
10.000	–0.291	–37.71
15.000	–0.853	–146.87
20.000	–2.864	–256.81

Table 2. Passband Gain and Phase
V_S = ±7.5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.201	180.00
0.625	–0.201	71.39
1.250	–0.727	–36.79
1.875	–2.075	–143.66
2.500	–5.205	–247.79
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.176	180.00
1.250	–0.176	71.34
2.500	–0.645	–36.88
3.750	–1.945	–143.93
5.000	–5.032	–248.52
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.161	180.00
1.875	–0.161	71.32
3.750	–0.574	–37.04
5.625	–1.789	–144.45
7.500	–4.779	–249.82
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.157	180.00
2.500	–0.157	71.23
5.000	–0.538	–37.28
7.500	–1.666	–145.02
10.000	–4.527	–251.13

Table 3. Passband Gain and Phase
V_S = ±5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.071	180.00
1.250	–0.071	71.48
2.500	–0.243	–37.29
3.750	–1.068	–146.34
5.000	–3.609	–255.40
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.081	180.00
2.500	–0.081	71.35
5.000	–0.236	–37.52
7.500	–0.981	–146.71
10.000	–3.371	–256.13
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.105	180.00
3.750	–0.105	71.26
7.500	–0.261	–37.62
11.250	–0.883	–146.80
15.000	–3.008	–256.57
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.134	180.00
5.000	–0.134	70.99
10.000	–0.292	–37.75
15.000	–0.771	–146.83
20.000	–2.571	–256.88

Table 4. Passband Gain and Phase
V_S = ±5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.189	180.00
0.625	–0.189	71.39
1.250	–0.707	–36.75
1.875	–2.048	–143.60
2.500	–5.711	–247.74
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.159	180.00
1.250	–0.159	71.35
2.500	–0.603	–36.85
3.750	–1.872	–144.00
5.000	–4.926	–248.80
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.149	180.00
1.875	–0.149	71.28
3.750	–0.536	–37.13
5.625	–1.704	–144.72
7.500	–4.621	–250.48
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.151	180.00
2.500	–0.151	71.10
5.000	–0.511	–37.52
7.500	–1.581	–145.45
10.000	–4.336	–252.01

TYPICAL PERFORMANCE CHARACTERISTICS

Table 5. Passband Gain and Phase
V_S = Single 5V, Ratio = 50:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.085	180.00
1.250	–0.085	71.54
2.500	–0.252	–37.15
3.750	–1.056	–146.12
5.000	–3.562	–255.22
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.101	180.00
2.500	–0.101	71.39
5.000	–0.251	–37.38
7.500	–0.947	–146.44
10.000	–3.252	–256.02
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.133	180.00
3.750	–0.133	71.16
7.500	–0.291	–37.56
11.250	–0.826	–146.55
15.000	–2.789	–256.52
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.162	180.00
5.000	–0.162	70.89
10.000	–0.307	–37.78
15.000	–0.647	–146.67
20.000	–2.201	–257.06

Table 6. Passband Gain and Phase
V_S = Single 5V, Ratio = 100:1, T_A = 25°C

FREQUENCY (kHz)	GAIN (dB)	PHASE (DEG)
f_{CLK} = 250kHz (Typical Unit)		
0.000	–0.283	180.00
0.625	–0.283	71.35
1.250	–0.799	–37.01
1.875	–2.143	–143.96
2.500	–5.271	–248.03
f_{CLK} = 500kHz (Typical Unit)		
0.000	–0.252	180.00
1.250	–0.252	71.28
2.500	–0.676	–37.16
3.750	–1.917	–144.46
5.000	–4.936	–249.40
f_{CLK} = 750kHz (Typical Unit)		
0.000	–0.231	180.00
1.875	–0.231	70.94
3.750	–0.603	–37.72
5.625	–1.704	–145.55
7.500	–4.535	–251.81
f_{CLK} = 1MHz (Typical Unit)		
0.000	–0.212	180.00
2.500	–0.212	70.83
5.000	–0.532	–38.11
7.500	–1.497	–146.47
10.000	–4.115	–253.92

PIN FUNCTIONS

Power Supply Pins (4, 12)

The V^+ (pin 4) and the V^- (pin 12) should each be bypassed with a 0.1μF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply during power-up should have a slew rate less than 1V/μs. When V^+ is applied before V^- and V^- is allowed to go above ground, a signal diode should clamp V^- to prevent latch-up. Figures 2 and 3 show typical connections for dual and single supply operation.

Clock Input Pin (11)

Any TTL or CMOS clock source with a square-wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to clock's ground at a single point only. Table 7 shows the clock's low and high level threshold values for dual or single supply operation. A pulse generator can be used as a clock source provided the high level ON time is greater than 0.5μs. Sine waves are not recommended for clock input frequencies less than 100kHz, since excessively slow clock rise or fall times generate internal clock jitter (maximum clock rise or fall time ≤ 1μs). The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path. A 1k resistor between clock source and pin 11 will slow down the rise and fall times of the clock to further reduce charge coupling (Figures 2 and 3).

PIN FUNCTIONS

Table 7. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Dual Supply = ±7.5V	≥ 2.18V	≤ 0.5V
Dual Supply = ±5V	≥ 1.45V	≤ 0.5V
Dual Supply = ±2.5V	≥ 0.73V	≤ –2.0V
Single Supply = 12V	≥ 7.80V	≤ 6.5V
Single Supply = 5V	≥ 1.45V	≤ 0.5V

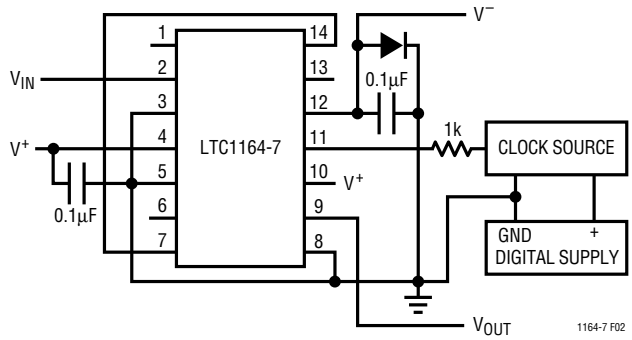


Figure 2. Dual Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

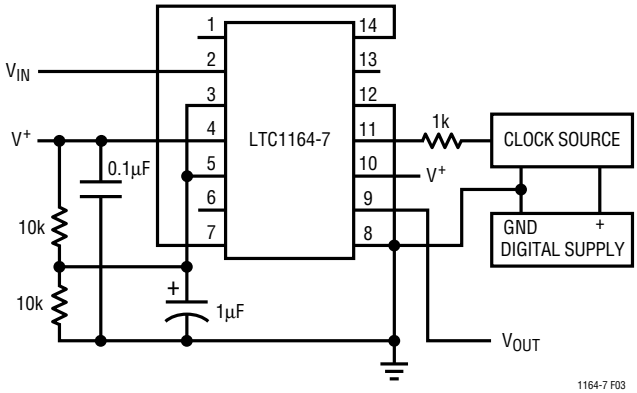


Figure 3. Single Supply Operation for an f_{CLK}/f_{CUTOFF} = 50:1

Analog Ground Pins (3, 5)

The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation, pins 3 and 5 should be connected to the analog ground plane. For single supply operation, pins 3 and 5 should be biased at 1/2 supply and should be bypassed to the analog ground plane with at least a 1µF capacitor (Figure 3). For single 5V operation at the highest f_{CLK} of 2MHz, pins 3 and 5 should be biased at 2V. This minimizes passband gain and phase variations.

Ratio Input Pin (10)

The DC level at this pin determines the ratio of the clock frequency to the cutoff frequency of the filter. Pin 10 at V^+ gives a 50:1 ratio and pin 10 at V^- gives a 100:1 ratio. For single supply operation the ratio is 50:1 when pin 10 is at V^+ and 100:1 when pin 10 is at ground. When pin 10 is not tied to ground, it should be bypassed to analog ground with a 0.1µF capacitor. If the DC level at pin 10 is switched mechanically or electrically at slew rates greater than 1V/µs while the device is operating, a 10k resistor should be connected between pin 10 and the DC source.

Filter Input Pin (2)

The input pin is connected internally through a 50k resistor tied to the inverting input of an op amp.

Filter Output Pins (9, 6)

Pin 9 is the specified output of the filter; it can typically source/sink 1mA. Driving coaxial cables or resistive loads less than 20k will degrade the total harmonic distortion of the filter. When evaluating the device's distortion an output buffer is required. A noninverting buffer, Figure 4, can be used provided that its input common-mode range is well within the filter's output swing. Pin 6 is an intermediate filter output providing an unspecified 6th order lowpass filter. Pin 6 should not be loaded.

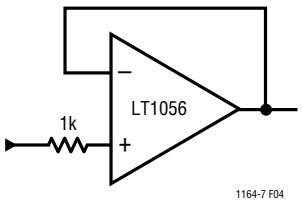


Figure 4. Buffer for Filter Output

PIN FUNCTIONS

External Connection Pins (7, 14)

Pins 7 and 14 should be connected together. In a printed circuit board the connection should be done under the IC package through a short trace surrounded by the analog ground plane.

NC Pins (1, 8, 13)

Pins 1, 8 and 13 are not connected to any internal circuit point on the device and should be preferably tied to analog ground.

APPLICATIONS INFORMATION

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pin (9). The clock feedthrough is tested with the input pin (2) grounded and it depends on PC board layout and on the value of the power supplies. With proper layout techniques the values of the clock feedthrough are shown in Table 8.

Table 8. Clock Feedthrough

V_S	50:1	100:1
Single 5V	$70\mu V_{RMS}$	$70\mu V_{RMS}$
±5V	$100\mu V_{RMS}$	$200\mu V_{RMS}$
±7.5V	$120\mu V_{RMS}$	$500\mu V_{RMS}$

Note: The clock feedthrough at Single 5V is imbedded in the wideband noise of the filter. The clock waveform is a square wave.

Any parasitic switching transients during the rise and fall edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, if bothersome, can be greatly reduced by adding a simple R/C lowpass network at the output of the filter pin (9). This R/C will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and it is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter's passband and cannot be reduced with post filtering. For instance, the LTC1164-7 wideband noise at ±5V supply is $105\mu V_{RMS}$, $95\mu V_{RMS}$ of which have frequency contents from DC up to the filter's cutoff frequency. The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

Speed Limitations

The LT1164-7 optimizes AC performance vs power consumption. To avoid op amp slew rate limiting at maximum clock frequencies, the signal amplitude should be kept below a specified level as shown in Table 9.

Table 9. Maximum V_{IN} vs V_S and Clock

POWER SUPPLY	MAXIMUM f_{CLK}	MAXIMUM V_{IN}
±7.5V	1MHz	$2.0V_{RMS}$ (f_{IN} > 20kHz) $0.7V_{RMS}$ (f_{IN} > 250kHz)
±5V	1MHz	$1.4V_{RMS}$ (f_{IN} > 20kHz) $0.5V_{RMS}$ (f_{IN} > 100kHz)
Single 5V	1MHz	$0.5V_{RMS}$ (f_{IN} > 100kHz)

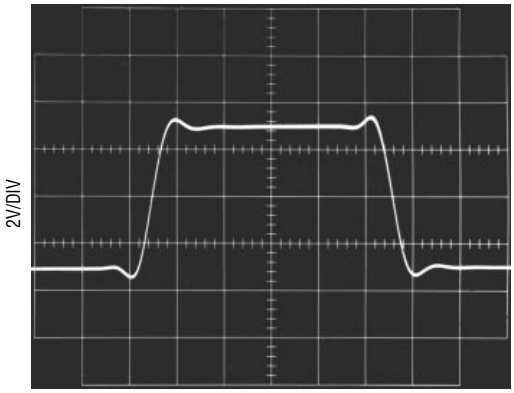
Table 10. Transient Response of LTC Lowpass Filters

LOWPASS FILTER	DELAY TIME* (SEC)	RISE TIME** (SEC)	SETTLING TIME*** (SEC)	OVER-SHOOT (%)
LTC1064-3 Bessel	$0.50/f_C$	$0.34/f_C$	$0.80/f_C$	0.5
LTC1164-5 Bessel	$0.43/f_C$	$0.34/f_C$	$0.85/f_C$	0
LTC1164-6 Bessel	$0.43/f_C$	$0.34/f_C$	$1.15/f_C$	1
LTC1264-7 Linear Phase	$1.15/f_C$	$0.36/f_C$	$2.05/f_C$	5
LTC1164-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1064-7 Linear Phase	$1.20/f_C$	$0.39/f_C$	$2.20/f_C$	5
LTC1164-5 Butterworth	$0.80/f_C$	$0.48/f_C$	$2.40/f_C$	11
LTC1164-6 Elliptic	$0.85/f_C$	$0.54/f_C$	$4.30/f_C$	18
LTC1064-4 Elliptic	$0.90/f_C$	$0.54/f_C$	$4.50/f_C$	20
LTC1064-1 Elliptic	$0.85/f_C$	$0.54/f_C$	$6.50/f_C$	20

* To 50% ±5%, ** 10% to 90% ±5%, *** To 1% ±0.5%

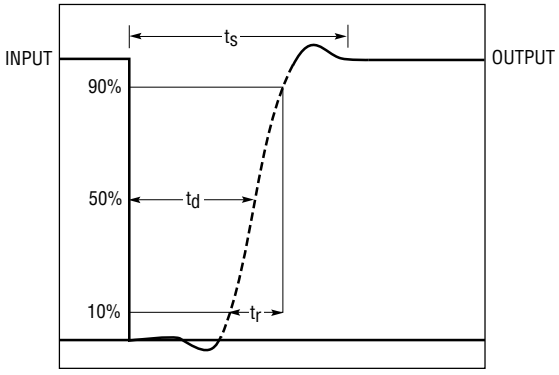
APPLICATIONS INFORMATION

Transient Response



INPUT = 1kHz ± 3V
f_{CLK} = 500kHz
f_C = 10kHz
V_S = ±7.5V

Figure 5.



RISE TIME (t_r) = $\frac{0.39}{f_{CUTOFF}}$ ±5%

SETTLING TIME (t_s) = $\frac{2.2}{f_{CUTOFF}}$ ±5%
(TO 1% of OUTPUT)

TIME DELAY (t_d) = GROUP DELAY ≈ $\frac{1.2}{f_{CUTOFF}}$
(TO 50% OF OUTPUT)

1164-7 F06

Figure 6.

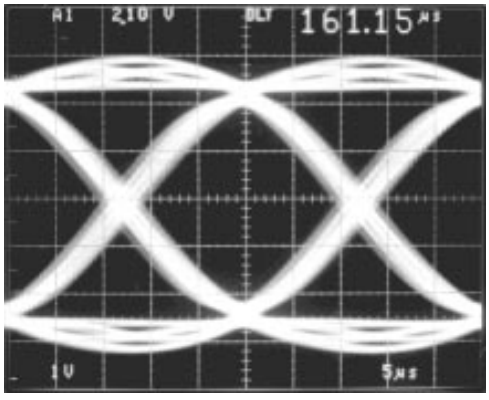
Aliasing

Aliasing is an inherent phenomenon of sampled data systems and it occurs when input frequencies close to the sampling frequency are applied. For the LTC1164-7 case at 100:1, an input signal whose frequency is in the range of f_{CLK} ±3%, will be aliased back into the filter's passband.

If, for instance, an LTC1164-7 operating with a 100kHz clock and 1kHz cutoff frequency receives a 98kHz 10mV input signal, a 2kHz, 143µV_{RMS} alias signal will appear at its output. When the LTC1164-7 operates with a clock-to-cutoff frequency of 50:1, aliasing occurs at twice the clock frequency. Table 11 shows details.

Table 11. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY (V_{IN} = 1V_{RMS}, $f_{IN} = f_{CLK} \pm f_{OUT}$) (kHz)	OUTPUT LEVEL (Relative to Input, 0dB = 1V_{RMS}) (dB)	OUTPUT FREQUENCY (Aliased Frequency f_{OUT} = ABS [$f_{CLK} \pm f_{IN}$]) (kHz)
50:1, f_{CUTOFF} = 2kHz		
190 (or 210)	–76.1	10.0
195 (or 205)	–51.9	5.0
196 (or 204)	–36.3	4.0
197(or 203)	–18.4	3.0
198 (or 202)	–3.0	2.0
199.5 (or 200.5)	–0.2	0.5
100:1, f_{CUTOFF} = 1kHz		
97 (or 103)	–74.2	3.0
97.5 (or 102.5)	–53.2	2.5
98 (or 102)	–36.9	2.0
98.5 (or 101.5)	–19.6	1.5
99 (or 101)	–5.2	1.0
99.5 (or 100.5)	–0.7	0.5



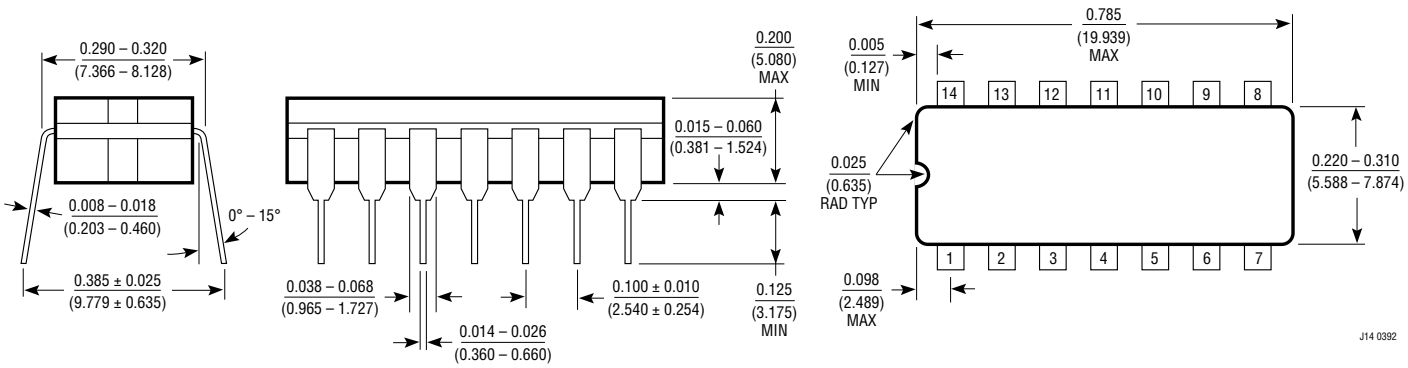
V_S = ±7.5V
f_{CLK} = 1MHz
f_C = 20kHz
(f_{CLK}/f_C) = 50:1

Figure 7. Eye Diagram

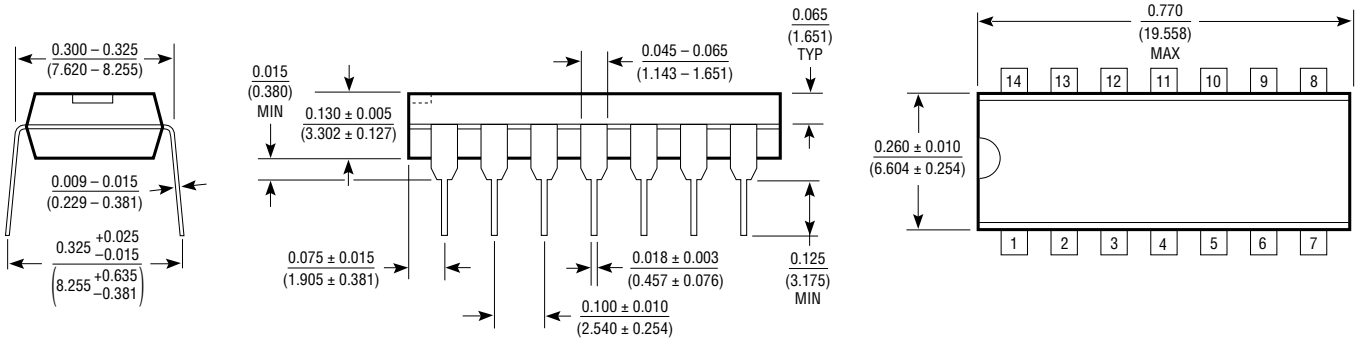
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

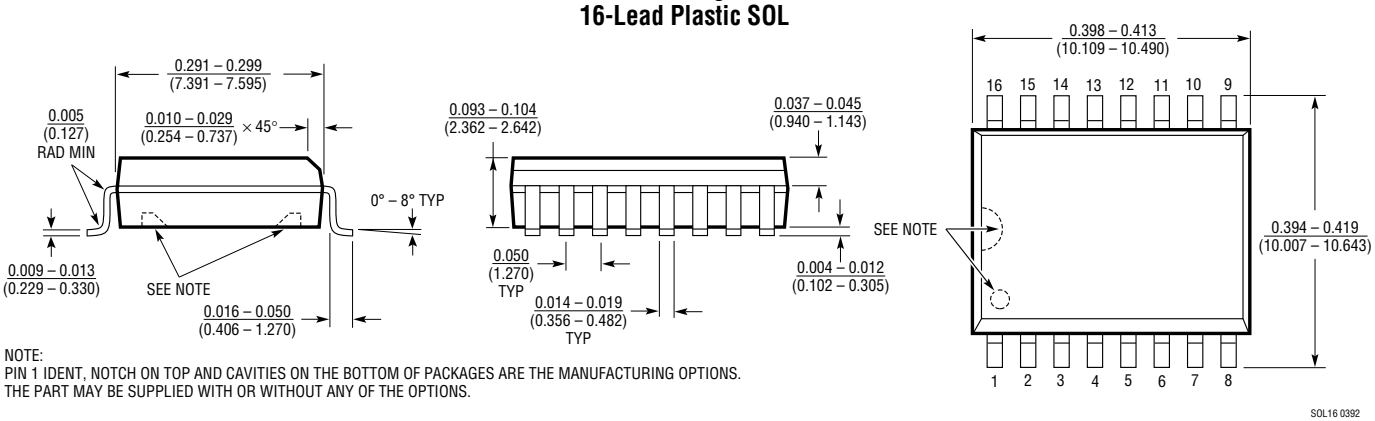
J Package
14-Lead Ceramic DIP



N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOL



NOTE:
PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS.
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7487
(408) 432-1900 • FAX: (408) 434-0507 • TELEX: 499-3977

LT/GP 1292 10K REV 0