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USB Power Manager with OVP and Li-Ion/Polymer Charger

FEATURES

Programmable Input Current Limit:
- Single Resistor at CLPROG Pin to Set and Monitor Input Current

Battery Charger/Ideal Diode/Controller:
- **13V Overvoltage Protection**
- Full Featured Battery Charger with 4.2V Float
- Up to 1.25A Programmable Charge Current
- Thermal Regulation Maximizes Charge Current Without Risk of Overheating
- Internal 2 Hour Termination Timer from Onset of Voltage Mode Charging
- Automatic Load Switchover to Battery Power with Internal Ideal Diode and Drive Output for Optional External MOSFET
- NTC Thermistor Input
- Bad Battery Time-Out Detection
- 4mm × 3mm 12-Lead DFN Package

APPLICATIONS

- Automatic Battery Charging/Load Switchover
- Backup Battery Charger
- Uninterrupted Supplies

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DESCRIPTION

The LTC®4067 is a USB power management and Li-Ion/ Polymer battery charger designed for portable battery powered applications. The part controls total current used by the USB peripheral for operation and battery charging. The total input current may be left unregulated, or it may be limited to 20% or 100% of the programmed value up to 1.5A (typically 500mA). Battery charge current is automatically reduced such that the sum of the load current and the charge current does not exceed the programmed input current.

With the addition of an external P-channel MOSFET the LTC4067 can withstand voltages up to 13V.
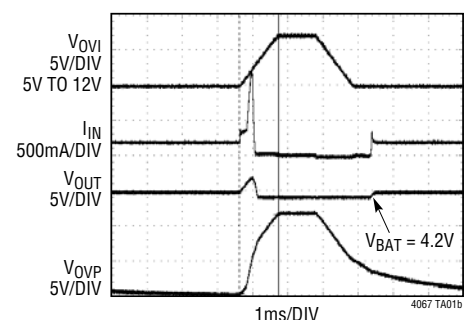
The LTC4067 includes a complete constant current/constant voltage linear charger for single cell Li-Ion batteries. The float voltage applied to the battery is held to a tight 0.4% tolerance, and charge current is programmed using an external resistor to ground. An end-of-charge status output, $\overline{CHRG}$, indicates full charge. Also featured is an NTC thermistor input used to monitor battery temperature while charging.

The LTC4067 is available in a 12-lead low profile 4mm × 3mm DFN package.

TYPICAL APPLICATION

I_{LIM0}	I_{LIM1}	$I_{IN(MAX)}$
L	H	O (SUSPEND)
L	L	$200V/R_{CLPROG}$
H	H	$1000V/R_{CLPROG}$
H	L	FIXED (2A)
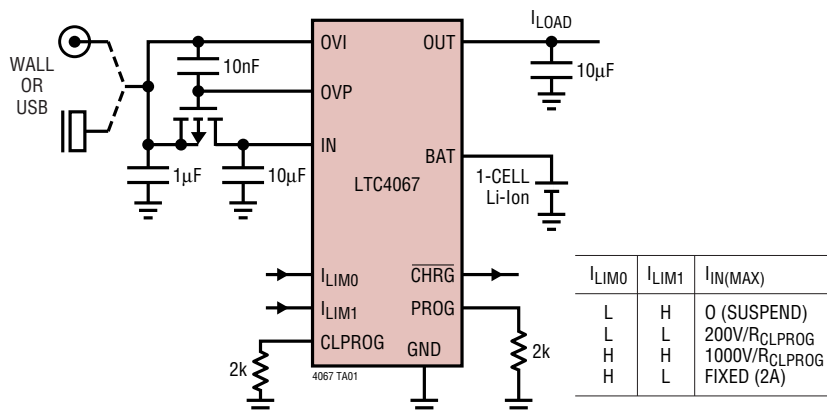
OVP Response to Ramp Input at OVI

LTC4067

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ABSOLUTE MAXIMUM RATINGS

(Note 1)

IN, OUT, BAT Voltage

(t < 1ms, Duty Cycle < 1%)...................... –0.3V to 7V
Steady State, IN, OUT, BAT Voltage.............. –0.3V to 6V
NTC, I_{LIM0}, I_{LIM1}, PROG, CLPROG, $\overline{CHRG}$, GATE

Voltages (Note 6)...................................–0.3V to V_{CC}
OVI, OVP Voltages .... –0.3V to 13V
Operating Temperature Range .... –40°C to 85°C
Storage Temperature Range................... –65°C to 125°C
Max Junction Temperature (T_{JMAX}) .... 125°C

PACKAGE/ORDER INFORMATION

TOP VIEW

CLPROG	1	12	IN
$\overline{CHRG}$	2	11	OUT
NTC	3	10	BAT
I_{LIM0}	4	9	GATE
I_{LIM1}	5	8	PROG
OVI	6	7	OVP

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DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DE PART MARKING
LTC4067EDE	4067

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range (Note 3), otherwise specifications are at T_A = 25°C. Note 2 unless otherwise noted, V_{IN} = 5V, V_{BAT} = 3.7V, V_{ILIM0} = 0V, V_{ILIM1} = 0V, R_{PROG} = 2k, R_{CLPROG} = 2k, V_{OVI} = 0V, V_{NTC} = V_{IN}/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	IN Supply Voltage		●			5.5	V
I_{IN}	Input Supply Current	V_{NTC} = 5V (Forces I_{BAT} = I_{PROG} = 0) SUSPEND: V_{ILIM0} = 0V, V_{ILIM1} = 5V, No Load SHUTDOWN: V_{PROG} = 5V	● ● ●		0.4 52 12	1.2 90 30	mA μA μA
I_{BAT}	Battery Supply Current	V_{BAT} = 4.3V, Charging Stopped SUSPEND: V_{ILIM0} = 0V V_{ILIM1} = 5V, No Load, V_{IN} = 5.5V SHUTDOWN: V_{PROG} = 5V IDEAL DIODE: V_{IN} = Float, BAT Powers OUT, No Load	● ● ● ●		14 6 2.5 60	30 12 5 100	μA μA μA μA
$I_{IN(MAX)}$	Maximum Input Current Limit	V_{OUT} = 4V, I_{LIM0} = 5V I_{LIM1} = 0V (Note 7)		1.5	2		A

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 3), otherwise specifications are at $T_A = 25°C$. Note 2 unless otherwise noted, $V_{IN} = 5V$, $V_{BAT} = 3.7V$, $V_{ILIM0} = 0V$, $V_{ILIM1} = 0V$, $R_{PROG} = 2k$, $R_{CLPROG} = 2k$, $V_{OVI} = 0V$, $V_{NTC} = V_{IN}/2$.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IUVLO}	IN Undervoltage Lockout	Rising Threshold Falling Threshold	●	3.5	3.8 3.675	4	V V
V_{BUVLO}	BAT Undervoltage Lockout	Rising Threshold Falling Threshold		2.5	2.8 2.7	3	V
Current Limit							
$R_{FWD,IN}$	On-Resistance of Input Power FET	$I_{OUT} = 200mA$			220		mΩ
I_{LIM}	Input Current Limit	HPWR Mode: $V_{ILIM0} = V_{ILIM1} = 5V$ LPWR Mode	● ●	475 90	500 98	525 110	mA mA
V_{CLPROG}	CLPROG Pin Servo Voltage	HPWR Mode: $V_{ILIM0} = V_{ILIM1} = V_{CC}$, $V_{OUT} = 4V$ LPWR Mode : $V_{OUT} = 4V$	● ●	0.95 0.18	1 0.2	1.05 0.22	V V
I_{SS}	Soft Start Inrush Current	$R_{CLPROG} = 4k$, Short at OUT (Note 8)			0.3		mA/µs
Battery Charger							
V_{FLOAT}	Regulated Output Voltage	$I_{BAT} = -2mA$ (0°C – 85°C); $I_{BAT} = -2mA$		4.185 4.167	4.2 4.2	4.215 4.234	V V
I_{CC-CHG}	Constant-Current Mode Charge Current	$R_{PROG} = 2k$, No Load at OUT $R_{PROG} = 1k$, No Load at OUT, $R_{CLPROG} = 1k$	● ●	470 940	500 1000	530 1060	mA mA
$I_{CHG(MAX)}$	Maximum Charge Current	$R_{PROG} = R_{CLPROG} = 0$ (Note 7)			2		A
V_{PROG}	PROG Pin Servo Voltage	$R_{PROG} = 2k$; $I_{BAT} = -500mA$ $R_{PROG} = 1k$; $I_{BAT} = -1A$ $R_{PROG} = 2k$, $V_{BAT} < V_{TRIKL}$, $I_{BAT} = I_{TRIKL}$	● ●	980 980 90	1000 1000 100	1020 1020 110	mV mV mV
I_{EOC}	End-of-Charge BAT Current	$V_{BAT} = 4.2V$; As A Ratio to Full BAT Charge Current (I_{CC-CHG})		0.08	0.093	0.106	mA/mA
I_{TRIKL}	Trickle Charge Current	$V_{BAT} = 2V$		35	50	60	mA
V_{RECHRG}	Recharge Battery Threshold Voltage	$V_{FLOAT} - V_{RECHRG}$	●	65	100	135	mV
t_{TIMER}	TIMER Period			1.7	2	2.3	hrs
	Low Battery Trickle Charge Time	Percent of Total Charge Time, $V_{BAT} < 2.8V$			25		%
T_{LIM}	Junction Temperature in Constant Temperature Mode	(Note 4)			105		°C
Ideal Diode							
R_{FWD}	On-Resistance, V_{ON} Regulation	$V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = -200mA$, Measured as $\Delta V/\Delta I$			200		mΩ
$R_{DIO,ON}$	On-Resistance V_{BAT} to V_{OUT}	$V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = -1A$			220		mΩ
V_{FWD}	Voltage Forward Drop ($V_{BAT} - V_{OUT}$)	$V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = -1mA$ $V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = -200mA$ $V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = -1A$	●	10	25 70 240	40	mV mV mV
$I_{D(MAX)}$	Ideal Diode Current Limit	$V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$ (Notes 4, 5)		1.5	2.1		A
I_{GPU}	GATE Pin Output Pull Up Current	$V_{OUT} > V_{BAT}$, $V_{GATE} = 0V$			1.9		mA
I_{GPD}	GATE Pin Output Pull Down Current	$V_{ILIM0} = 0V$, $V_{ILIM1} = 5V$, $V_{BAT} = 4.3V$, $I_{OUT} = 1A$, $V_{GATE} = 4.3V$			1.9		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 3), otherwise specifications are at T_A = 25°C. Note 2 unless otherwise noted, V_{IN} = 5V, V_{BAT} = 3.7V, V_{ILIM0} = 0V, V_{ILIM1} = 0V, R_{PROG} = 2k, R_{CLPROG} = 2k, V_{OVI} = 0V, V_{NTC} = V_{IN}/2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC							
I_{NTC}	NTC Input Leakage Current	V_{NTC} = 2.5V			0	±1	µA
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		$0.725 \cdot V_{IN}$	$0.733 \cdot V_{IN}$ $0.02 \cdot V_{IN}$	$0.741 \cdot V_{IN}$	V V
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		$0.287 \cdot V_{IN}$	$0.29 \cdot V_{IN}$ $0.02 \cdot V_{IN}$	$0.293 \cdot V_{IN}$	V V
V_{DIS}	NTC Disable Voltage	NTC Input voltage to GND (Falling) Hysteresis	●	80	100 30	120	mV mV
Logic							
F_{MOD}	Serrated Fault Pulse Modulation Frequency at $\overline{CHRG}$ Pin	$(V_{DIS} < V_{NTC} < V_{HOT})$ or $(V_{NTC} > V_{COLD})$ V_{BAT} < 2.9V for Longer Than Trickle Charge Time			1.5 6		Hz Hz
F_{PW}	Serrated Fault Pulse Width at $\overline{CHRG}$ Pin	$(V_{DIS} < V_{NTC} < V_{HOT})$ or $(V_{NTC} > V_{COLD})$ V_{BAT} < 2.9V for Longer Than Trickle Charge Time			1.33 2.62		µs µs
F_{TF}	Serrated Fault Pulse Frequency at $\overline{CHRG}$ Pin	$(V_{DIS} < V_{NTC} < V_{HOT})$ or $(V_{NTC} > V_{COLD})$ or V_{BAT} < 2.9V for Longer Than Trickle Charge Time			35		kHz
V_{OL}	Output Low Voltage ($\overline{CHRG}$)	I_{SINK} = 5mA	●			1.5	V
V_{IH}	Enable Input High Voltage	ILIM0, ILIM1 Pin Low to High	●	1.2			V
V_{IL}	Enable Input Low Voltage	ILIM0, ILIM1 Pin High to Low	●			0.4	V
I_{PULLDN}	Logic Input Pull Down Current	ILIM0, ILIM1			2		µA
V_{OVTH}	Overvoltage Protection Threshold (OVI Pin)	V_{OVI} Rising Threshold Hysteresis		5.8	6 250	6.2	V mV
$V_{PROG,SD}$	Shutdown Threshold	$V_{CC} - V_{PROG}$ Rising (Note 6) Hysteresis			1.4 50		V mV
$I_{PROG,PULLUP}$	PROG Pin Shutdown Sense Current	V_{PROG} = 1V			3.5		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Current into a pin is positive and current out of a pin is negative. All Voltages referenced to GND

Note 3: The LTC4067 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C ambient operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 4: Specification is guaranteed by design and not 100% tested in production.

Note 5: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature exceeds 125°C when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.
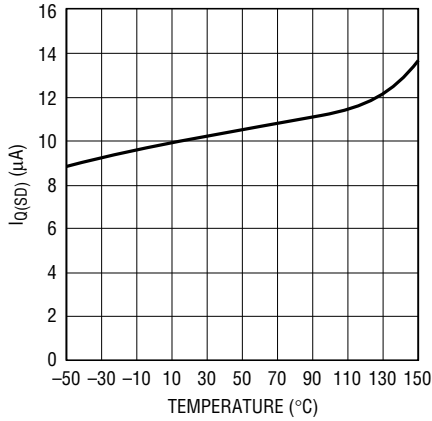
Note 6: V_{CC} is the greater of V_{IN}, V_{OUT} or V_{BAT}.

Note 7: Accuracy of programmed current may degrade for currents greater than 1A.

Note 8: CLPROG soft-start scales with inverse of CLPROG resistor. If R_{CLPROG} = 2k, then I_{SS} = 0.6mA/µs.
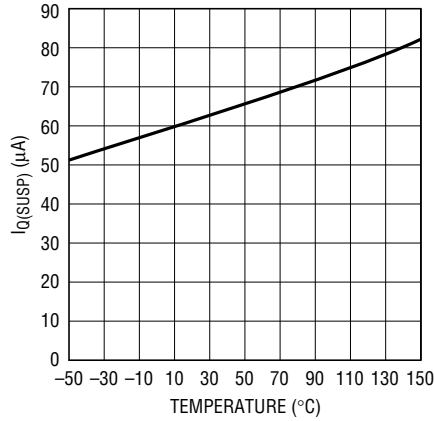
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TYPICAL PERFORMANCE CHARACTERISTICS

Input Supply Current vs Temperature (Shutdown Mode)

4067 G01
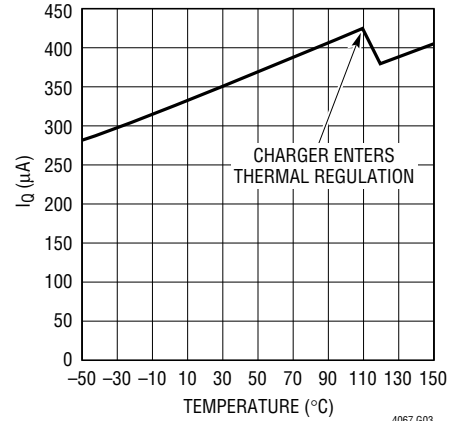
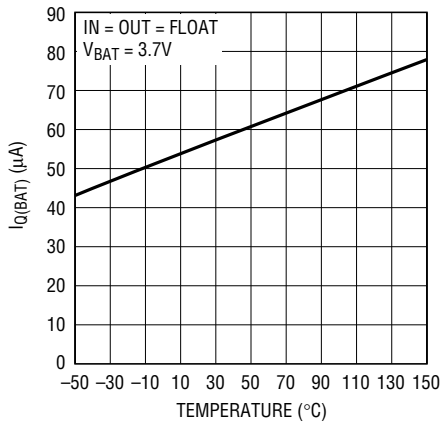### Input Supply Current vs Temperature (Suspend Mode)

4067 G02
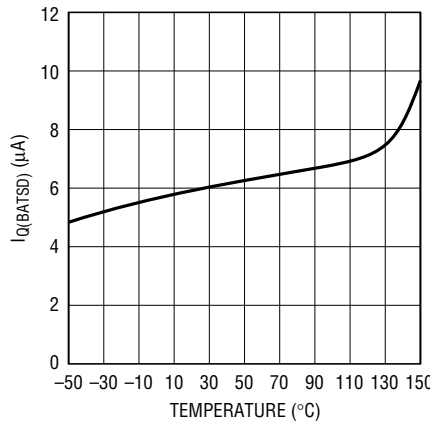
Input Supply Current vs Temperature

CHARGER ENTERS THERMAL REGULATION

4067 G03

Battery Current vs Temperature

IN = OUT = FLOAT
V_{BAT} = 3.7V

4067 G04

Battery Current vs Temperature (Shutdown)

4067 G09

Input Current Limit vs Temperature (High Power)

V_{CLPROG}

I_{LIM}
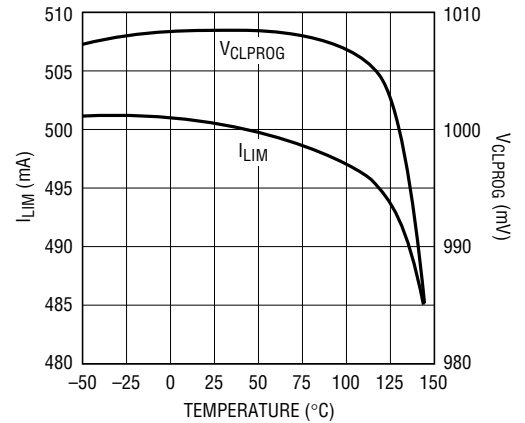
4067 G05

Input Current Limit vs Temperature (Low Power)

V_{CLPROG}

I_{LIM}
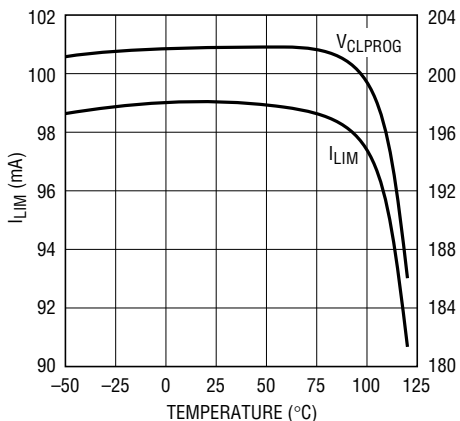
4067 G06

V_{CLPROG} vs Temperature at I_{IN} = 500mA

HPWR

V_{OUT} = 4V
R_{CLPROG} = 2k
I_{OUT} = 200mA

LPWR
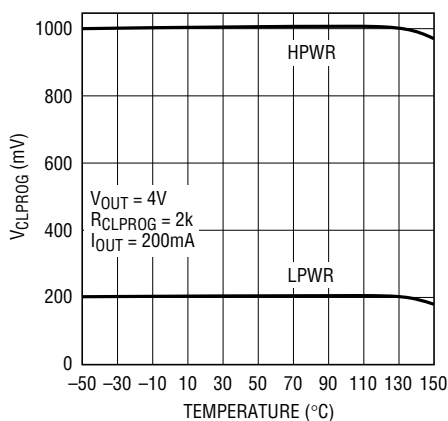
4067 G07

R_{ON} vs Temperature

V_{IN} = 4.45V
R_{CLPROG} = 0k
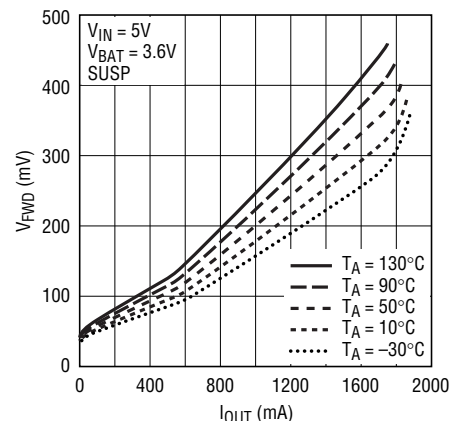HPWR

R_{ON}, 1A
R_{ON}, 500mA
R_{ON}, 200mA
R_{ON}, 100mA
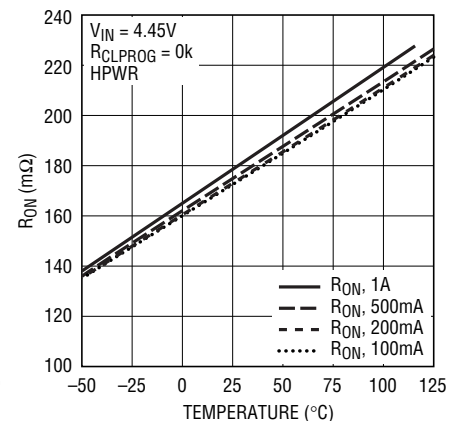
4067 G08

TYPICAL PERFORMANCE CHARACTERISTICS

V_PROG vs Temperature at I_BAT = –500mA

4067 G11
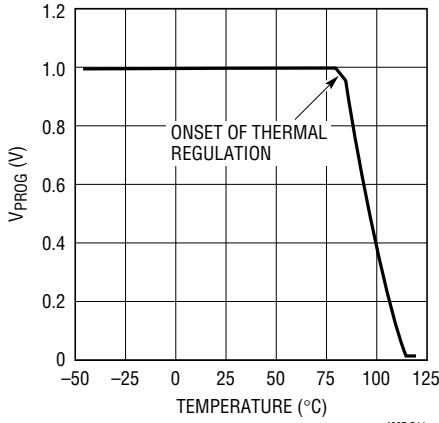
Battery Float Voltage vs Temperature

4067 G10
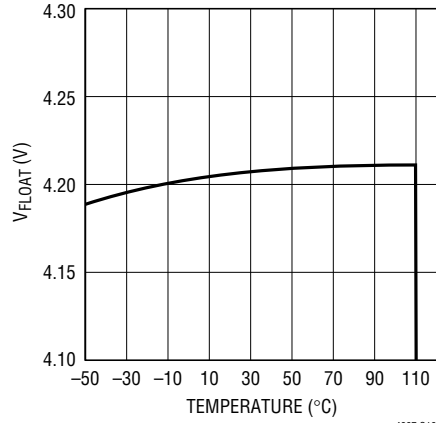
Battery Regulated (Float) Voltage vs Input Voltage

4067 G12

Charge Current vs Battery Voltage

4067 G13

Charge Current vs Battery Voltage

4067 G14
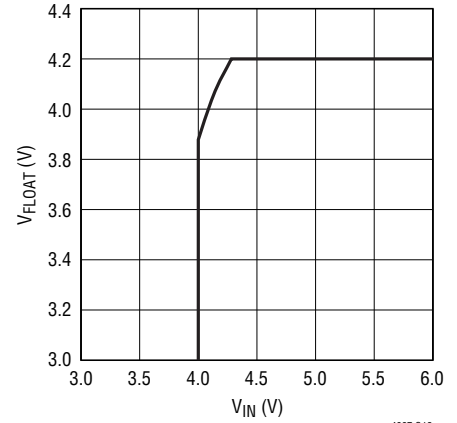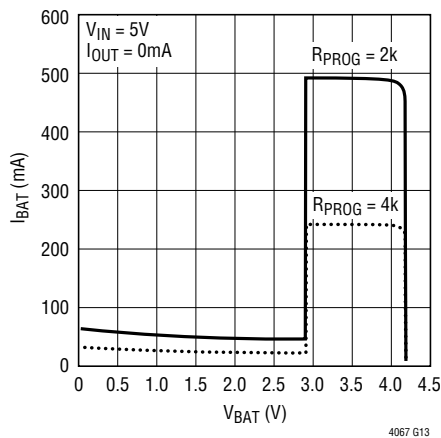
Charge Current vs Temperature (Thermal Regulation)
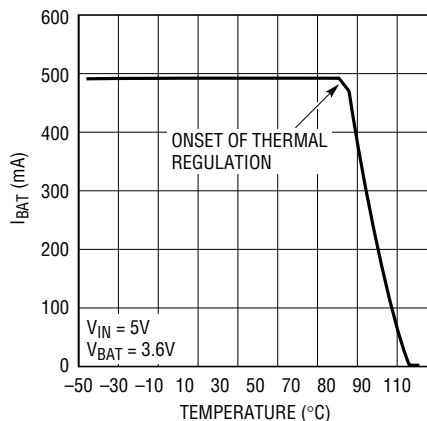
4067 G17

Ideal Diode Forward Voltage vs Current and Temperature

4067 G18

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TYPICAL PERFORMANCE CHARACTERISTICS

Ideal Diode Forward Voltage and Resistance vs Current
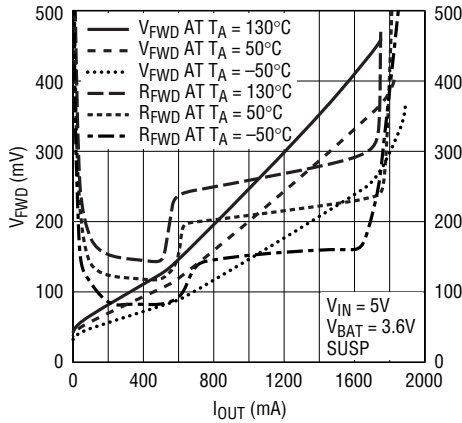
4067 G19

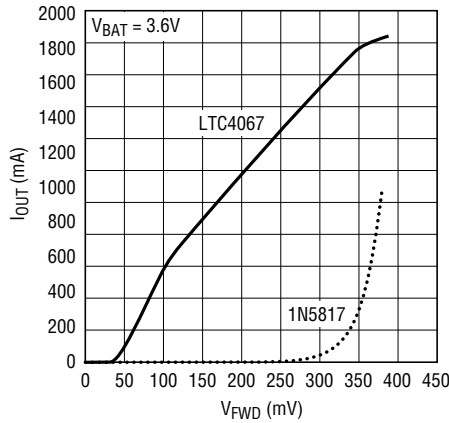### Ideal Diode and Schottky Diode Forward Voltage vs Current

4067 G13

V_{PROG} vs I_{BAT}
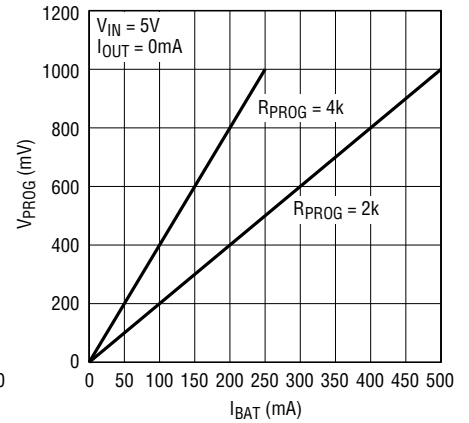
4067 G21

V_{CLPROG} vs I_{IN}
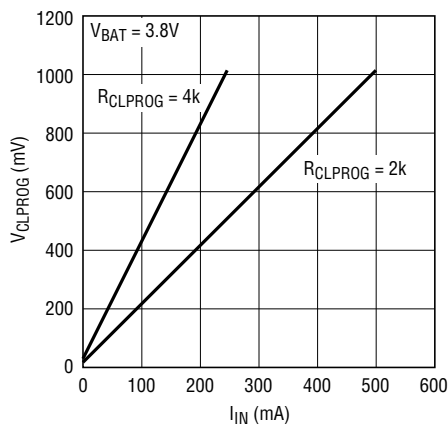
4067 G22

I_{IN} or I_{BAT} and I_{OUT} HPWR Mode
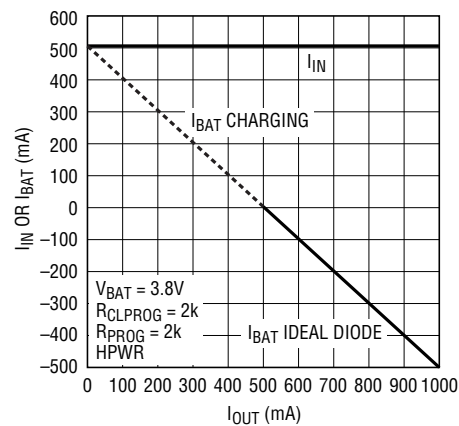
4067 G23

TYPICAL PERFORMANCE CHARACTERISTICS

$(V_{IN} - V_{OUT})$ vs I_{OUT}

V_{IN} = NTC = 4.4V
CLPROG = 2k
I_{LIM0} = 4.4V
I_{LIM1} = 4.4V

4067 G28

$\overline{CHRG}$ Pin Serrated Pulse for NTC Faults

2V/DIV

20µs/DIV   4067 G31

$\overline{CHRG}$ Pin Serrated Pulse for BAD BAT Faults

2V/DIV

20µs/DIV   4067 G32

$\overline{CHRG}$ V_{OL} vs $I_{\overline{CHRG}}$

4067 G33

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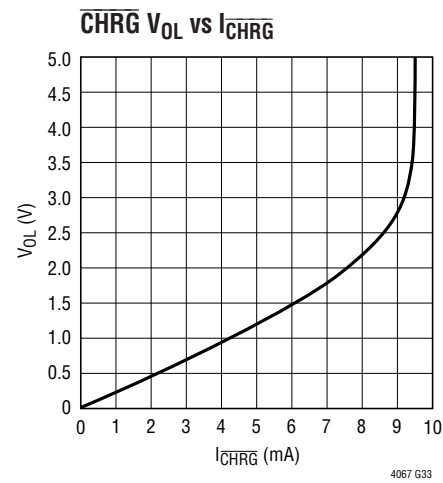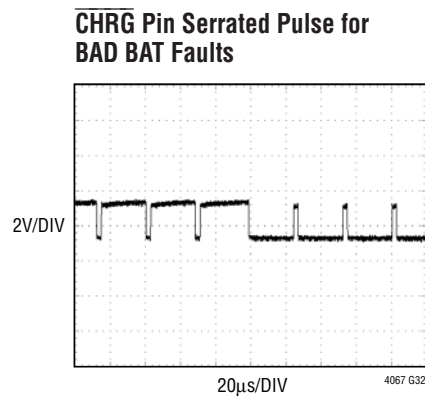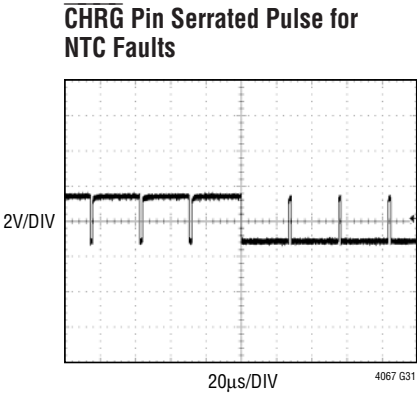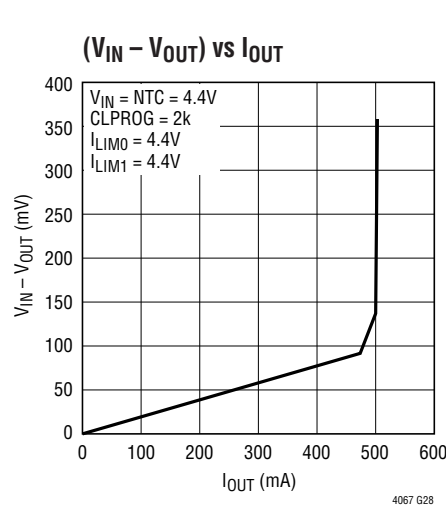
PIN FUNCTIONS

CLPROG (Pin 1): Current Limit Program Pin. Connecting a 1% resistor, R_{CLPROG}, to ground programs input current limit depending on the selected operating mode. Operating mode and input current limit are programmed depending on the I_{LIM0} and I_{LIM1} pin voltages according to the following table:

Table 1. I_{LIM} Programming

I_{LIM0}	I_{LIM1}	I_{LIMIT} (A)	MODE
L	H	0	SUSPEND
L	L	$200V/R_{CLPROG}$	Low Power
H	H	$1000V/R_{CLPROG}$	High Power
H	L	2	CLDIS

The maximum CLPROG resistance value should be no more than 5k. Ground to disable the current limit function.

CHRG (Pin 2): Open Drain Charge/Fault Status Output. When the battery is being charged, the CHRG pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the charge current drops below a programmable level or the supply is removed, the CHRG pin is forced into a high impedance state. Float or tie to ground when not in use.

NTC (Pin 3): Thermistor sense input to the thermistor monitoring circuits. Under normal operation, tie a thermistor from the NTC pin to ground and a resistor of equal value from the NTC pin to IN. Connect the NTC pin to ground to disable this feature.

I_{LIM0} (Pin 4): Current Limit Control Input. Float or connect to ground when not in use (see Table 1).

I_{LIM1} (Pin 5): Current Limit Control Input. Float or connect to ground when not in use (see Table 1).

OVI (Pin 6): Overvoltage Protection Sense Input. Connect to ground when not in use. Bypass to OVP with a 10nF capacitor.

OVP (Pin 7): Overvoltage Protection Output. Drive output for an external high-voltage protection PFET. Float when not in use.

PROG (Pin 8): Charge Current Program Pin. Connecting a 1% resistor, R_{PROG}, to ground programs the charge current during the constant-current portion of the charge cycle according to the following formula:

$$I_{CC-CHG} \text{ (A)} = 1000V/R_{PROG}$$

If the PROG pin is pulled above the V_{SD} threshold or left floating, the LTC4067 enters low power SHUTDOWN mode to conserve power, in this way an open-drain driver in series with the PROG resistor serves as an ENABLE control. Grounding this pin disables charge current limit and turns off CHRG status signal.

GATE (Pin 9): External Ideal Diode Gate Connection. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to OUT and the drain should be connected to BAT. It is important to maintain high impedance on this pin and minimize all leakage paths.

BAT (Pin 10): Single-Cell Li-Ion Battery. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to OUT through the ideal diode or be charged from the battery charger.

OUT (Pin 11): Output Voltage of the PowerPath™ Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from OUT. The LTC4067 will partition the available power between the external load on OUT and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to OUT ensures that OUT is powered even if the load exceeds the allotted input current from IN or if the IN power source is removed. OUT should be bypassed with a low impedance multilayer ceramic capacitor of at least 10µF.

IN (Pin 12): USB Input Voltage. IN will usually be connected to the USB port of a computer or a DC output wall adapter. IN should be bypassed with a low impedance multilayer ceramic capacitor of at least 1µF.

Exposed Pad (Pin 13): Ground. The exposed pad is ground and must be soldered to the PC board for proper functionality and for maximum heat transfer.

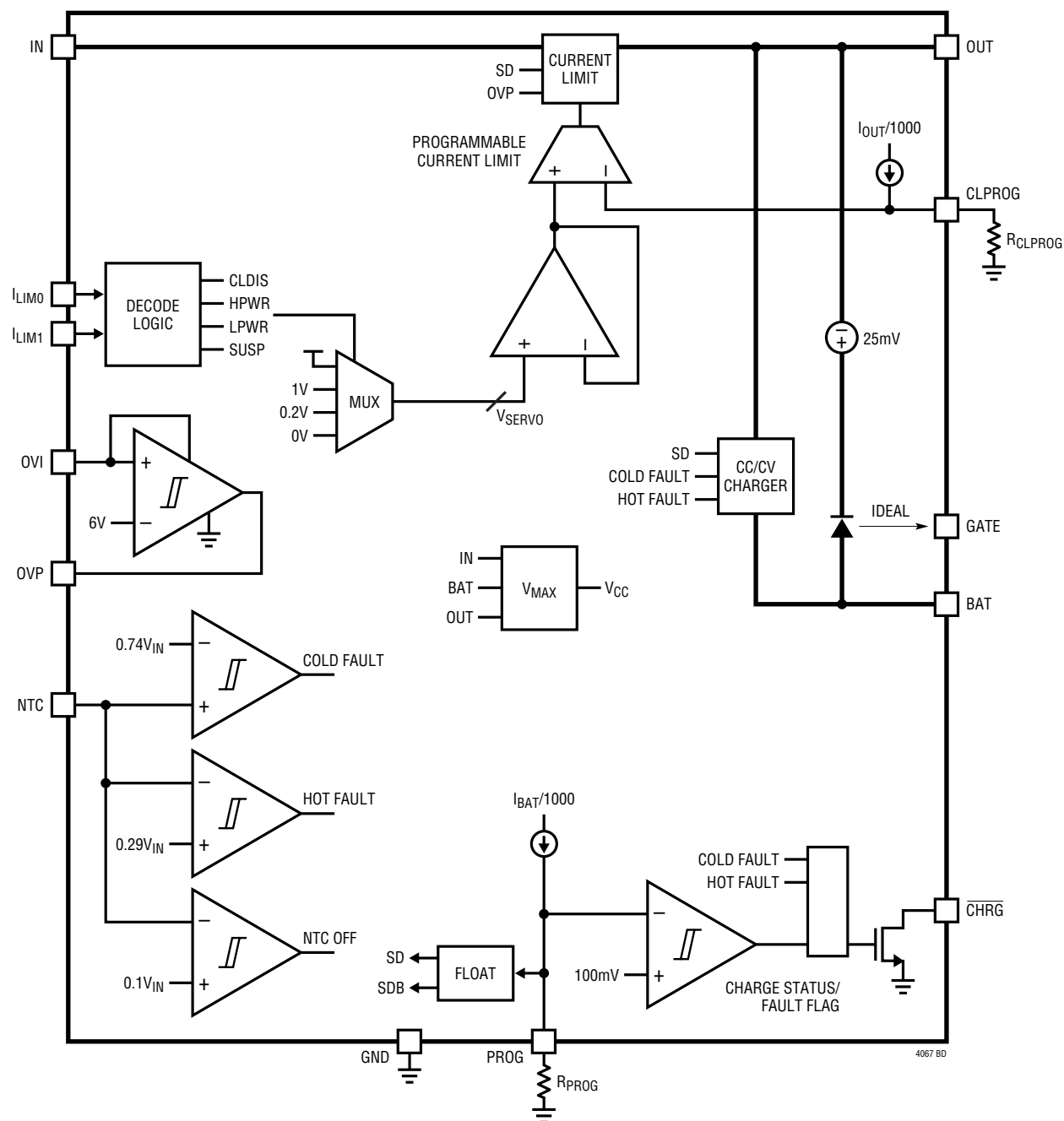PowerPath is a trademark of Linear Technology Corporation.

BLOCK DIAGRAM

Figure 1. Simplified Block Diagram

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Introduction

The LTC4067 is a complete PowerPath controller for battery powered USB applications. The LTC4067 is designed to receive power from a USB source (or a wall adapter) or a battery. It can then deliver power to an application connected to the OUT pin and a battery connected to the BAT pin (assuming that an external supply other than the battery is present). Power supplies that have limited current resources (such as USB V_{BUS} supplies) should be connected to the IN pin which has a programmable current limit. Battery charge current will be adjusted to ensure that the sum of the charge current and the load current does not exceed the programmed input current limit.

An internal ideal diode function provides power from the battery when output/load current exceeds the input current limit or when the input power is removed. Powering the load through the ideal diode instead of connecting the load directly to the battery allows a fully charged battery to remain fully charged until external power is removed. Once external power is removed the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

Furthermore, powering switching regulator loads from the OUT pin (rather than directly from the battery) results in shorter battery charge times. This is due to the fact that switching regulators typically require constant input power. When this power is drawn from the OUT pin voltage (rather than the lower BAT pin voltage) the current consumed by the switching regulator is lower leaving more current available to charge the battery.

Finally, the LTC4067 provides overvoltage controller circuitry which, when used in conjunction with an external P-channel MOSFET, will protect against overvoltage damage if a wall adapter with greater than 6V output is used. The circuit will tolerate input voltages up to 13V without damage.

USB PowerPath Controller

The input current limit and charge control circuits of the LTC4067 are designed to limit input current as well as control battery charge current as a function of I_{OUT}. OUT drives the combination of the external load and the battery charger.

If the combined load does not exceed the programmed input current limit, OUT will be connected to IN through an internal 200mΩ P-channel MOSFET.

If the combined load at OUT exceeds the programmed input current limit, the battery charger will reduce its charge current by the amount necessary to enable the external load to be satisfied while maintaining the programmed input current. Even if the battery charge current is set to exceed the allowable USB current, the USB specification will not be violated. The input current limit will ensure that the USB specification is never violated. Furthermore, load current at OUT will always be prioritized and only excess available current will be used to charge the battery.

The current out of the CLPROG pin is a fraction (1/1000th) of the IN current. When a programming resistor is connected from CLPROG to GND, the voltage on CLPROG represents the input current:

$$I_{IN} = \frac{V_{CLPROG}}{R_{CLPROG}} \bullet 1000$$

The input current limit is programmed by the I_{LIM0} and I_{LIM1} pins (see Table 1 in PIN FUNCTIONS). The LTC4067 can be configured to limit input current to one of several possible settings as well as be deactivated (USB suspend). The input current limit will be set by the appropriate servo voltage and the resistor on CLPROG according to the following expressions:

$$I_{LIM} (A) = 0 \text{ (SUSPEND)}$$

$$I_{LIM} = \frac{200V}{R_{CLPROG}} \text{(Low Power)}$$

$$I_{LIM} = \frac{1000V}{R_{CLPROG}} \text{(High Power)}$$

$$I_{LIM} (A) = 2A \text{ (CLDIS)}$$

Under worst-case conditions, the USB specification will not be violated with an R_{CLPROG} of greater than 2.1k.

Current Limit Disable (CLDIS)

When I_{LIM1} is low and I_{LIM0} is high, the input current limit is set to a higher current limit for increased charging and

OPERATION

current availability at OUT. This mode is typically used when there is power available from a wall adapter.

Suspend Mode

When I_{LIM1} is high and I_{LIM0} is low, the LTC4067 enters suspend mode to comply with the USB specification. In this mode, the power path between IN and OUT is put in a high impedance state to reduce the IN input current to 50μA. If no other power source is available to drive OUT, the system load connected to OUT is supplied through the ideal diode connected to BAT.

Ideal Diode From BAT to OUT

The LTC4067 has an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and external ideal diodes will respond quickly whenever OUT drops below BAT.

If the load increases beyond the input current limit, additional current will be pulled from the battery via the ideal diodes. Furthermore, if power to IN (USB) is removed, then all of the application's power will be provided by the battery via the ideal diodes. The ideal diodes are fast enough to keep OUT from dropping with just the recommended output capacitor. The ideal diode consists of a precision amplifier that enables an on-chip P-channel MOSFET whenever the voltage at OUT is approximately 30mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 200mΩ. If this is sufficient for the application, then no external components are necessary. However, if more conductance is needed, an external P-channel MOSFET can be added from BAT to OUT.

The GATE pin of the LTC4067 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the MOSFET should be connected to OUT and the drain should be connected to BAT. Capable of driving a 1nF load, the GATE pin can control an external P-channel MOSFET having extremely low on-resistance.

If the BAT voltage is below the V_{BUVLO} threshold the ideal diodes are disabled.

IN Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors IN and keeps the input current limit circuitry off until IN rises above the rising UVLO threshold (3.8V) and at least 50mV above OUT. Hysteresis on the UVLO turns off the input current limit if IN drops below 3.675V or 50mV below OUT. When this happens, system power at OUT will be drawn from the battery via the ideal diode. To minimize the possibility of oscillation in and out of UVLO when using resistive input supplies, the input current limit is reduced when IN falls to within a few hundred millivolts of the UVLO threshold. To ensure that the full input current limit is available and a complete battery charge cycle can be achieved, apply at least 4.25V to IN.

Battery Charger

The LTC4067 includes a constant-current/constant-voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing.

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below 2.8V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.8V, the battery charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach 1000V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional current will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the battery voltage approaches the 4.2V required to maintain a full charge, otherwise known as the float voltage, the

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OPERATION

charge current begins to decrease as the LTC4067 enters constant-voltage mode. Once the battery charger detects that it has entered constant-voltage mode, the two hour safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, the timer will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.3ms. The charge cycle and safety timer will also restart if the IN UVLO cycles low and then high (e.g. IN is removed and then replaced).

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1000th of the battery charge current is delivered to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1000 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1000V}{I_{CC-CHG}}, I_{CC-CHG} = \frac{1000V}{R_{PROG}}$$

In either the constant-current or constant-voltage charging modes, the PROG pin voltage will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CC-CHG} due to limited input current available and prioritization with the system load drawn from OUT.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 105°C. Thermal regulation protects the LTC4067 from excessive temperature due to high power operation or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC4067 or external components. The benefit of the LTC4067 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Low Power Shutdown

The LTC4067 enters a low power shutdown mode if the PROG pin is pulled above the shutdown threshold, V_{SD}. In shutdown, the BAT pin current is reduced to 5μA, the IN pin current is reduced to 10μA, the internal battery charge timer and end-of-charge comparator output are both reset. All power paths are put in a high impedance state.

A weak (2.5μA) pull up at the PROG pin causes the LTC4067 to enter low power shutdown if the PROG pin is floated. An external N-channel MOSFET transistor with its drain tied in series with the PROG pin, or an open drain driver may thereby serve as an enable input for the LTC4067.

NTC

Under normal operation, tie a thermistor from the NTC pin to GND and a resistor of equal value from NTC to IN. When the voltage on this pin is above $0.74 \bullet V_{IN}$ (cold, 0°C) or below $0.29 \bullet V_{IN}$ (hot, 50°C) the charge timer is suspended, but not cleared, the charging is disabled and the $\overline{CHRG}$ pin flashes from Hi-Z to active pull-down with a serrated pulse. When the voltage on NTC comes back to between $0.29 \bullet V_{IN}$ and $0.74 \bullet V_{IN}$, the charger timer continues from where it left off, the charging is re-enabled

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if the battery is below the recharge threshold. There is approximately 3°C of temperature hysteresis associated with each of the input comparators. If the NTC pin is tied to GND, thermistor qualified charging is disabled.

Fault Conditions

The $\overline{CHRG}$ pin provides information as to the charging status, indicating an active charge cycle with a strong open-drain pull down at the $\overline{CHRG}$ pin. NTC faults and bad battery faults are indicated with serrated pulses; this is described in more detail under the heading Fault Conditions in the Applications Information section.

When the battery is being charged, the $\overline{CHRG}$ pin is pulled low by an internal N-channel MOSFET. When the charge cycle enters voltage mode charging and the charge current is reduced below $I_{CC-CHG}/10$, the $\overline{CHRG}$ indicates that the charge cycle is nearly complete by switching to a Hi-Z state. Also when the battery voltage exceeds the OUT voltage and the input supply is removed, or the LTC4067 is put into suspend or shutdown modes, the $\overline{CHRG}$ pin is forced into a high impedance state. If a bad battery is detected, or if an NTC temperature fault is detected, charging is halted and the $\overline{CHRG}$ pin switches to a series of serrated open-drain pull down pulses. These serrated current pulses are designed to cause an LED connected from the $\overline{CHRG}$ pin to a positive supply voltage to visibly flash, indicating to the user that there is a problem, as well as allowing a microcontroller to detect a fault condition within 300µs.

Overvoltage Protection

The OVI input is provided to sense potentially hazardous voltages at the input in case an unregulated wall adapter is applied. If an overvoltage condition is detected the OVP pin is driven high to turn off an external PMOS transistor inserted in series with the IN pin to disconnect the high voltage from the LTC4067.

Table 2 lists recommended P-channel MOSFETs to use with the LTC4067.

Table 2. Recommended OVP Transistors

PART NUMBER	DESCRIPTION
IRLML6402	P-channel 16V
FDR8508P	Dual P-channel 16V

If the OVP pin is high, the power path from IN to OUT is disabled.

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APPLICATIONS INFORMATION

Battery Charger Stability Considerations

The LTC4067 battery charger contains two control loops: constant voltage and constant current. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive battery lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to ground. Furthermore, a 4.7µF capacitor with a 0.2Ω to 1Ω series resistor is required from BAT to ground to keep the ripple voltage low when the battery is disconnected.

In constant-current mode the PROG pin is in the feedback loop, not the BAT pin. Because of the additional pole created by PROG pin capacitance, additional capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 6k. However additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 500kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq 1/(2\pi \cdot 5 \cdot 10^5 \, C_{PROG})$$

Average, rather than instantaneous, battery current may be of interest to the user. For example, if a switching power supply operating in low current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses. In such a case, a simple RC filter at the PROG pin measures the average BAT pin current, as shown in the figure below. A 20k resistor has been added between the PROG pin and the filter capacitor to ensure stability. This technique may also be used on the CLPROG pin.
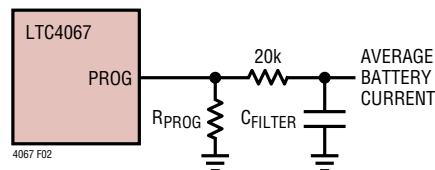

Figure 2. Isolating Capacitive Load on PROG Pin and Filtering.

NTC Thermistor Input Pin

An NTC input provides the option of charge qualification using battery temperature and an external thermistor thermally coupled to the battery. When the thermistor senses an over or under temperature condition, charging is suspended until the temperature returns to a safe operating range. The $\overline{CHRG}$ pin flashes while this out of temperature condition persists. If the NTC pin is grounded, NTC charge qualification is disabled. For more information on the $\overline{CHRG}$ pin during fault conditions see the Fault Conditions heading.

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor in thermal contact with the battery. The thermal regulation feature of the LTC4067, requires a thermistor, R_{NTC}, between the NTC pin and GND as well as a second resistor, R_{NOM}, from the NTC pin to IN. The recommended R_{NOM} resistor has a value equal to the value of the chosen NTC thermistor at 25°C. (For a Vishay NTHS0603N02N1002 thermistor this value is 10k.) The LTC4067 charger goes into hold mode when the resistance, R_{HOT}, of the NTC thermistor drops to 0.41 times the value of R_{NOM} or approximately 4.1k, which is at 50°C. Hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature range. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4067 is also designed to go into hold mode when the value of the

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NTC thermistor, R_{COLD}, increases to 2.82 times the value or R_{NOM}. (For a Vishay NTHS0603N02N1002 thermistor this value is 28.2k which corresponds to a temperature of approximately 0°C). The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip points.

Fault Conditions

The $\overline{CHRG}$ pin is used to signal two distinct fault condi-tions: NTC faults and bad battery faults. Both of these conditions are signaled at the $\overline{CHRG}$ pin with a series of serrated open-drain pull-down pulses that are intended to produce a visible "blinking" at an LED tied to this pin as well as to produce a pulse train that is detectable to a microprocessor input connected to this pin. The serrated pulses are described with the aid of Figure 3, assuming that the $\overline{CHRG}$ pin is connected to a positive rail with a resistive pull-up. When an NTC fault condition is detected during a normal charge cycle, the $\overline{CHRG}$ pin immediately goes from a strong open-drain pull down to a high-im-pedance state that pulses on for 1.4µs and then off at a 35kHz rate. This signal is further modulated by a 1.5Hz blink frequency that reverses from pulsing high-to-low to pulsing low-to-high.
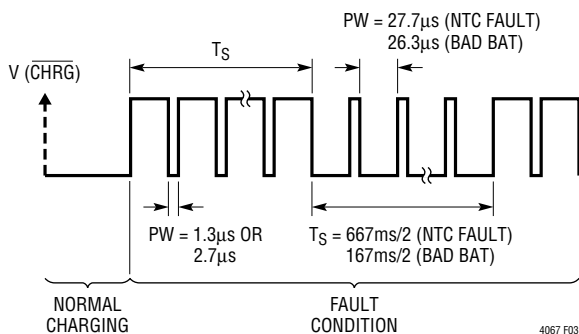
Table 3 illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 3. $\overline{CHRG}$ Output Pin

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLE
Charging	0Hz	0Hz (Lo-Z)	100%
$I_{BAT} < I_{CC-CHG}/10$	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	4.7% to 95.3%
Bad Battery	35kHz	6.1Hz at 50%	9.4% to 90.6%

A bad battery fault has a 2.8µs pulse at the same rate that is modulated by a 6Hz blink frequency. As the $\overline{CHRG}$ pin immediately changes state upon entering a failure mode, a microprocessor observing this pin detects the fault condi-tion within 29µs of the failure occurring, by measuring the pulse width. Furthermore the blink frequency is visually detected by hooking this signal up to an LED.

When connecting a microprocessor with a positive logic suppy that is different than the LED anode, a diode must be inserted in series with the microcontroller input so as to aviod the condition where the LED may inadvertantly power up the microcontroller. A circuit that allows visual fault and/or charge status as well as providing a safe microcontroller interface is shown in Figure 4.
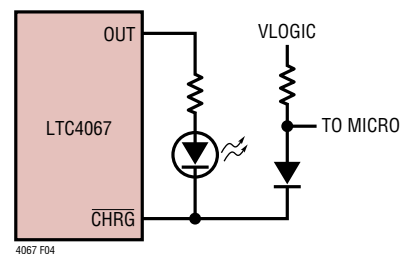

Figure 3

Figure 4. $\overline{CHRG}$ Pin Connection to Drive a Microcontroller at the Same Time as Providing a Visual Fault and/or Charge Status

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TYPICAL APPLICATIONS

Li-Ion Charger from 5V Wall Adapter with Overvoltage Protection

Figure 5 illustrates an application where the LTC4067 is used to charge a single-cell Li-Ion battery from a wall adapter with built-in overvoltage protection.

Overvoltage protection is achieved with the OVI and OVP pins of the LTC4067 along with an external PFET in series with the IN pin. This PFET disconnects the LTC4067 from potentially damaging overvoltage conditions that are caused by attaching the wrong wall adapter. When the OVI input senses a voltage greater than V_{OVTH}, the OVP output is pulled up to disable the PFET. When OVI is below this threshold, the OVP output is pulled low, turning on this PFET. In the event that large in-rush currents are expected, it is recommended that a decoupling capacitor be placed from OVI to GND. The body diode of this PFET must be connected so that it is reverse biased when an overvoltage condition exists.

A 10nF capacitor is recommended to dynamically pull-up on the gate of Q1 if a fast edge occurs at the wall input during a hot-plug. In the event that this capacitor is pre-charged below the OVI rising threshold when a high voltage spike occurs, the OVP output cannot guarantee turning off Q1 before the IN pin voltage exceeds the absolute maximum

voltage for this pin. This may occur in the event that the wall input suddenly steps from 5.5V to a higher voltage. In this case, a zener diode is also recommended to keep the IN pin voltage to a safe level.

In the example of Figure 5, the input current limit from the wall adapter is programmed to 1A with a 1k resistor from CLPROG to GND (assuming I_{LIM0} and I_{LIM1} are held high). And the charge current is programmed to 500mA via the 2k resistor from the PROG pin to GND.

An optional second external PFET connected between OUT and BAT serves as a high-performance ideal diode; to connect the load to the battery with an extremely low impedance. This ideal diode is controlled by the GATE output pin whenever the wall adapter is not present or the load demands more current than is available from the wall adapter input (Connect the source of the PFET to OUT and the drain to BAT).

Instantaneous monitoring of both input current and charge current is achieved by measuring the voltages at the CLPROG and PROG pins respectively.

Low-power shutdown is engaged by any of the following. Disabling an external NFET tied in series with the PROG pin resistor, by floating the PROG pin with a single-pole switch, by tying R_{PROG} to an open-drain output, by pulling
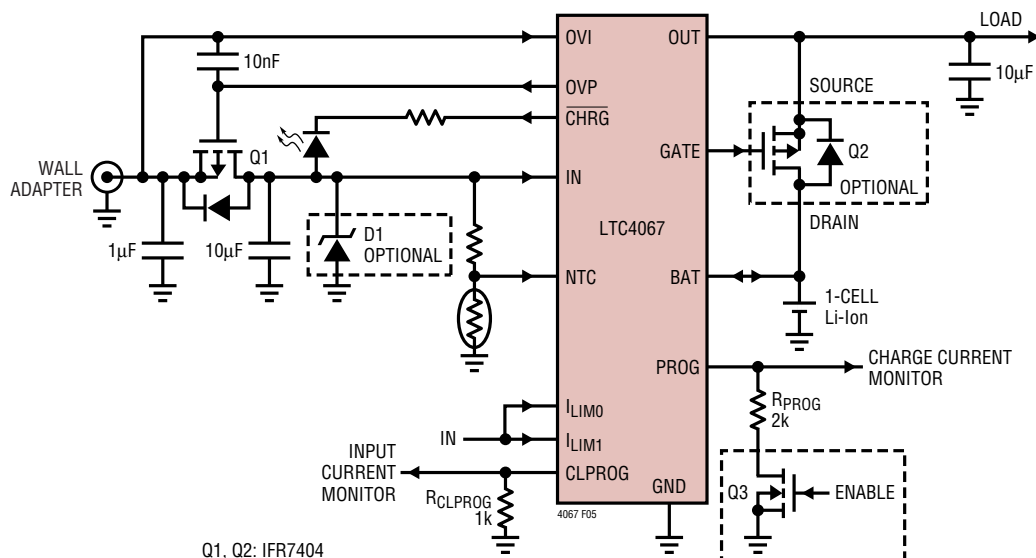
Figure 5. Li-Ion Charger/Controller with Overvoltage Protection

TYPICAL APPLICATIONS

the PROG pin to the most positive supply rail (IN, BAT or OUT)(not shown). In low-power shutdown total current consumption of the LTC4067 is less than 20µA.

Figure 6 illustrates an application for charging single-cell Li-Ion batteries directly from a USB bus conforming to the USB requirements for low-power (LPWR), high-power (HPWR), or self-powered functions. Here, the LTC4067 ensures that the load at OUT sees the USB potential when the USB port is applied. When the USB port is removed the load is powered from the battery through an internal 200mΩ ideal diode. Optionally an external PFET driven by the GATE pin is used to improve performance by reducing the series resistance.

The 2k resistor at the CLPROG pin ensures that the maximum current drawn from the USB input port is kept below the maximum allowed depending on the permitted power allocation. 500mA for HPWR USB function or 100mA for LPWR USB function. The LTC4067 is configured to comply with the USB SUSPEND specification by driving the I_{LIM0} pin low and the I_{LIM1} pin high, whereby the load at OUT is powered from the battery and the only current drawn from the USB port is due to the two series NTC pin resistors.

The 2k resistor at the PROG pin selects 500mA for the charge current to automatically charge a single-cell Li-Ion battery following a constant-current/constant-voltage (CC/CV) algorithm with a built-in timer that halts charging after the battery achieves the maximum float voltage

of 4.2V. Note that actual charge current depends on the load current, as the charger shares the USB current with the load. During a charge cycle the $\overline{CHRG}$ pin signals that the battery is charging in constant-current mode by pulling to GND through an open-drain drive output capable of driving an LED for visual indication of charge status. When the charge current drops to less than 10% of the programmed charge current, and the battery is above the recharge threshold (4.1V), the $\overline{CHRG}$ pin assumes a high impedance state (but top-off charge current continues to flow until the internal charge timer elapses). Bad battery and battery out-of-temperature conditions are also flagged with the $\overline{CHRG}$ pin as described in the Fault Conditions section.

If the load demands more current than allowed by the USB current limit, the charge current is automatically scaled back. Up to the point where an ideal diode function from BAT to OUT turns on once the OUT voltage drops below the BAT voltage. When the ideal diode is engaged, the battery charge cycle is paused and the load at OUT draws current both from the USB port as well as from the battery.

At any time, the user may monitor both instantaneous charge current and instantaneous USB current by observing the PROG pin and CLPROG pin voltages respectively. When probing these nodes with a capacitive sensor, a series resistance is recommended to ensure that bulk capacitance from these two nodes to GND does not exceed 50pF.
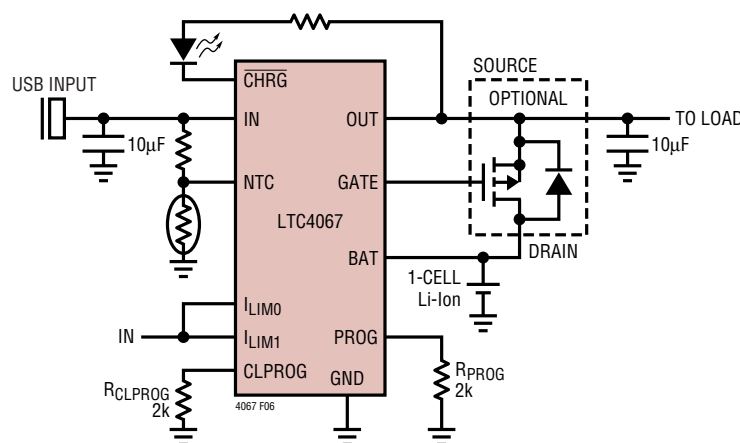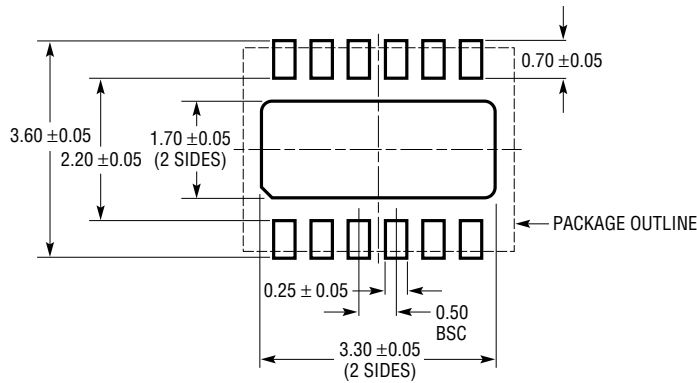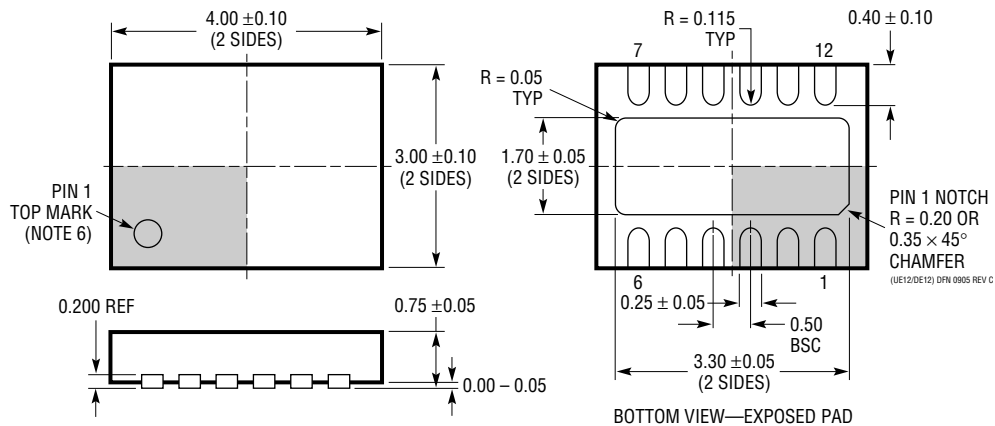

Figure 6. USB Battery Charger

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PACKAGE DESCRIPTION

DE/UE Package
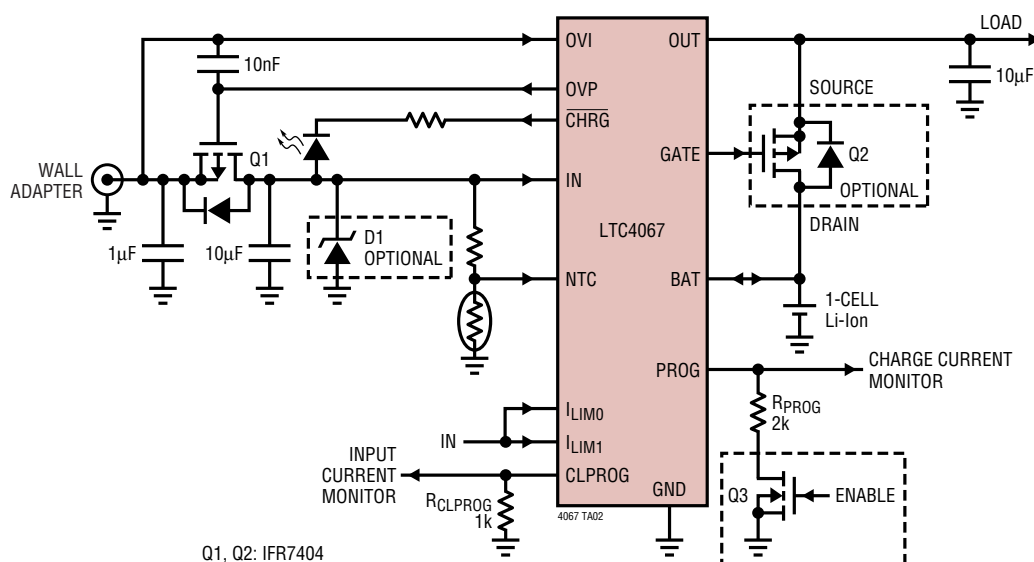**12-Lead Plastic DFN (4mm × 3mm)**
(Reference LTC DWG # 05-08-1695 Rev C)

0.70 ±0.05

3.60 ±0.05

1.70 ±0.05
(2 SIDES)

2.20 ±0.05

PACKAGE OUTLINE

0.25 ± 0.05

0.50
BSC

3.30 ±0.05
(2 SIDES)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

4.00 ±0.10
(2 SIDES)

3.00 ±0.10
(2 SIDES)

PIN 1
TOP MARK
(NOTE 6)

R = 0.115
TYP

0.40 ± 0.10

R = 0.05
TYP

7   12

1.70 ± 0.05
(2 SIDES)

PIN 1 NOTCH
R = 0.20 OR
0.35 × 45°
CHAMFER

(UE12/DE12) DFN 0905 REV C

6   1

0.25 ± 0.05

0.50
BSC

3.30 ±0.05
(2 SIDES)

BOTTOM VIEW—EXPOSED PAD

0.200 REF

0.75 ±0.05

0.00 – 0.05

NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Li-Ion Charger/Controller with Overvoltage Protection

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Battery Chargers		
LTC4054	Standalone Linear Li-Ion Battery Charger with Integrated Pass Transistor in ThinSOT™	Thermal Regulation Prevents Overheating, C/10 Termination, C/10 Indicator, Up to 800mA Charge Current
LTC4059	900mA Linear Lithium-Ion Battery Charger	2mm × 2mm DFN Package, Thermal Regulation, Charge Current Monitor Output
LTC4065/LTC4065A	Standalone Li-Ion Battery Chargers in 2 × 2 DFN	4.2V, ±0.6% Float Voltage, Up to 750mA Charge Current, 2mm × 2mm DFN, "A" Version has ACPR Function.
LTC4411/LTC4412	Low Loss PowerPath Controller in ThinSOT	Automatic Switching Between DC Sources, Load Sharing, Replaces ORing Diode
LTC4412HV	High Voltage Power Path Controllers in ThinSOT	V_{IN} = 3V to 36V, More Efficient than Diode ORing, Automatic Switching Between DC Sources, Simplified Load Sharing, ThinSOT Package.
Power Management		
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	Seamless Transition Between Power Sources: USB, Wall Adapter and Battery; 95% Efficient DC/DC Conversion
LTC4055	USB Power Controller and Battery Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode, 4mm × 4mm QFN16 Package
LTC4066	USB Power Controller and Li-Ion Battery Charger with Low-Loss Ideal Diode	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 50mΩ Ideal Diode, 4mm × 4mm QFN24 Package
LTC4085	USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, 4mm × 3mm DFN14 Package
LTC4089/ LTC4089-5	USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger	High Efficiency 1.2A Charger from 6V to 36V (40V Max) Input Charges Single-Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ option, Bat-Track Adaptive Output Control (LTC4089), Fixed 5V Output (LTC4089-5), 4mm × 3mm DFN-14 Package

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LT 0407 • PRINTED IN USA

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