Data Sheet

# LTC7050

## Dual SilentMOS Smart Power Stage in 5mm × 8mm LQFN

## FEATURES

- 70 A Peak Output Current per Channel
- SilentMOS™ Smart Power Stage
  - Utilizes Low EMI/EMC Silent Switcher®2 Architecture
  - Ultra-low SW-Voltage Overshoot
  - Frequency Up to 2 MHz
- $V_{IN}$ Up to 14 V
- Up to 94% Efficiency at 1 MHz with 1.8 $V_{OUT}$
- Integrated Boost Diodes and Capacitors
- Accurate Switch Current Monitoring
- Power MOSFET Overcurrent Protection
- Input Overvoltage and Bias Undervoltage Protection
- Thermal Monitor with Overtemperature Flag
- 3.3 V/5 V Compatible Tri-State PWM Input
- 5mm × 8mm LQFN Package

## APPLICATIONS

- High Current Servers and Workstations
- Networking/Telecom Microprocessor Supplies
- Small Form-Factor POL Converter

## TYPICAL APPLICATION

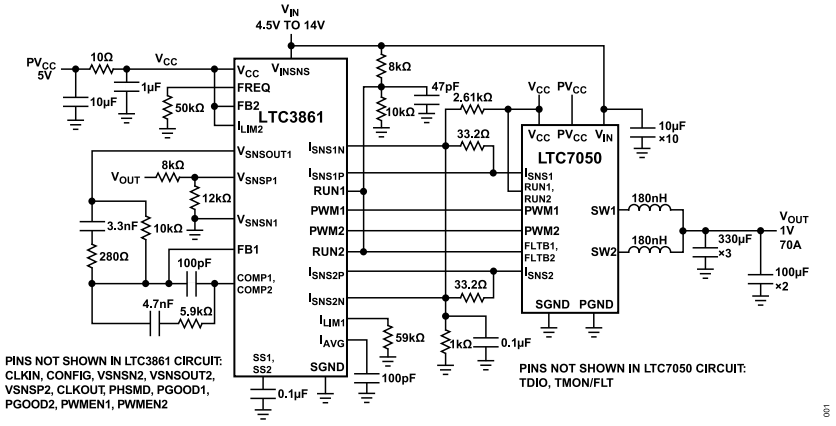


*Figure 1. 12 $V_{IN}$, 1 V/70 $A_{OUT}$ 1 MHz Dual-Phase POL Converter*

## GENERAL DESCRIPTION

The LTC7050[1] dual monolithic power stage fully integrates high speed drivers with low resistance half-bridge power switches plus comprehensive monitoring and protection circuitry in an electrically and thermally optimized package. With a suitable high frequency controller, this power stage forms a compact, high current voltage regulator system with state-of-the-art efficiency and transient response.

SilentMOS technology utilizes second generation Silent Switcher 2 architecture reducing both EMI and switch-node voltage overshoot while maximizing efficiency at high switching frequencies.

High speed current sensing provides low latency switch current information, enabling tight current balancing and immediate overcurrent protection.

Thermally-enhanced packaging provides dual 40 A rated continuous output current capability.

[1] Protected by U.S. patents, including 9525351.

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## REVISION HISTORY

**6/2023—Rev. 0 to Rev. A**

Updated Format (Universal) ... 1
Deleted Figure 2 and Figure 3; Renumbered Sequentially ... 1
Changes to Table 1 ... 4
Changes to Table 2 ... 6
Changes to Active Diode Mode Section ... 13
Changes to Power Sequence Section ... 14
Changes to Figure 29 ... 16
Added Figure 30 ... 16
Changes to Figure 31 ... 17
Added Evaluation Boards ... 18

**9/2021—Revision 0: Initial Version**

## FUNCTIONAL BLOCK DIAGRAM

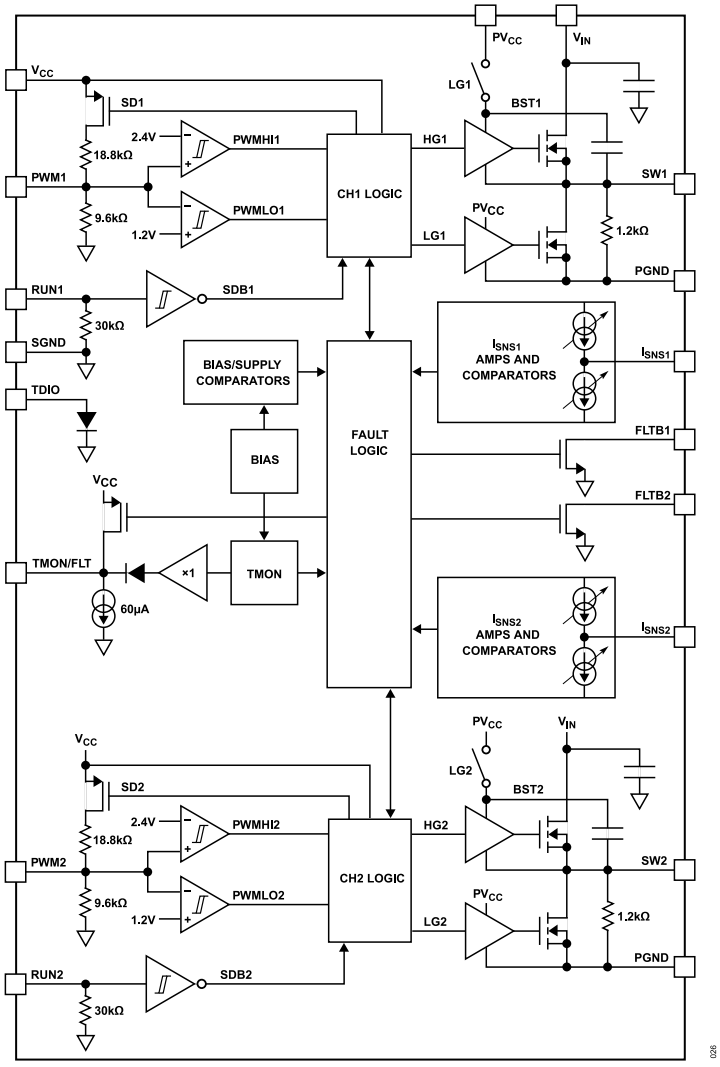



*Figure 2.*

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$T_J$ = −40°C to +125°C for the minimum and maximum values, $V_{IN}$ = 12 V, $PV_{CC}$ = $V_{CC}$ = 5 V, unless otherwise noted.

*Table 1.*

| Parameter[1] | Symbol | Test Conditions/Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IN}$ SUPPLY | | | | | | |
| Power Input Supply Range | $V_{IN}$ | | | | 14 | V |
| $V_{IN}$ Overvoltage Lockout Threshold | $V_{IN}$ | $V_{IN}$ Rising | 14.9 | | 15.7 | V |
| $V_{IN}$ Overvoltage Lockout Hysteresis[2] | $V_{IN}$ | | | 0.4 | | V |
| $V_{IN}$ Overvoltage Lockout Delay[2, 3] | $V_{IN}$ | | | 1 | | µs |
| $V_{IN}$ Shutdown Current[2] | $V_{IN}$ | $V_{IN}$ = 12 V, RUN1 = RUN2 = 0 | | 25 | | µA |
| $V_{CC}$ SUPPLY | | | | | | |
| $V_{CC}$ Input Supply Range | $V_{CC}$ | | 4.5 | 5 | 5.5 | V |
| $V_{CC}$ Undervoltage Lockout Threshold | $V_{CC(UVLO)}$ | $V_{CC}$ Rising | 4.05 | 4.15 | 4.25 | V |
| $V_{CC}$ Undervoltage Lockout Hysteresis[2] | VUVLO_HYST | | | 0.2 | | V |
| $V_{CC}$ Supply Current in Shutdown[2] | $I_{VCC(SD)}$ | RUN1 = RUN2 = 0 V | | 14 | | µA |
| $V_{CC}$ Supply Current in Active[2] | $I_{VCC\_active}$ | RUN1 = RUN2 = 5 V, PWM = Float | | 2.5 | | mA |
| $PV_{CC}$ SUPPLY | | | | | | |
| Driver Input Supply Range | $PV_{CC}$ | | 4.5 | 5 | 5.5 | V |
| $PV_{CC}$ Undervoltage Lockout Threshold | $PV_{CC(UVLO)}$ | $PV_{CC}$ Rising | 3.9 | 4.0 | 4.1 | V |
| $PV_{CC}$ Undervoltage Lockout Hysteresis[2] | PVUVLO_HYST | | | 0.35 | | V |
| $PV_{CC}$ Supply Current in Shutdown[2] | $I_{PVCC(SD)}$ | RUN1 = RUN2 = 0 V | | 300 | | µA |
| $PV_{CC}$ and $V_{CC}$ Supply Current in Active[2] | $I_{PVCC\_active}$ | RUN1 = RUN2 = 5 V, PWM = Float | | 2.5 | | mA |
| UNDERVOLTAGE TIME LOCKOUT DELAY, FROM $V_{CC}$ AND $PV_{CC}$ TO SW LOW[2, 3] | $t_{UVLO}$ | $PV_{CC}$, $V_{CC}$ Rising<br>RUN = 5 V PWM = 0 | | 1 | | µs |
| RUN INPUT | | | | | | |
| RUN High Threshold | $V_{IH\_RUN}$ | RUN Rising | 2.2 | 2.45 | 2.7 | V |
| RUN Hysteresis[2] | $V_{RUN\_HYS}$ | | | 0.2 | | V |
| EN Pull-Down Resistor[2] | $R_{PD\_RUN}$ | | | 30 | | kΩ |
| Propagation Delay for RUN Low to High[2, 3] | $T_{d\_RUNH}$ | From RUN Low ≥ High to SW = 0, PWM = 0 | | 12 | | µs |
| Propagation Delay for RUN High to Low[2, 3] | $T_{d\_RUNL}$ | From RUN High ≥ Low to SW High Z, PWM = 0 | | | 0.1 | µs |
| PWM INPUT | | | | | | |
| PWM High Threshold | $V_{IH\_PWM}$ | $V_{IN}$ = 1 V, $PV_{CC}$ = 6 V | | | 2.7 | V |
| PWM Low Threshold | $V_{IL\_PWM}$ | $V_{IN}$ = 5 V | 0.8 | | | V |
| PWM Tri-State Range | $V_{TR\_PWM}$ | $V_{IN}$ = 1 V and 5 V | 1.5 | | 2.1 | V |
| PWM Pull-Down Resistor[2] | $R_{PD\_PWM}$ | To SGND, $V_{IN}$ = 5 V | | 9.6 | | kΩ |
| PWM Pull-Up Resistor[2] | $R_{PU\_PWM}$ | To $V_{CC}$, $V_{IN}$ = 5 V | | 18.8 | | kΩ |
| Delay Time, PWM High to SW High[2, 3] | $t_{PWMHI-SW}$ | No Fault Condition | | 10 | | ns |
| Delay Time, PWM Low to SW Low[2, 3] | $t_{PWMLO-SW}$ | No Fault Condition | | 10 | | ns |
| Tri-State to Low Propagation Delay[2] | $t_{Tri\_Lo\_Delay}$ | PWM Going Low to SW Going Low, $V_{IN}$ = 5 V | | 20 | | ns |
| Tri-State to High Propagation Delay[2] | $t_{Tri\_Hi\_Delay}$ | PWM Going High to SW Going High, $V_{IN}$ = 5 V | | 30 | | ns |
| Active to Tri-State Delay Time[2, 3] | $t_{Tri\_Hold}$ | PWM Going to High Z to SW High Z | | 20 | | ns |
| PWM Minimum ON-Time[2] | $t_{PWM\_MINON}$ | $V_{IN}$ = 5 V | | 20 | | ns |
| PWM Floating Voltage | $V_{PWM\_FLOAT}$ | | 1.6 | 1.7 | 1.8 | V |
| $I_{SNS}$ OUTPUT | | | | | | |
| Current Sense Gain ($I_{MON}/I_{OUT}$)[2] | $A_{IMON}$ | $V_{ISNS}$ = 1.5 V<br>$I_{OUT}$ = 5 A to 25 A, PWM = 0, $V_{IN}$ = 5 V | 8.5 | 10 | 11.5 | µA/A |
| Overall Accuracy[2] | $I_{SNS}$ | $I_{OUT}$ = 25 A, $V_{ISNS}$ = 1.5 V, PWM = 0, $V_{IN}$ = 5 V<br>Accuracy at Trim | | 250 ±12.5 | | µA |
| | | $I_{OUT}$ = −10 A, $V_{ISNS}$ = 1.5 V, PWM = 0 | | 100 | | µA |

## SPECIFICATIONS

*Table 1. (Continued)*

| Parameter[1] | Symbol | Test Conditions/Comments | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| IMON Operational Voltage Range | $V_{IMON}$ | $V_{IN}$ = 5 V | 1.2 | | 2.0 | V |
| FLTB OUTPUT | | | | | | |
| Fault Bar Open-Drain Pull-Down Resistance[2] | $R_{FLTB-PD}$ | FLTB Low | | | 1 | kΩ |
| TMON/FLT OUTPUT | | | | | | |
| Thermal Monitor Gain[2, 3] | $A_{TMON}$ | 0°C < $T_J$ < 150°C | | 8 | | mV/°C |
| Thermal Monitor Voltage[2, 3] | $V_{TMON}$ | $T_J$ = 0°C | | 0.6 | | V |
| | | $T_J$ = 25°C, $V_{IN}$ = 1 V | 780 | 800 | 825 | mV |
| | | $T_J$ = 125°C | | 1.6 | | V |
| Overtemperature Protection Accuracy[2, 3] | OTP | | | 150 | | °C |
| Overtemperature Hysteresis[2, 3] | OTP_Hys | | | 40 | | °C |
| Thermal Monitor Maximum Source Current[2] | $I_{SOURCE\_TMON}$ | $T_J$ = 25°C, $T_{MON}$ Forced at 0 V, $V_{IN}$ = 1 V | | 650 | | µA |
| Thermal Monitor Maximum Sink Current[2] | $I_{SINK\_TMON}$ | $T_J$ = 25°C, $T_{MON}$ Forced at 1.28 V, $V_{IN}$ = 1 V | | 45 | | µA |
| Tdiode Forward Voltage Drop[2] | $V_{Tdiode}$ | $T_J$ = 25°C, $I_F$ = 0.1 mA, $V_{IN}$ = 1 V | | 678 | | mV |
| Tdiode Voltage Drop Temperature Coefficient[2, 3] | $V_{Tdiode}$ | $I_F$ = 0.1 mA | | –1.8 | | mV/°C |
| SW NODE | | | | | | |
| SW Floating Voltage[2] | $V_{SW\_Float}$ | $V_{IN}$ = 12 V | | 0.7 | | V |
| SW Pull-Down Resistance[2] | $R_{SW-PGND}$ | $V_{IN}$ = 5 V | | 1.2 | | kΩ |
| OVERCURRENT LIMITS | | | | | | |
| Positive Overcurrent Threshold[2] | $I_{\_OCP}$ | PWM = H, $V_{IN}$ = 0.2 V | 80 | 90 | 100 | A |
| Negative Overcurrent Threshold[2] | $I_{\_NCP}$ | PWM = L, $V_{IN}$ = 1 V | | –45 | | A |
| Positive Overcurrent Blanking Time[2, 3] | $t_{Blank\_OC}$ | PWM = H | | 22 | | nS |
| Negative Overcurrent Blanking Time[2, 3] | $t_{Blank\_NC}$ | PWM = L | | 55 | | nS |
| Positive Zero Current Threshold[2] | $I_{\_ZCP}$ | $V_{IN}$ = 0.2 V | | 5 | | A |
| Negative Zero Current Threshold[2] | $I_{\_ZCN}$ | $V_{IN}$ = 1 V | | –8 | | A |

1 All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

2 Specifications are $T_A$ = 25°C.

3 This parameter is not tested but is guaranteed by design.

## ABSOLUTE MAXIMUM RATINGS

*Table 2.*

| Parameter | Rating |
|---|---|
| $V_{IN}$ DC Voltage | –0.3 V to +16 V |
| $V_{IN}$ Transient Voltage | –0.3 V to +20 V |
| SW1, SW2 Voltage | –0.3 V to +16 V DC |
| SW1, SW2 Voltage (20 ns) | –2 V to +20 V |
| $PV_{CC}$, $V_{CC}$ Voltage | –0.3 V to +6 V |
| RUN1, RUN2 | –0.3 V to ($V_{CC}$ + 0.3 V) |
| PWM1, PWM2 | –0.3 V to ($V_{CC}$ + 0.3 V) |
| $I_{SNS1}$, $I_{SNS2}$ | –0.3 V to ($V_{CC}$ + 0.3 V) |
| FLTB1, FLTB2 | –0.3 V to ($V_{CC}$ + 0.3 V) |
| TDIO Voltage/Current | –0.3 V/+5 mA |
| AbsMax Junction Temperature[1, 2] | 125°C |
| Storage Temperature | –55°C to +150°C |
| Reflow (Package Body) Temperature | 260°C |

[1] The LTC7050A is specified over the –40°C to 125°C operating junction temperature range. High Junction temperatures degrade operating lifetimes. Note the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$ in °C) and power dissipation ($P_D$, in Watts) according to the formula:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where $\theta_{JA}$ (in °C/W) is the package thermal impedance.

[2] The LTC7050 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

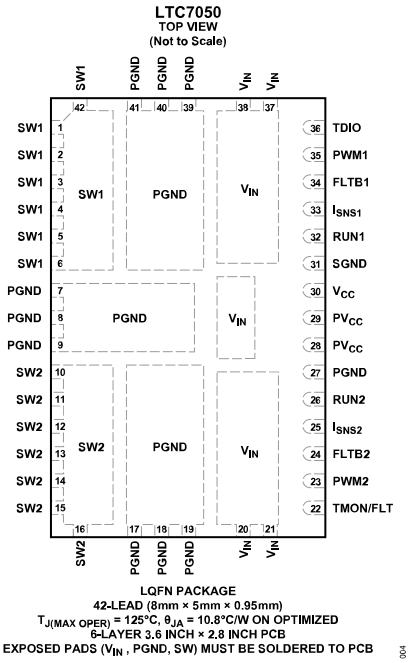



*Figure 3. Pin Configuration*

*Table 3. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 to 6, 10 to 15 | SW1, SW2 | Power Stage Switch Node. The output of the power stage, this node is connected to $V_{IN}$ through the high side N-channel FET and to PGND through the low side N-channel FET. |
| 7, 8, 9, 17, 18, 19, 27, 39, 40, 41 | PGND | Power Stage Ground. This pin is connected to SW through the low side N-channel FET. Also powers the drivers. |
| 20, 21, 37, 38 | $V_{IN}$ | Power Stage Supply. This pin is connected to SW through the high side N-channel FET. |
| 22 | TMON/FLT | Temperature Monitor/Fault Pin. This pin provides a voltage, referred to SGND, of 0.6 V to 1.8 V corresponding to die temperature of 0°C to 150°C for a gain of 8 mV/°C. Above 150°C, the pin is pulled high to indicate an overtemperature (OT) fault. The pin has limited current sinking capability, so multiple like pins can be tied together for highest temperature and single-OT-fault reporting. |
| 23, 35 | PWM2, PWM1 | PWM Input Pin. With RUN driven high, SW will nominally follow this pin high, low, and high-Z. Nominal 3 V CMOS logic levels; can be driven with 3 V to 5 V CMOS signals. Resistor divider holds voltage at 1.7 V when in high-Z state. |
| 24, 34 | FLTB2, FLTB1 | Fault Bar Pin. This open-drain pin pulls down when the chip/channel encounters a fault condition such as OC or OCN. |
| 25, 33 | $I_{SNS2}$, $I_{SNS1}$ | Current Sense Pin. This pin sources/sinks instantaneous current equal to 1/100,000 the SW node current, positive and negative. |
| 26, 32 | RUN2, RUN1 | When this pin is driven high, the channel is enabled. SW node is in high-Z state when RUN is low. |
| 28, 29 | $PV_{CC}$ | 5 V Driver Supply. This pin powers the low side gate driver directly and the high side gate driver through an internal bootstrapped supply riding on SW. Bypass this pin with a 10 µF ceramic capacitor to PGND in close proximity to chip. |
| 30 | $V_{CC}$ | 5 V Supply. Bypass this pin with a 1 µF ceramic capacitor to SGND in close proximity to chip. |
| 31 | SGND | Circuit Ground. |
| 36 | TDIO | Temperature Diode Pin. This pin provides a reference diode to SGND for use in measuring die temperature. |

## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C, $V_{IN}$ = 12 V, $PV_{CC}$ = $V_{CC}$ = 5 V unless otherwise noted.

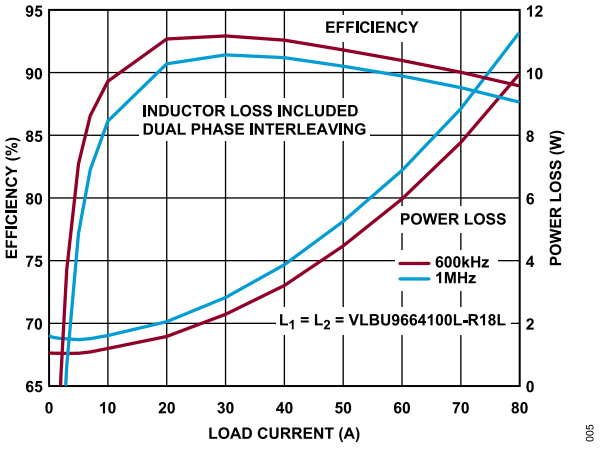



*Figure 4. 12 $V_{IN}$ to 1 $V_{OUT}$ Efficiency*

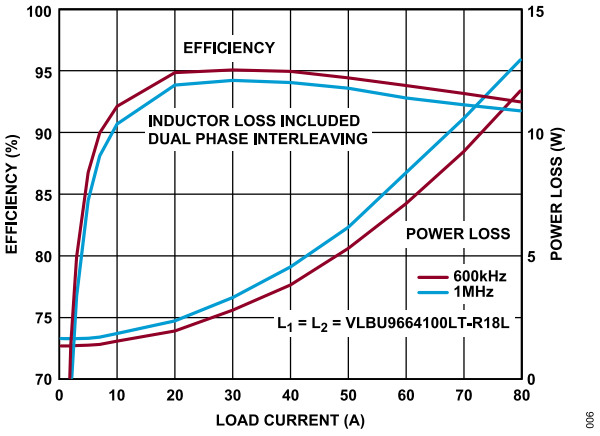



*Figure 5. 12 $V_{IN}$ to 1.8 $V_{OUT}$ Efficiency*

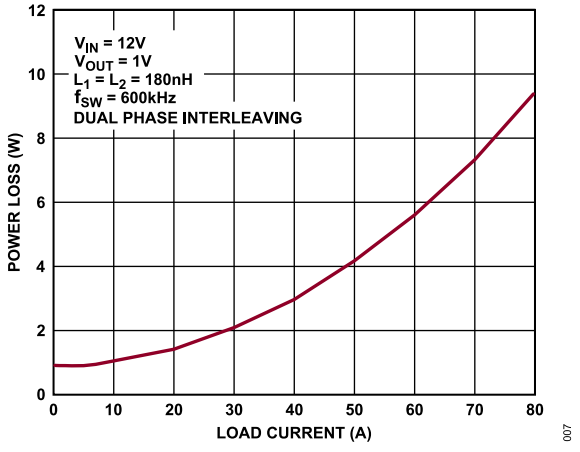



*Figure 6. Power Dissipation vs. Load*

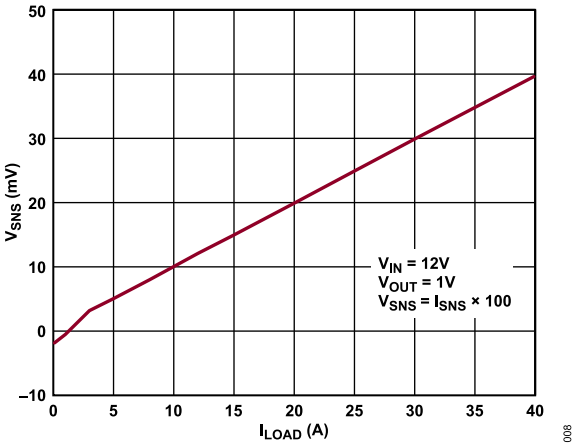



*Figure 7. $V_{SNS}$ vs. $I_{LOAD}$*

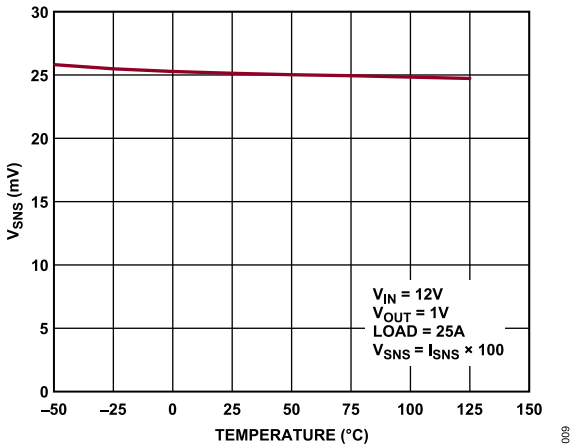



*Figure 8. $V_{SNS}$ vs. Temperature*

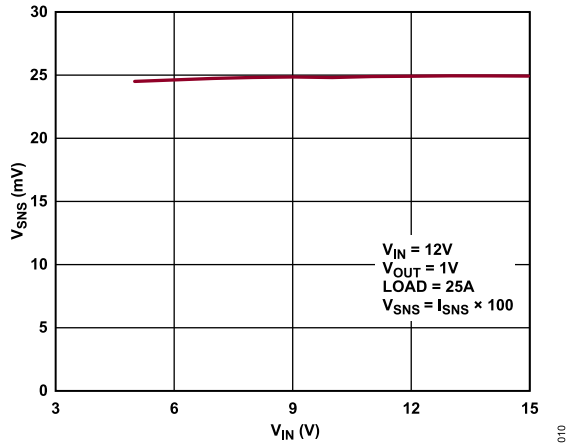



*Figure 9. $V_{SNS}$ vs. $V_{IN}$*

## TYPICAL PERFORMANCE CHARACTERISTICS

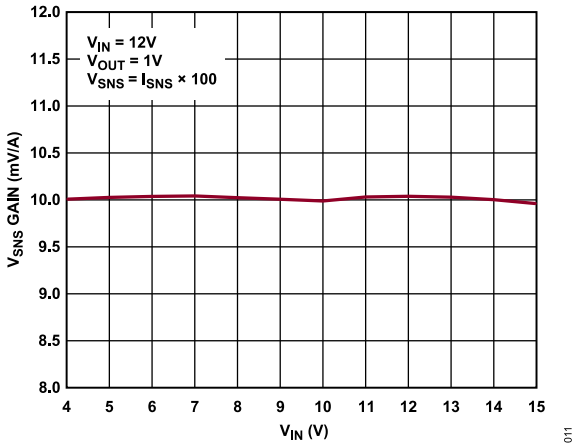



*Figure 10. $V_{SNS}$ Gain vs. $V_{IN}$*

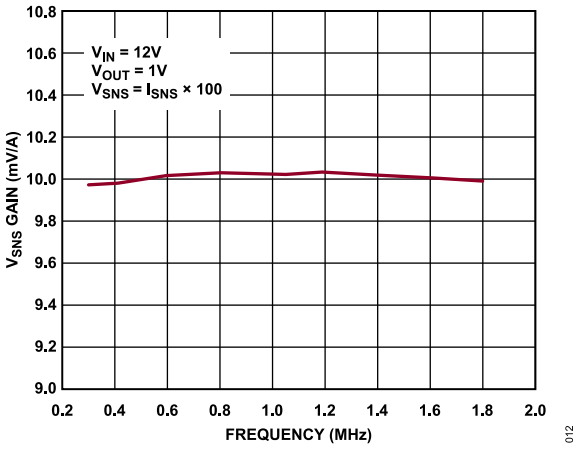



*Figure 11. $V_{SNS}$ Gain vs. Frequency*

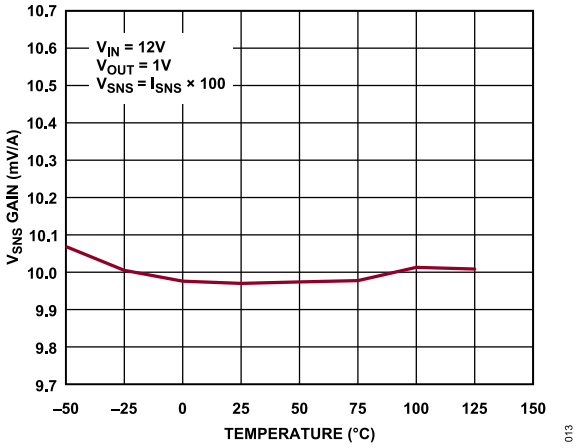



*Figure 12. $V_{SNS}$ Gain vs. Temperature*

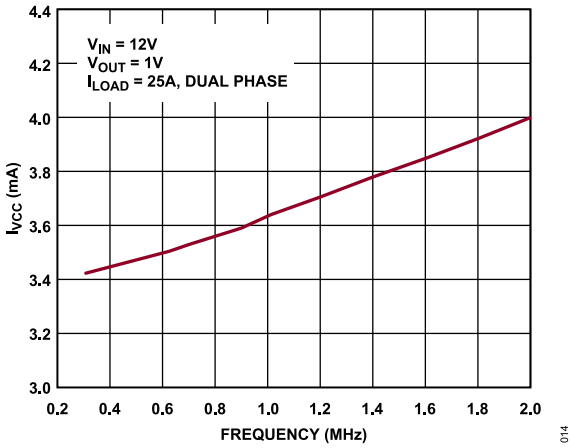



*Figure 13. $I_{VCC}$ vs. Frequency*

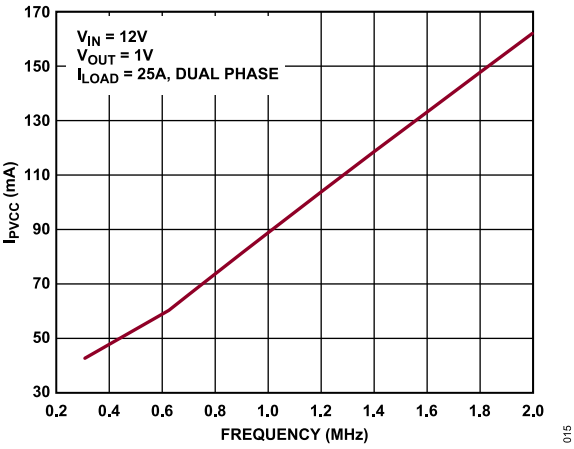



*Figure 14. $IPV_{CC}$ vs. Frequency*

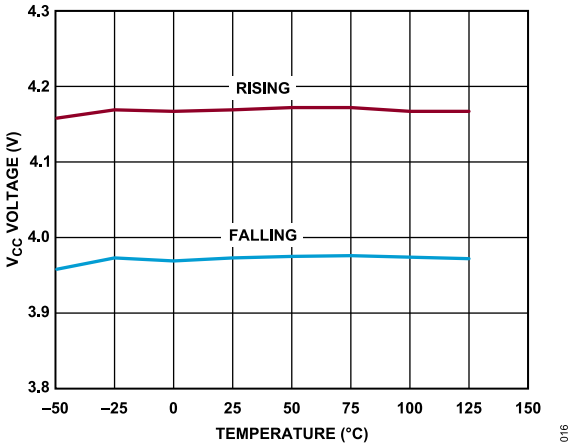



*Figure 15. $V_{CC}$ UVLO vs. Temperature*

## TYPICAL PERFORMANCE CHARACTERISTICS

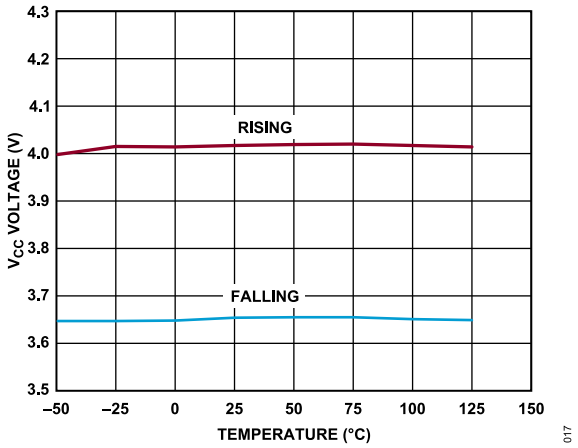



*Figure 16. $PV_{CC}$ UVLO vs. Temperature*

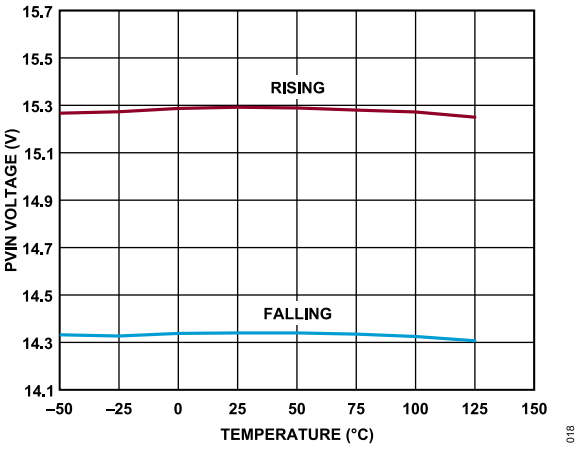



*Figure 17. $PV_{IN}$ OVLO vs. Temperature*

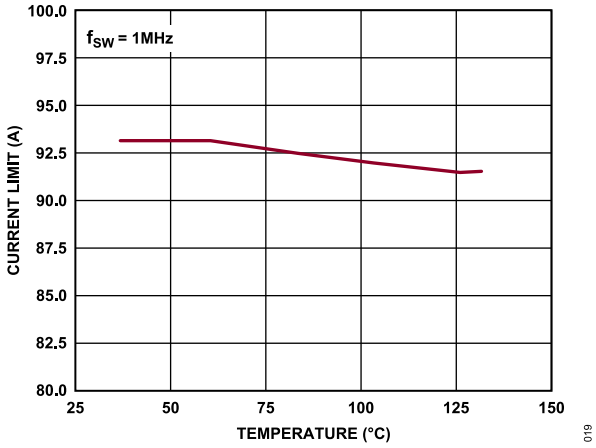



*Figure 18. Current Limit vs. Temperature*

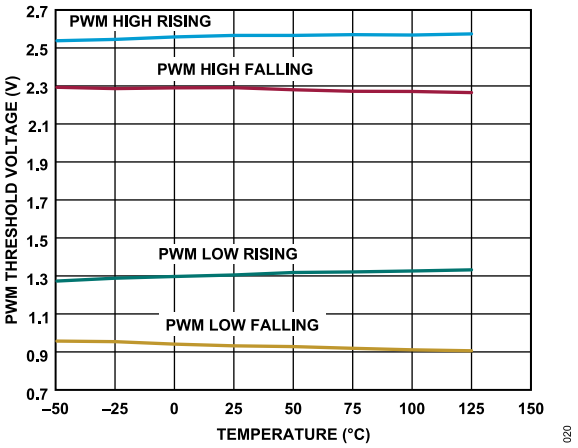



*Figure 19. PWM Threshold vs. Temperature*

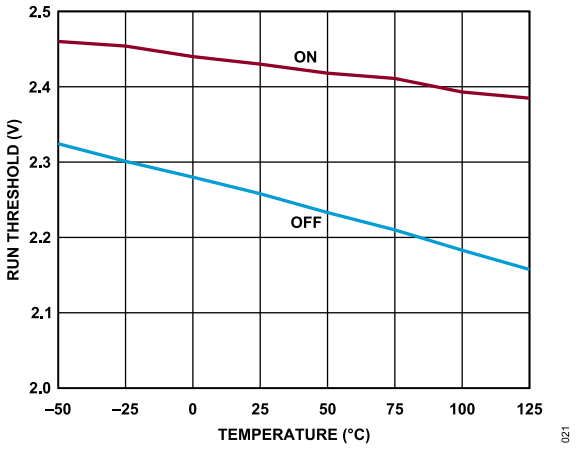



*Figure 20. RUN Threshold vs. Temperature*

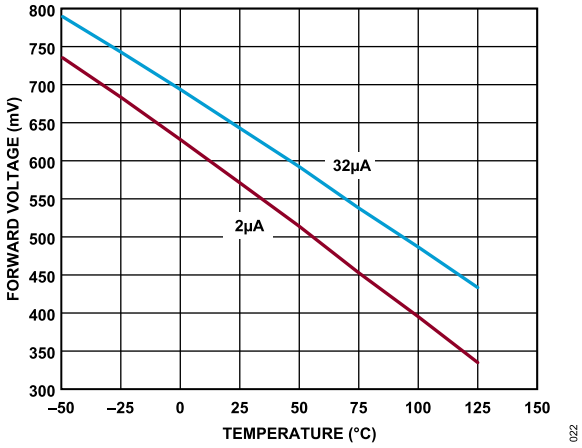



*Figure 21. TDIO Forward Voltage*

## TYPICAL PERFORMANCE CHARACTERISTICS

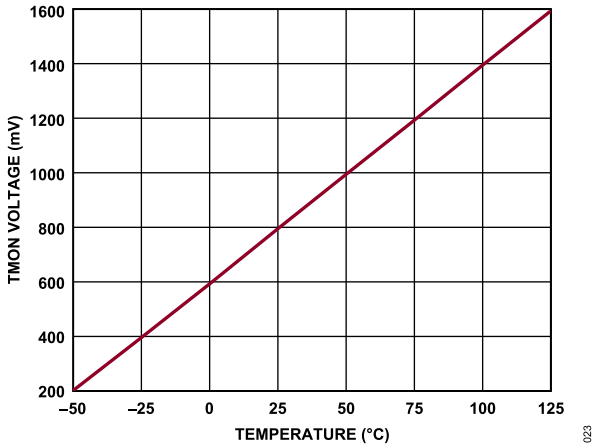



*Figure 22. TMON vs. Temperature*

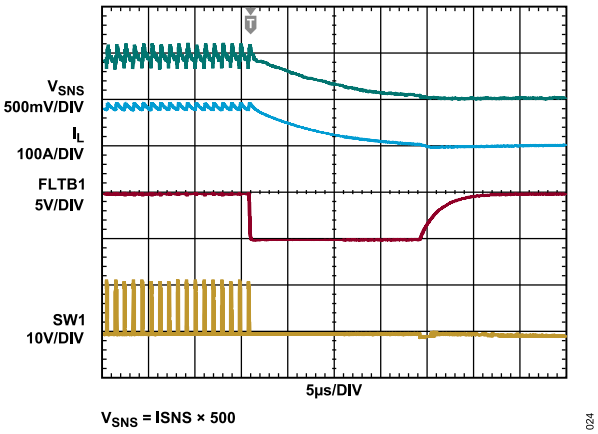



*Figure 23. Overcurrent Protection*

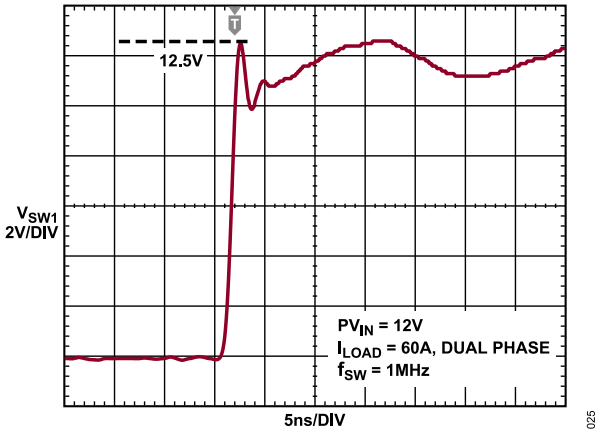



*Figure 24. Switching Rising Edge*

## THEORY OF OPERATION

### MAIN CONTROL ARCHITECTURE

The LTC7050 is a dual-channel or dual-phase integrated-driver half-bridge power MOSFET stage for DC/DC step-down applications. It is designed to be used in a synchronous switching architecture with a logic-level controller providing PWM three-state control outputs. The relationship between the transition thresholds and the three input states of the LTC7050 is illustrated in Figure 25.

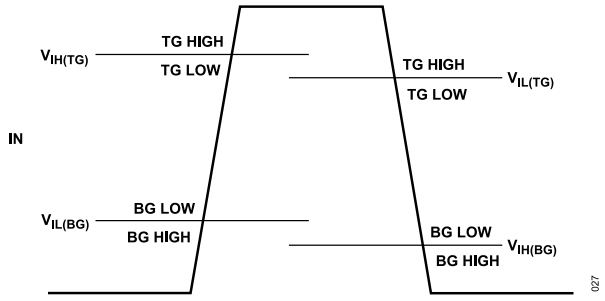



*Figure 25. Three-State Input Operation*

In normal operation, PWMHI turns on the high side FET, and PWMLO turns on the low side FET. SW node follows the PWM pin with a typical 10 ns delay. There is <1 ns dead time before SW rises from PGND to $V_{IN}$ and a typical 3 ns dead time after SW falls.

The high side FET driver is powered from the internal BST node to SW via an internal integrated switch and capacitor, which allows lower dropout than achievable with a typical diode as well as higher-frequency operation.

### CURRENT SENSE

Real-time current sense amplifiers provide a scaled-down version of SW current. During PWMHI or PWMLO, the $I_{SNS}$ pin sources or sinks, according to SW current direction, a current equal to 1/100,000 the instantaneous SW current.

Associated current comparators flag high side FET positive overcurrent (OC) and low side FET negative overcurrent (OCN) conditions. Zero-current of both FETs are also detected by associated current comparators.

### TEMPERATURE MONITOR AND OVERTEMPERATURE FAULT

Normally, TMON outputs a voltage from 0.6 V to 1.8 V, corresponding to a die temperature range of 0°C to 150°C. The TMON voltage is calculated by:

$$V_{TMON}\,(V) = 800\ mV + (T_J\,(°C) - 25°C) \times (8\ mV/°C) \quad (2)$$

Figure 26 illustrates the relationship between $V_{TMON}$ and die temperature.

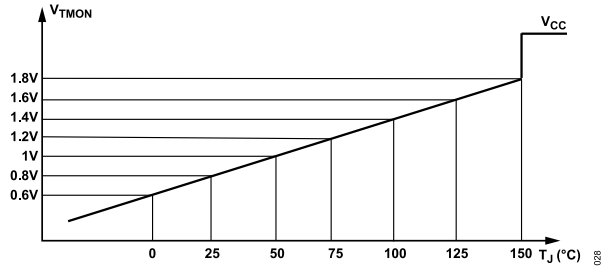



*Figure 26. $V_{TMON}$ vs. Die Temperature*

TMON is driven by an amplifier that can source current but has limited sinking capacity. This allows multiple TMON pins to be paralleled, with the highest temperature being reported. Overtemperature is triggered at 150°C (typical), and it causes the TMON pin to be pulled high to $V_{CC}$. The overtemperature fault will be cleared once the internal temperature falls 20°C (typical) below the threshold.

TDIO pin is internally connected to the anode of a P/N junction diode while the cathode is connected to SGND. It provides an alternative measurement of die temperature for the controllers, such as LTC3884-1, to measure the die temperature using direct $V_{BE}$ method or $\Delta V_{BE}$ method.

### VOLTAGE FAULT CONDITIONS

When $V_{CC}$ or $PV_{CC}$ is in UVLO, or $V_{IN}$ is in OVLO, SW will not respond to PWM and both top FET and bottom FET are off.

When BST-to-SW voltage is in UVLO, SW will not respond to a PWMHI until a PWMLO is provided such that BST-to-SW voltage is recharged sufficiently.

### OVER CURRENT FAULT CONDITIONS

When the high side FET is on, instantaneous SW current of >93 A (net current flowing out of SW) will trip the overcurrent (OC) comparator and set the internal OC state. When this happens, regardless of PWM pin state, the high side FET will be turned off, and the low side FET will be turned on until SW current decreases to 5 A, at which point OC state will be reset. Normal PWMHI-to-high-side-FET and PWMLO-to-low-side-FET operation resumes.

When the low side FET is on, instantaneous SW current of <–45 A (net current flowing into SW) will trip the OCN comparator. When this happens, regardless of PWM pin state, the low side FET will be turned off and the high side FET will be turned on until SW current increases to –8 A, at which point OCN state will be reset. Normal PWMHI-to-high-side-FET and PWMLO-to-low-side-FET operation resumes. The trigger and reset of over current condition are illustrated in Figure 27.

In either OC or OCN condition, FLTB is pulled down.

## THEORY OF OPERATION

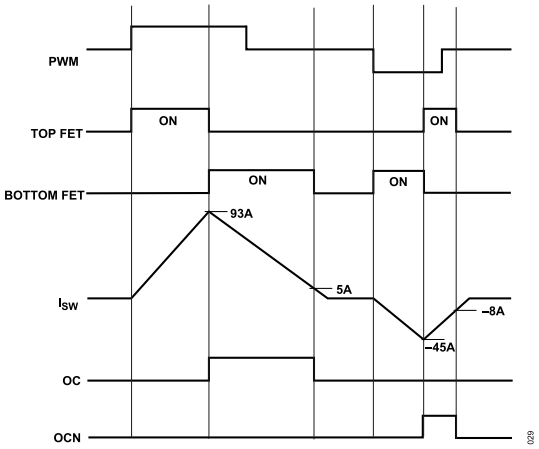



*Figure 27. Over Current Conditions*

### ACTIVE DIODE MODE

If PWM goes from high to Hi-Z state while large (>5 A) currents are still flowing through the top FET from $V_{IN}$ to SW, the top FET will turn off and the bottom FET will turn on to freewheel the current until it has been ramped down. If PWM goes from high to Hi-Z state while large (≥8 A) currents are still flowing through the top FET from SW to $V_{IN}$, the top FET will not turn off until the current has been ramped down.

Similarly, if PWM goes from low to Hi-Z state while large (≥8 A) currents are still flowing through the bottom FET from SW to PGND, the bottom FET will turn off, and the top FET will turn on to freewheel the current until it has been ramped down. If PWM goes from low to Hi-Z state while large (>5 A) currents are still flowing through the bottom FET from PGND to SW, the bottom FET will not turn off until the current has been ramped down.

## APPLICATIONS INFORMATION

### POWER SEQUENCE

LTC7050 requires the following input signals to operate normally: $V_{IN}$, $V_{CC}/PV_{CC}$, RUN, and PWM. Make sure that $V_{IN}$ and $V_{CC}/PV_{CC}$ are present and the RUN pin of LTC7050 is pulled up before enabling the PWM controller. Do not force RUN pin voltages above $V_{CC}$ voltage.

### FAULT MANAGEMENT

The fault management and shutdown mode of LTC7050 is summarized in Table 4. Connecting the open-drain output FLTB pin to the controller's RUN pin can prevent the controller from starting up and force the converter to restart once the LTC7050 runs into fault conditions, except BST-to-SW undervoltage fault.

***Table 4. Fault Management and Shutdown Mode Summary***

| | FLTB | Respond to PWM | TMON |
|---|---|---|---|
| $V_{IN}$ OVLO | Low | No, Both FETs Off Until $I_{SW}$ = 0 | Report Temperature |
| $V_{CC}$ UVLO | Low | No, Immediate Off | Floating |
| $PV_{CC}$ UVLO | Low | No, FETs Off Until $I_{SW}$ = 0. | Report Temperature |
| Positive OC | Low | No, Top FET Immediate Off | Report Temperature |
| Negative OC | Low | No, Bottom FET Immediate Off | Report Temperature |
| Overtemperature | Low | Yes | Pull Up to $V_{CC}$. |
| BST-to-SW UV | High | Ignore PWMHI | Report Temperature |
| RUN Shutdown | Low | No, Both FETs Off | Floating |

### CURRENT SENSE AND CURRENT LIMIT

$I_{SNS}$ sources and sinks a current which is 1/100,000 of the SW current. According to the controller's maximum current sense signal range, select a proper resistor to convert the $I_{SNS}$ current into a differential voltage signal reflecting the real-time SW current. The resistor should be biased at a low impedance common mode voltage, which has current sinking and sourcing capability. Make sure that at the maximum positive current and negative current, the $I_{SNS}$ pin voltage is in the specified range so that the gain $I_{SNS}/I_{SW}$ remains constant.

A general LTC7050 application circuit is shown on the first page of this data sheet. LTC7050 is optimized for the application of high frequency high current voltage regulator. External component selection is largely driven by the load requirement and begins with the selection of the switching frequency $f_{SW}$ and inductor L. Refer to Frequency Selection section and Inductor Selection section for the guidance. The $I_{SNS}$ resistors are selected to set the current limit.

In high frequency high current applications, the switching spikes coupled to the $I_{SNS}$ signal may result in a reading offset in heavy load range, but does not impact the $\Delta I_{SNS}/\Delta I_{SW}$ gain. An optional resistor between $I_{SNS}$ pin to GND can mitigate the offset. The resistor value ROS is calculated by $I_{SNS}$ pin voltage (referring to GND) divided by the offset current observed. The resistor value may be different for a different switching frequency. This modification does not impact the internal overcurrent protection and negative overcurrent protection.

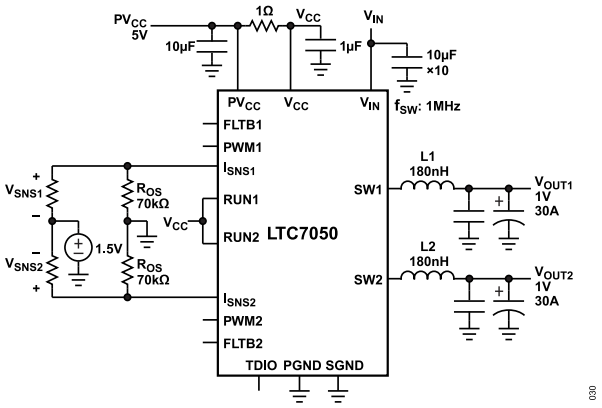



*Figure 28.*

### FREQUENCY SELECTION

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing FET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. In the selection of switching frequency, make sure that the high side on-time at maximum input voltage is longer than LTC7050's minimum on-time, $t_{ON(MIN)}$, which is the smallest time duration that the LTC7050 is capable of turning on the top FET. It is determined by internal timing delays, power stage timing delays and the gate charge required to turn on the top FET. Low duty cycle applications may approach this minimum on-time limit (see Equation 3).

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (3)$$

### INPUT CAPACITORS

The LTC7050 should be connected to a $V_{IN}$ supply through low impedance power planes. Ceramic input capacitors should be placed as close to the package as physically possible, with size and quantity appropriate for temperature rise with ripple current as calculated below.

For a buck converter, the switching duty cycle can be estimated by Equation 4.

$$D = \frac{V_{OUT}}{V_{IN}} \quad (4)$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated by Equation 5.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta} \times \sqrt{D \times (1 - D)} \quad (5)$$

where η is the estimated efficiency of the power section.

### INDUCTOR SELECTION

Given the desired input and output voltages, the inductor value and operating frequency, $f_{SW}$, directly determine the inductor's peak-to-peak ripple current (Equation 6).

## APPLICATIONS INFORMATION

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times L}\right) \quad (6)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to Equation 7.

$$L \geq \left(\frac{V_{IN} - V_{OUT}}{f_{SW} \times I_{RIPPLE}}\right) \times \frac{V_{OUT}}{V_{IN}} \quad (7)$$

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

### OUTPUT CAPACITORS

The LTC7050 is designed for high frequency switching and low output voltage ripple noise. The bulk output capacitors defined as $C_{OUT}$ are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. $C_{OUT}$ can be a low ESR tantalum capacitor, a low ESR polymer capacitor, or ceramic capacitors. At 1 MHz, the typical output capacitance range is from 500 µF to 1000 µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required.

### BYPASSING AND GROUNDING

The LTC7050 requires proper bypassing on the $PV_{CC}$ and $V_{CC}$ supplies due to its high speed switching (nanoseconds) and large AC currents (amperes). Careless component placement and PCB trace routing may cause excessive ringing and under/overshoot. Follow the following steps to obtain the optimum performance from the LTC7050.

- Mount the bypass capacitors as close as possible between the $V_{CC}$ and SGND pins, and the $PV_{CC}$ and PGND pins. The traces should be shortened as much as possible to reduce lead inductance.
- Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Any significant ground drop will degrade signal integrity.
- Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the input pin and the output power stage.
- Be sure to solder the Exposed Pad on the back side of the LTC7050 packages to the board. Failure to make good thermal contact between the exposed back side and the copper board will result in far greater thermal resistances.

### PCB LAYOUT

Due to the LTC7050's high power density and high speed, high frequency operation, proper PCB layout and composition are critical to maximizing performance.

At a minimum, the PCB should be 4-layer with at least top and bottom layers 2 oz. copper. As much as possible, top and bottom layers should be continuous $V_{IN}$ and PGND areas. At least one inner layer, preferably the second, should be a continuous PGND plane.

Copper-filled vias should be used under the package exposed pads to connect top and bottom PCB layers. $\theta_{JCbottom}$ is <1°C/W. Anything less than copper-filled vias will compromise $\theta_{JA}$ greatly.

The inductor pads should be placed as close as possible to the package, with traces as short and wide as possible. If possible, SW traces should be doubled up with the second layer, taking care not to couple to sensitive traces.

A recommended PCB layout is shown in Figure 30.

## APPLICATIONS INFORMATION

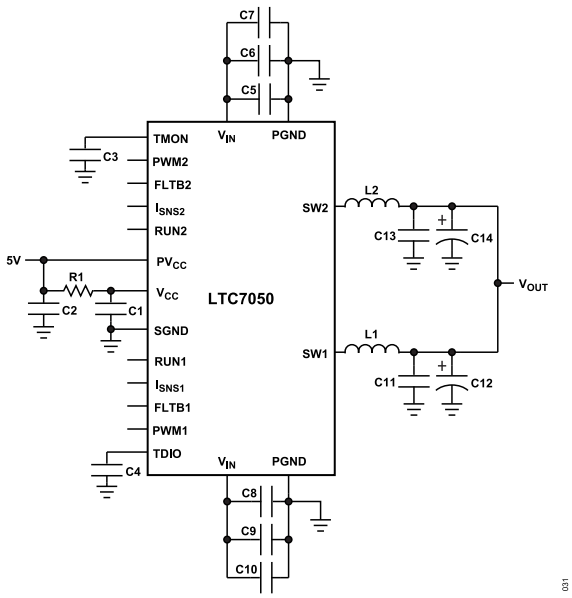



*Figure 29. Schematic*

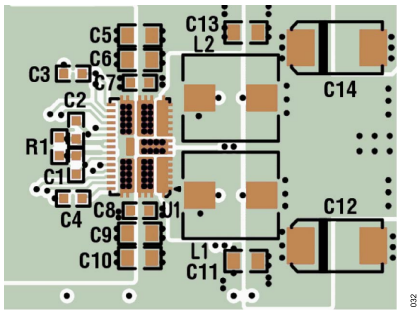



*Figure 30. Example PCB Layout*

## APPLICATIONS INFORMATION

### TYPICAL APPLICATIONS

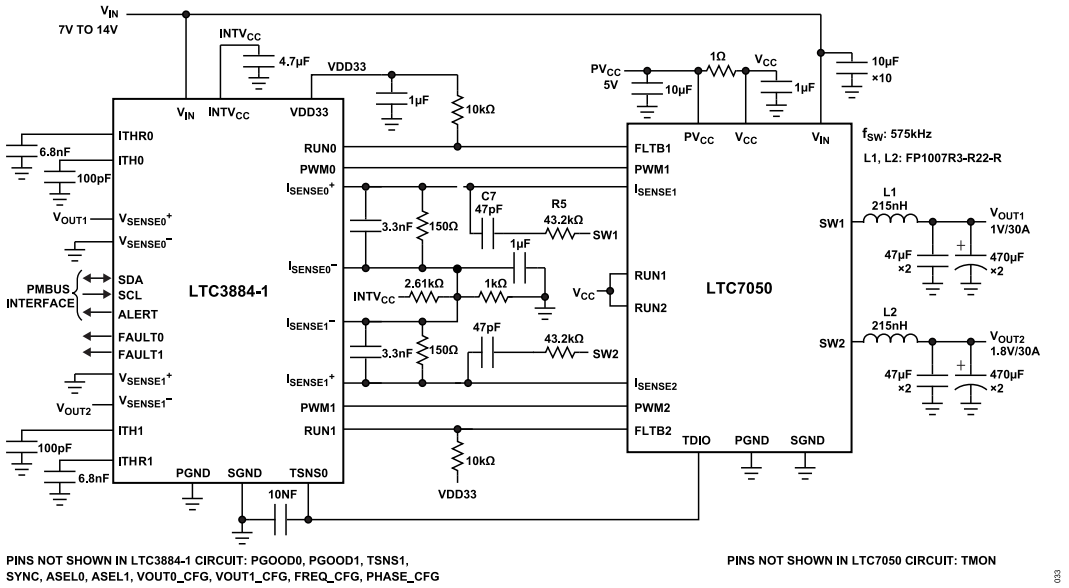
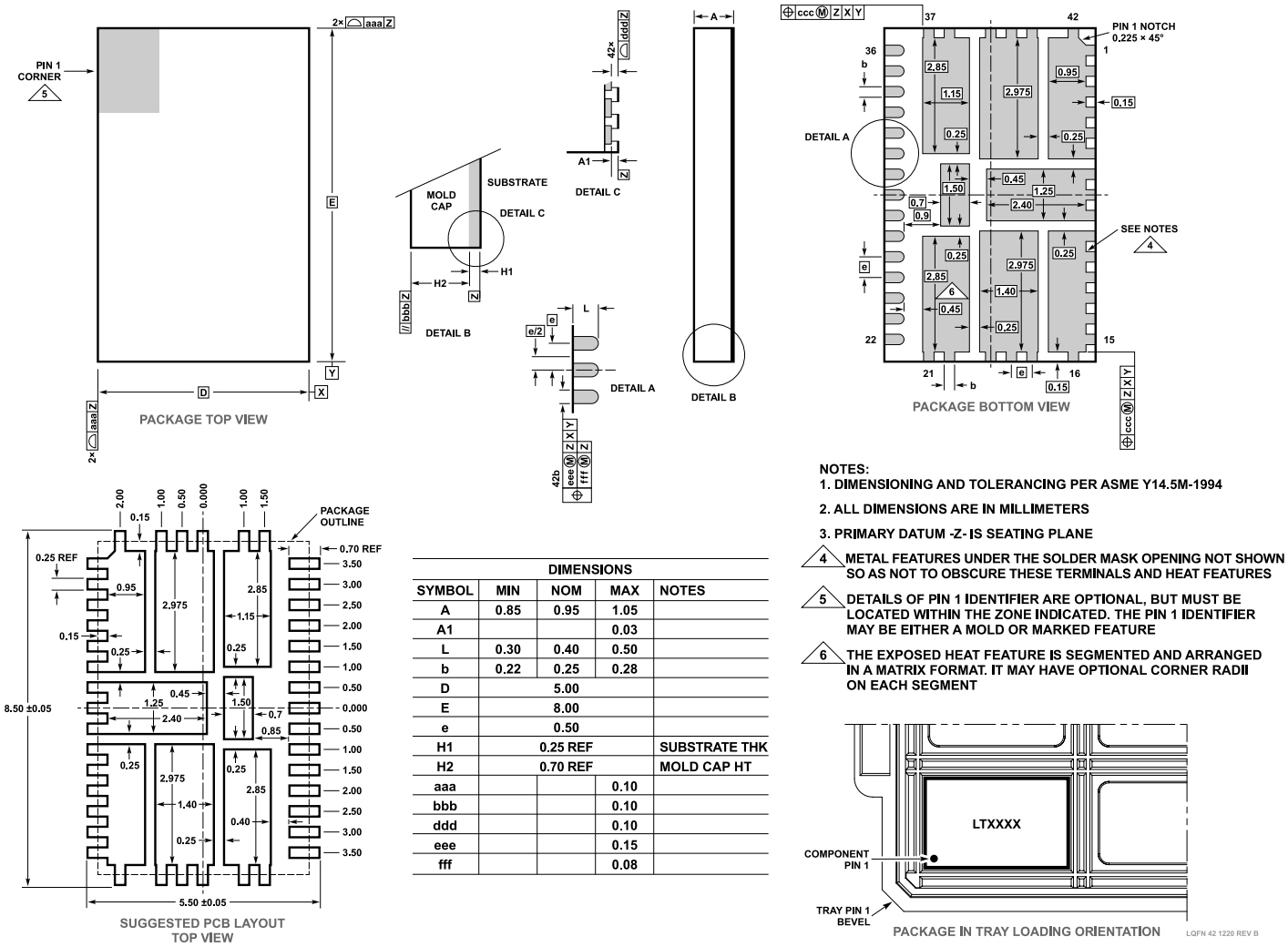



*Figure 31. LTC7050 and LTC3884-1 Schematic*

## Related Parts

| Part Number | Description | Comments |
|---|---|---|
| LTC7051 | SilentMOS Smart Power Stage in 5 mm × 8 mm LQFN | 140 A Peak Current, Silent Switcher 2 Architecture, $V_{IN}$ Up to 14 V, 5 mm × 8 mm LQFN Package |
| LTC7050-1 | Dual SilentMOS Smart Power Stage in 5 mm × 8 mm LQFN | 70 A Peak Current per Channel, Silent Switcher 2 Architecture, $V_{IN}$ Up to 16 V, 5 mm × 8 mm LQFN Package |
| LTC7051-1 | SilentMOS Smart Power Stage in 5 mm × 8 mm LQFN | 140 A Peak Current, Silent Switcher 2 Architecture, $V_{IN}$ Up to 16 V, 5 mm × 8 mm LQFN Package |
| LTC3888/LTC3888-1 | Dual Output 8-Phase Step-Down DC/DC Controller with Digital Power System Management | 4.5 V ≤ $V_{IN}$ ≤ 26.5 V, 0.3 V ≤ $V_{OUT}$ ≤ 3.45 V, $I^2C$/PMBus Control, Programmable Loop Compensation, 5 mm × 8 mm QFN-52 |
| LTC3884/LTC3884-1 | Dual Output PolyPhase® Step-Down Controller with Sub-Milliohm DCR Sensing and Digital Power System Management | 4.5 V ≤ $V_{IN}$ ≤ 38 V, 0.5 V ≤ $V_{OUT}$ ≤ 5.5 V, $I^2C$/PMBus Control, Programmable Loop Compensation, 5 mm × 8 mm QFN-52 |
| LTC7851 | Quad Output Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing | Operates with DrMOS, Power Blocks or External Drivers/MOSFETs, $V_{IN}$ Range Depends on External Components, 4.5 V≤ $V_{CC}$ ≤ 5.5 V, 0.6 V ≤ $V_{OUT}$ ≤ $V_{CC}$ –0.5 V |
| LTC7852/LTC7852-1 | Dual Output 6-Phase Current Mode Synchronous Buck Controller with Current Monitoring | Operates with DrMOS, Power Blocks, 0.5 V ≤ $V_{OUT}$ ≤ 2 V, Hiccup Mode Overcurrent Protection, Flexible Phase Configuration |
| LTC3861 | Dual, Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing | Operates with Power Blocks, DrMOS or External MOSFETs 3 V≤ $V_{IN}$ ≤ 24 V |
| LTC3882/LTC3882-1 | Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller with Digital Power System Management | 3 V ≤ $V_{IN}$ ≤ 38 V, 0.5 V ≤ $V_{OUT1,2}$ ≤ 5.25 V, ±0.5% $V_{OUT}$ Accuracy $I^2C$/PMBus Interface, uses DrMOS or Power Blocks |
| LTC3887/LTC3887-1 | Dual Output Multiphase Step-Down DC/DC Controller with Digital Power System Management, 70mS Start-Up | 4.5 V ≤ $V_{IN}$ ≤ 24 V, 0.5 V ≤ $V_{OUT0,1}$ (±0.5%) ≤ 5.5 V, 70mS Start-Up, $I^2C$/PMBus Interface, –1 Version uses DrMOS or Power Blocks |

## OUTLINE DIMENSIONS




| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 0.85 | 0.95 | 1.05 | |
| A1 | | | 0.03 | |
| L | 0.30 | 0.40 | 0.50 | |
| b | 0.22 | 0.25 | 0.28 | |
| D | | 5.00 | | |
| E | | 8.00 | | |
| e | | 0.50 | | |
| H1 | | 0.25 REF | | SUBSTRATE THK |
| H2 | | 0.70 REF | | MOLD CAP HT |
| aaa | | | 0.10 | |
| bbb | | | 0.10 | |
| ddd | | | 0.10 | |
| eee | | | 0.15 | |
| fff | | | 0.08 | |

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT

LQFN 42 1220 REV B

*Figure 32. 42-Lead, 5 mm × 8 mm × 0.95 mm, LQFN*
*(05-08-1571)*
*Dimensions shown in millimeters*

Updated: May 09, 2023

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| LTC7050AV#PBF | -40°C to +125°C | 42-Lead LQFN (8mm x 5mm x 0.95mm w/ EP) | 05-08-1571 |

[1] Parts ending with PBF are RoHS and WEEE compliant.

## EVALUATION BOARDS

| Model[1] | Description |
|---|---|
| DC2881A-A | Evaluation Board |

[1] DC2881A-A is RoHS compliant.