

DATA SHEET

LTE052T-060
Active matrix 5" color
TFT LCD Module

Product Specification

March 30th 2000

Philips Flat Display Systems

CONTENTS

1	GENERAL DESCRIPTION
2	FEATURES
3	APPLICATIONS
4	QUICK REFERENCE DATA
4.1	Block diagram
5	MECHANICAL DATA
5.1	Dimensions
5.2	Electrical connectors
6	PINNING
7	ELECTRICAL CHARACTERISTICS
7.1	Limiting values
7.2	Recommended operating condition module
7.3	Recommended operating condition backlight
7.4	Characteristics
7.5	Input and output timing
7.5.1	Displayed lines (PAL mode)
7.5.2	Displayed lines (NTSC mode)
7.6	External clock
7.7	Backlight dimming
7.8	Power on/off sequences
8	OPTICAL DATA
8.1	Optical characteristics
8.2	Pixel organization
8.3	Contrast ratio
8.4	Response time
8.5	Viewing angle
9	ENVIRONMENTAL DATA
9.1	Environmental tests
9.2	Mechanical tests
9.3	Electrostatic discharge
9.4	Electromagnetic compatibility (EMC)
9.5	Safety
10	HANDLING AND SAFETY REQUIREMENTS
11	MOUNTING
12	DEFINITIONS

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support applications, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Flat Display Systems customers using or selling these products for use in such applications do so at their own risk and agree to fully identify Philips Flat Display Systems for any damages resulting from such improper use or sale

Active matrix 5" color TFT LCD module**LTE052T-060**

W W W .

1 GENERAL DESCRIPTION

This is an active matrix LCD module
Which comprises

- A 5" color TFT panel
- Panel driver electronics
- Integrated backlight
- Integrated interface card

The 5" active area has full color capability using 320 (xRGB) x 234 pixels. The panel has a 4:3 aspect ratio and a wide viewing angle.

The module can withstand intense
Environmental conditions

Outline dimensions compatible with
double DIN size for automotive use.

2 FEATURES

- RGB stripe configuration
- Two analog RGB with Hsync and Vsync inputs
- Two analog RGB channels with possibility of picture in picture.
- (C) VBS for synchronisation or Hs Vs with CLK signal
- Selectable NTSC/PAL (RGB)
- Up/down and left/right control signals
- Display aspect ratio 4 : 3
- Display resolution 234 lines
- High contrast TFT LCD drive system
- High speed response
- High brightness
- Wide viewing angle
- Integrated high efficiency backlight
- Extended temperature range.

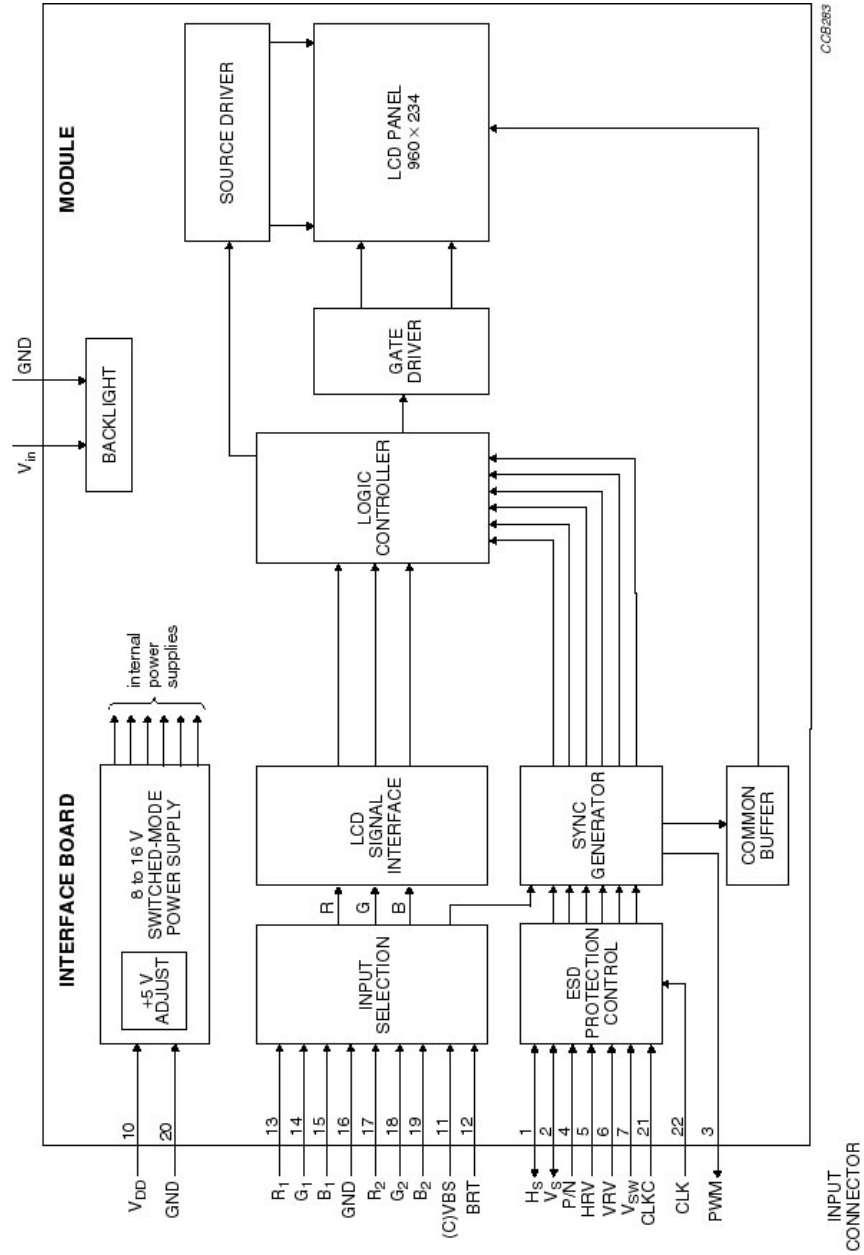
3 APPLICATIONS

- Car navigation
- TV and DVD monitors
- Video games
- Automation and process control monitors.

4 QUICK REFERENCE DATA

PARAMETERS	VALUE	UNIT
Overall dimensions		
Width	126.9	mm
Height	89.6	mm
Depth	13.1	mm
Active area dimensions		
Width	102.70	mm
Height	74.76	mm
Display resolution	320x234	pixels
Pixel dimensions:		
Horizontal	3x0.107	mm
Vertical	0.319	mm
Pixel configuration	RGB stripe	
Supply voltage (module)	8 to 16	Volt
Power consumption (without inverter)	1.2	W
Backlight life at 25C; $I_{lamp} = + 6.0$ mA (RMS) Continuous operation	min. 10000	hours
Typical viewing angle (contrast ratio >5)		
Horizontal right	70	deg
Horizontal left	70	deg
Vertical up	50	deg
Vertical down	70	deg
Maximum operating ambient temperature	70	C
Operating panel surface temperature range	-30 to +85	C
Storage temperature range	-40 to +90	C
Typical response time:		
Rise time	30	ms
Fall time	15	ms
Mass of the module	183 +/- 10	g

4.1 BLOCK DIAGRAM (fig. 1)

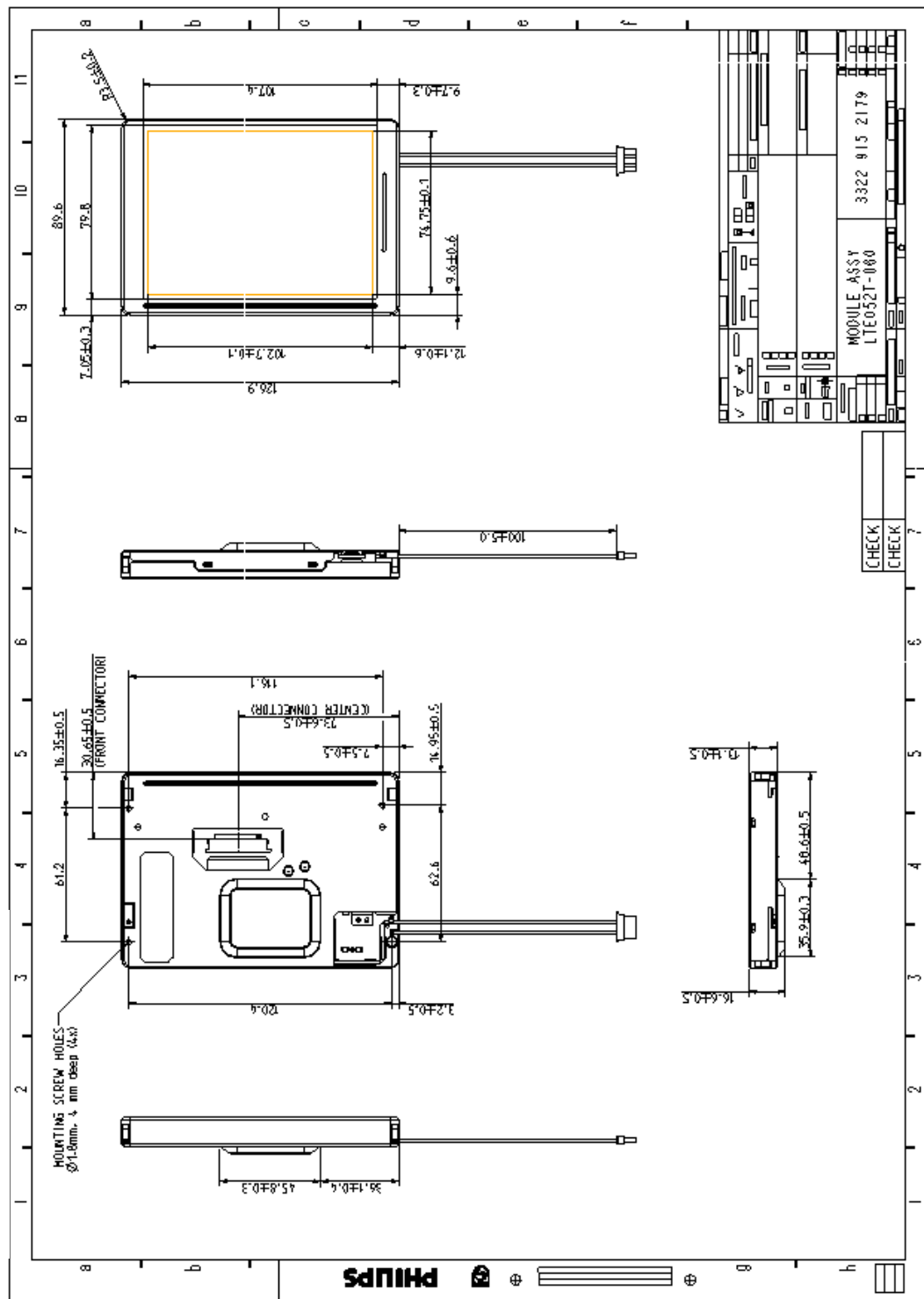


4.1 diagram

Active matrix 5" color TFT LCD module

LTE052T-060

5 MECHANICAL DATA (fig. 2)



Active matrix 5" color TFT LCD module**LTE052T-060**

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5.1 Dimensions

PARAMETER	VALUE	UNIT
Display format	(320x3) x 234	dots
Active area	102.7 x 74.8	mm
Screen size (diagonal)	127 5.0	mm inch
Pixel pitch: Horizontal vertical	3x 0.107 0.319	mm mm
Dot configuration	RGB stripe	
Overall dimensions (excluding connectors) Width Height Depth	126.9 +/- 0.2 89.6 +/- 0.2 13.1 +/- 0.5	mm mm mm
Mass of the module	183 +/- 10	g

5.2 Electrical connectors

SERVICE	NUMBER OF PINS	MATING CONNECTOR
Interface	22	22-pin flex foil (1mm pitch)
Backlight	2	SM02 (8.0)B-BHS 1- TB

6 PINNING

SYMBOL	PIN	I/O	DESCRIPTION
Analog interface			
H _s	1	I/O	Horizontal sync; notes 1 and 2
V _s	2	I/O	Vertical sync; notes 1 and 3
PWM	3	O	Synchronization signal for backlight
P/N	4	I	PAL/NTSC control signal, note 8
HRV	5	I	Horizontal scanning direction; note 4
VRV	6	I	Vertical scanning direction note 5
V _{sw}	7	I	RGB ₁ /RGB ₂ video signal switching; note 6
n.c.	8	-	Not connected
n.c.	9	-	Not connected
V _{DD}	10	I	Supply voltage
VBS	11	I	VBS input for sync separator
BRT	12	I	Brightness control
R ₁	13	I	Red video signal 1
G ₁	14	I	Green video signal 1
B ₁	15	I	Blue video signal 1
n.c.	16	-	Not connected
R ₂	17	I	Red video signal 2
G ₂	18	I	Green video signal 2
B ₂	19	I	Blue video signal 2
GND	20	I	Ground
CLKC	21	I	Change I/O direction of CLK, H _s and V _s ; note 7
CLK	22	I	Clock signal
Backlight			
V _{in}	1	I	Backlight input voltage
GND	2	I	Backlight ground connection

NOTES

- 1 CLKC= LOW: module is activated by CLK, H_s and H_s.
- 2 CLKC = HIGH: H_s is output, synchronised to VBS signal
CLKC = LOW: H_s is horizontal sync input.
- 3 CLKC = HIGH: V_s is output, synchronised to VBS signal
CLKC = LOW: V_s is vertical sync input.
- 4 HRV = HIGH: image is normal
HRV = LOW: image is reversed into horizontal direction.
- 5 VRV = HIGH: image is normal
VRV = LOW: image is reversed into vertical direction.
- 6 V_{sw} = HIGH: RGB1 is selected
V_{sw} = LOW: RGB2 is selected
- 7 CLKC = HIGH : H_s and V_s become output mode
CLKC = LOW: CLK, H_s and V_s become input mode
- 8 P/N switching when not operating

7 ELECTRICAL CHARACTERISTICS**7.1 Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134)

T_{amb} = 25 C.; GND = 0V; unless otherwise stated

SYMBOL	DESCRIPTION	MIN>	MAX.	UNIT
V _{dd}	Power supply voltage (pin 10)	-0.3	20	V
V _i (analog)	Analog input voltage (peak to peak value)	-0.3	5	V
V _i (dig)	Digital input voltage	-0.3	5	V
V _o (dig)	Digital output voltage	-0.3	5.3	V

7.2 Recommended operating conditions module

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP	MAX	UNIT
V _{DD}	Power supply ; note 1	Within 200 ms	7.8	12.0	16.0	V
V _{DD} , ripple	Ripple on supply voltage	Freq. > 400 Hz			0.1	V
V _{i(a)}	Analog input voltage:note 2 AC component (peak-to-peak value): - AC component video content (peak-to peak value), note 3 - DC component		0.7 - -1.0	1.0 0.7 0	2.0 - +1.0	V V V
BRT	Brightness control		0		5.0	V
f _{Hs}	VBS horizontal sync frequency NTSC PAL	CLKC=HIGH	15.13 15.03	15.73 15.63	16.33 16.23	kHz kHz
t _w (Hs)	VBS horizontal sync pulse width NTSC PAL	CLKC=HIGH	4.2 4.2	4.7 4.7	5.2 5.2	μs μs
t _r (Hs), t _f (Hs)	VBS horizontal sync pulse rise and fall times	CLKC=HIGH	-	-	0.5	μs
f _{Vs}	Vertical sync frequency NTSC	CLKC=HIGH	f _H /284	f _H /262	f _H /258	Hz

Active matrix 5" color TFT LCD module

LTE052T-060

	PAL		$f_H/344$	$f_H/312$	$f_H/304$	Hz
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$T_{w(Vs)}$	Vertical sync. Pulse width NTSC PAL	CLKC = HIGH	- -	3H 2.5H	- -	
$T_{r(Vs)}, t_{f(Vs)}$	Vertical sync pulse rise and fall times	CLKC = HIGH	-	-	0.5	μs
F_{clk}	Input clock frequency	CLKC = LOW	6.0	6.8	7.6	MHz
T_{wh}	Input clock pulse width HIGH	CLKC = LOW	20	-	-	ns
T_{wl}	Input clock pulse width LOW	CLKC = LOW	20	-	-	ns
$T_{r(clk)}$	Input clock rise time	CLKC = LOW	-	-	10	ns
$T_{f(clk)}$	Input clock fall time	CLKC = LOW	-	-	10	ns
F_{Hs}	HSY input frequency	CLKC = LOW	$f_{clk}/465$	$f_{clk}/435$	$f_{clk}/405$	kHz
$T_{w(Hs)}$	HSY input pulse width	CLKC = LOW	1	5	9	μs
$T_{r(Hs)}, t_{f(Hs)}$	HSY input pulse rise and fall times	CLKC = LOW	-	-	0.05	μs
F_{Vs}	VSY input frequency	CLKC = LOW	50	$F_{Hs}/2$ 62	$F_{Hs}/258$	Hz
$T_{w(Vs)}$	VSY input pulse width	CLKC = LOW	1H	3H	5H	
t_{su1}	VSY to HSY set-up time	CLKC = LOW	1.0	-	-	μs
t_{HO1}	VSY to HSY hold time	CLKC = LOW	1.0	-	-	μs
t_{su2}	CLK to HSY set-up time	CLKC = LOW	25	-	-	ns
t_{HO2}	CLK to HSY hold time	CLKC = LOW	25	-	-	ns

NOTES

- 1 The module does not have load dump, under or over-voltage protection.
- 2 Applies to VBS input
- 3 Applies to VR₁, VG₁, VB₁, VR₂, VG₂, and VB₂.

7.3 Recommended operating conditions backlight

T_{amb} = -30 to +85 C; relative humidity < 90% at 60 C.

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP	MAX	UNIT
$V_{L(rms)}$	CCFL tube voltage (RMS value)	Il(rms) = 6 mA	530	580	630	V
$I_{L(rms)}$	CCFL tube current (RMS Value)	Normal operation	5.5	6.0	6.5	mA
f_L	CCFL drive frequency		20	-	70	kHz
$V_{IGS(rms)}$	Ignition voltage (RMS value): Tamb = 25 C Tamb = -30 C		- -	1000 -	- 1700	V V

7.4 Characteristics

GND = 0 V; $T_{amb} = -30$ to $+70$ °C; unless otherwise stated.

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H_S, V_S, CLK, V_{SW}						
V _{IH}	HIGH-level input voltage		3.5			V
V _{IL}	LOW-level input voltage				1.5	V
P/N, VRV, CLKC, HRV						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
H_S, V_S, PWM						
V _{OH}	HIGH-level output voltage	I _{OH} = -4 mA	2.4			V
V _{OL}	LOW-level output voltage	I _{OL} = +4 mA			0.4	V
CLK see note 1						
V _{OL}	LOW-level output voltage	I _{OL} = +4 mA			0.4	V
CLK, HRV						
I _{IH}	HIGH-level input current	V _I = +5 V	-0.1		+0.1	μA
I _{IL}	LOW-level input current	V _I = 0 V			-4.5	μA
H_S, P/N, V_S, VRV, CLKC						
I _{IH}	HIGH-level input current	V _I = +5 V			+10	μA
I _{IL}	LOW-level input current	V _I = 0 V			-200	μA
VSW						
I _{IH}	HIGH-level input current	V _I = +5 V			+10	μA
	LOW-level input current	V _I = 0 V			-600	μA
R₁, G₁, B₁, R₂, G₂, B₂, V_{SW}, VBS						
C _i	input capacitance	f = 1 MHz		28		pF
P/N, HRV, VRV, CLK, PWM, H_S, V_S						
C _i	input capacitance	f = 1 MHz		37		pF
CLKC						
C _i	input capacitance	f = 1 MHz		10		nF

NOTE

1 At CLKC = HIGH, CLK = zero (internal clock mode)

7.5 Input and output timing

SYMBOL	DESCRIPTION	CONDITIONS	TYP.	UNIT
t_{field}	field period:			
	NTSC	$f_{\text{field}}=60\text{Hz}$	16.67	ms
	PAL	$f_{\text{field}}=50\text{Hz}$	20.0	ms
t_{line}	line period:			
	NTSC		63.5	μs
	PAL		64.0	μs
f_{line}	line frequency:			
	NTSC		15.73	kHz
	PAL		15.625	kHz
t_{DV1}	V_S delay field 1		1H	
t_{DV2}	V_S delay field 2		H/2	
t_{VO}	vertical pulse width		4H	
t_{VID}	video signal on-display time		50.1	μs
$t_{\text{d(disp)}}$	sync edge to start display delay time:			
	NTSC		10.6	μs
	PAL		11.1	μs
$t_{\text{pd(HS)}}$	sync edge to H_S delay time	50% level	1.4	μs
t_{HO}	horizontal pulse width	50% level	1.2	μs

7.5.1 DISPLAYED LINES (PAL MODE)

Field 1 displayed line numbers:
27 to 298

Field 2 displayed lines numbers:
339 to 611

In PAL, on average, every seventh line is skipped.

Actual lines skipped in field 1:
34 + 14N where N = 0,1 to 18 and
40 + 14M where M = 0,1 to 18.

Actual lines skipped in field 2
344 + 14N where N = 0,1 to 18 and
350 + 14M where M = 0,1 to 18.

7.5.2 DISPLAYED LINES (NTSC MODE)

Field 1 displayed line numbers:
23 to 256

Field 2 displayed lines numbers:
286 to 519

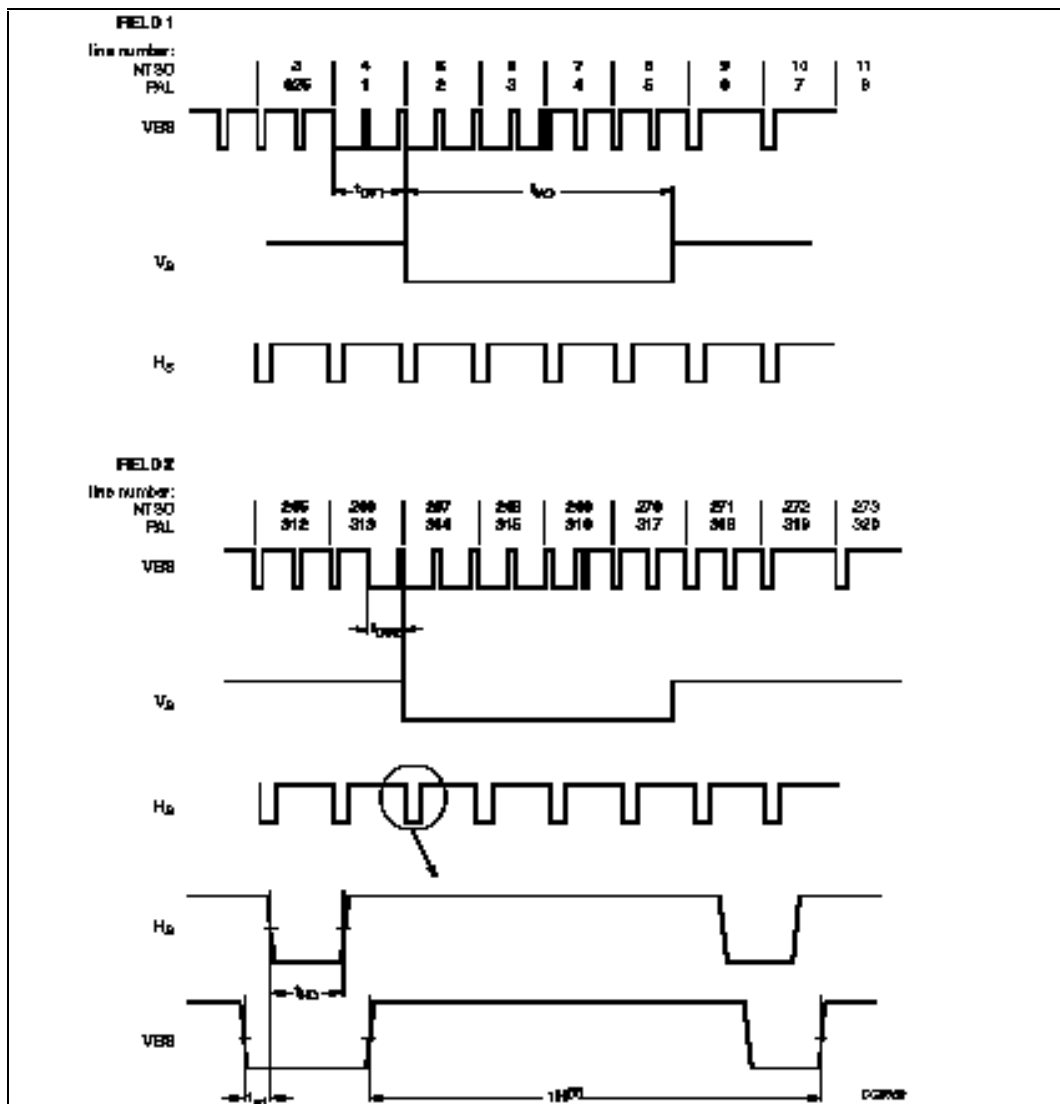


Fig. 3 Input and output signals

7.6 External clock

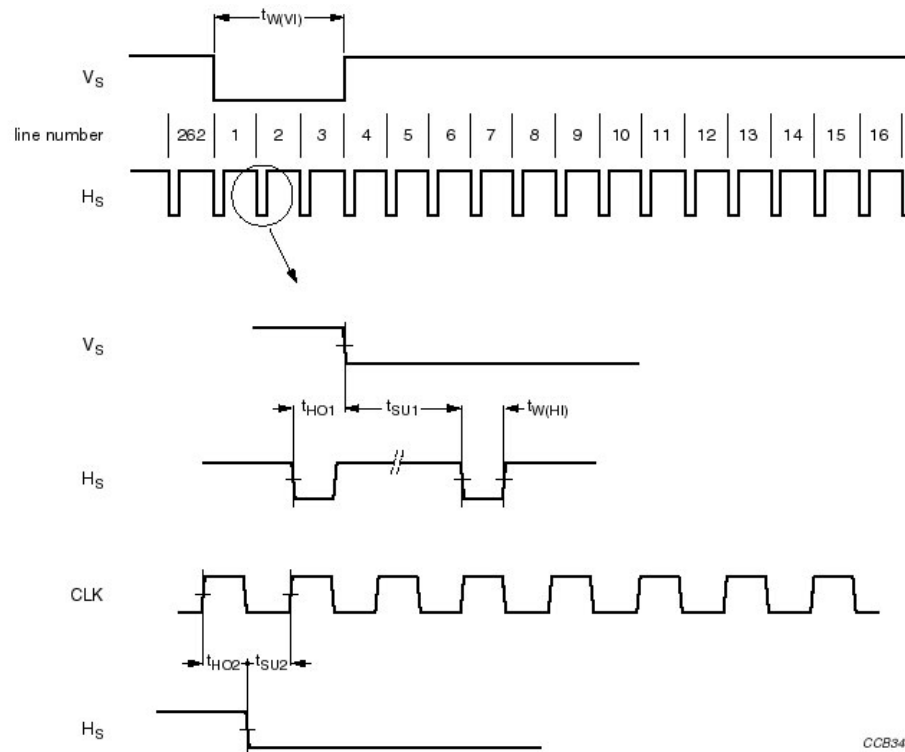


Fig. 4. Definition of line and pixel numbers

7.7 Backlight dimming

PWM timing is only valid for standard PAL or NTSC synchronisation signal

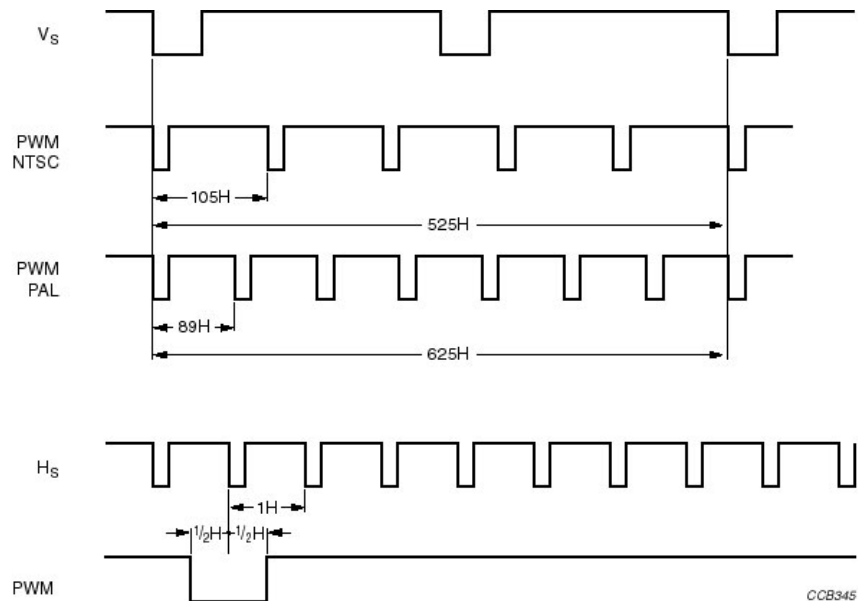


Figure 5 Generated PWM signal for NTSC and PAL

7.8 Power on/off sequences

Recommended sequence for power on:

- 1 Switch on the power supply
- 2 Switch on the control signals

Recommended sequence for power off:

- 1 Switch off the control signals power supply
- 2 Switch off the power supply

Power supply reset:

If the power supply voltage V_{DD} drops $\pm 7.2V$, the module switches off. The module will automatically switch on when the V_{DD} increases above $\pm 7.4V$. Maximum transition time from 6.5 to 8 Volt is 500 msec.

8 OPTICAL DATA

8.1 Optical characteristics

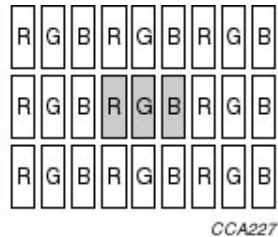
$T_{amb} = +22 \pm 3$ C; elapsed time from switch-on is greater than 45 minutes; driving conditions are typical values unless otherwise specified. Measurements are made perpendicular to the panel unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L	luminance	$I_{(RMS)} = 6.0$ mA; note 1.	300	350		Cd/m ²
CR _{max}	maximum contrast ratio	At optimum viewing angle; note 1	100 : 1	200		
α	viewing angle: Θ =horizontal right Θ =horizontal left Θ =vertical up Θ =vertical down	CR>5; note 1	60 60 45 45	70 70 50 70		deg deg deg deg
t _{res}	average response time	rise time fall time		30 15		ms ms
x _W y _W x _R y _R x _G y _G x _B y _B	color coordinates: white white red red green green blue blue	peak white; note 2	0.265 0.280 0.557 0.274 0.263 0.523 0.122 0.071	0.315 0.330 0.607 0.324 0.313 0.573 0.147 0.121	0.365 0.380 0.657 0.374 0.363 0.623 0.172 0.171	
α_{opt}	Optimum viewing angle (for contrast)	$\Theta = 270$ (6 o'clock); notes.1 and 3		3		deg

NOTES

1. Brightness control input (BRT) open circuit
2. No dimming
3. Customer is advised to use the display in the 12 o'clock direction

8.2 Pixel organization



8.3 Contrast ratio

The contrast ratio (CR) is the ratio between the transmission (τ) in a full white area

($R = G = B = 1$) and the transmission (τ_d) in a dark area ($R = G = B = 0$):

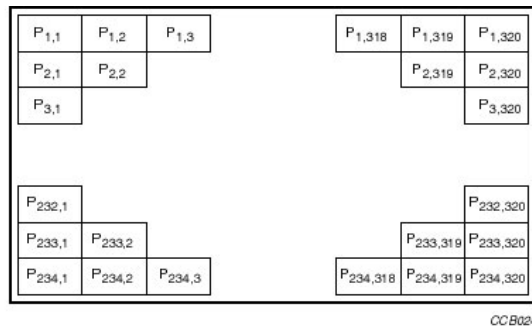
$$CR = \tau / \tau_d$$

8.4 Response time

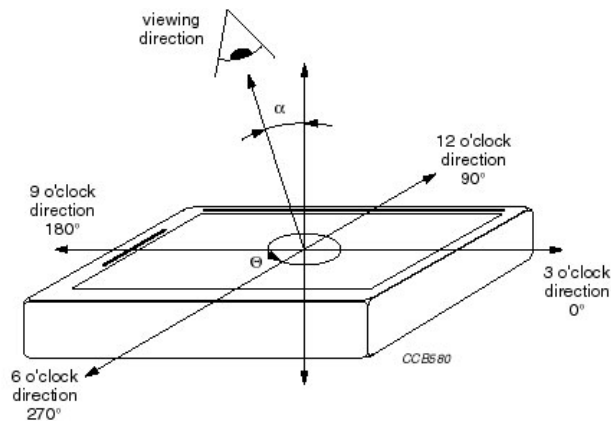
Response time (t_{res}) is the mean of rise time (t_r) and fall time (t_f):

$$t_{res} = (t_r + t_f) / 2$$

Rise time is the time for luminance to change from 10% to 90% as a result of a change of electrical condition, fall time is the time for luminance to change from 90% to 10% as a result of a change of electrical condition.



8.5 Viewing angle



9 ENVIRONMENTAL DATA

9.1 Environmental tests

Measurements are performed after two hours in room temperature environment; unless otherwise specified.

TEST	CONDITIONS	METHOD	REMARK
High temperature, operating	$T_{\text{panel}} = +85^{\circ}\text{C}$ for 240 hours	IEC 60068-2-2Bb	panel surface temperature
Low temperature, operating	$T_{\text{amb}} = -30^{\circ}\text{C}$ for 240 hours	IEC 60068-2-1Ab	
High temperature storage	$T_{\text{amb}} = +90^{\circ}\text{C}$ for 240 hours	IEC 60068-2-2Bb	module not operated
Low temperature storage	$T_{\text{amb}} = -40^{\circ}\text{C}$ for 240 hours	IEC 60068-2-1Ab	module not operated
High temperature, high humidity, operating	$T_{\text{amb}} = +60^{\circ}\text{C}$, RH = 90% for 240 hours	IEC 60068-2-3Ca	module operating
Thermal shock	$T_{\text{amb}} = -40$ to 85°C ; 168 cycles	IEC 60068-2-14Nb	module not operated
UV 765 W/m ²	168 hr	IEC 60068-2-5Sa	module not operated

9.2 Mechanical tests

TEST	CONDITIONS	METHOD	REMARK
Shock	3 directions: X, Y, Z axes; 6 repeats; peak acceleration = 100 G; pulse duration = 6 ms	IEC 60068-2-27Ea	not operated; not packed
Vibration	3 directions: X, Y, Z axes; 6 repeats; sweep time = 11 minutes; peak acceleration = 10 G; frequency = 10 to 150 Hz; amplitude = 1.5 mm peak-to-peak	IEC 60068-2-6Fc	not operated; not packed

9.3 Electrostatic discharge (ESD)

Under directive "89/336/EEG" conforms with "EN50082-1".

9.4 Electromagnetic (EMC)

Under directive "89/336/EEG" conforms with "EN55022/B" and "EN61000-4-6".

9.5 Safety

Complies with "IEC60950"

10 Handling and safety requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the liquid crystalline material. In case of contamination with liquid crystal material, wash immediately with water and soap.

CAUTION
At temperatures lower than the rated storage temperature, the liquid crystal solidifies causing permanent damage to the display.
At temperatures higher than the rated storage temperature, the liquid crystal turns into an isotropic liquid and may not recover.
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronics components.
Disassembling the display module can cause permanent damage and invalidates the warranty agreements.
Observe general precautions that are common to handling delicate electronic components. The glass can break and polarizers can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

11 MOUNTING

CAUTION
Allow enough space at the back of the module for sufficient airflow to disperse heat generated by the backlighting system.

12 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development
Preliminary specifications	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specification
Limiting values	
Limiting values given are in accordance with the absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability	
Application information	
Where applications information is given, it is advisory and does not form part of the specification.	

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1. SCOPE

This Quality Description Sheet applies to all versions of the Active Matrix Liquid Crystal Display Module type number LTE052T-060 (hereinafter called the Module), supplied by Philips Flat Panel Display Co. (PFPD) B.V. to the Customer or an agent of the Customer.

2. Conformance to specification

Conformance to specification regarding visual defects is guaranteed by a 100% final inspection and by a lot release based on a sampling inspection with zero defects. With regard to parametric specifications the PFPD Quality Assurance monitoring system will apply.

3. Inspection conditions and test patterns

Item	Conditons	
Lighting	Fluorescent light (Day-Light Type) Display Surface illumination to be 500 - 1000 Lux.	
Temperature	25 °C +/- 5 °C	
Driving Conditon	Equipment	Customer controller or PFPD original controller
	Test pattern	Black, White, R, G, B
	Supply voltage	typical supply voltages given in commercial specification
	inspection time	≤ 1 minute

Remarks: Inspect at 20 inches from display.
Defects that are not noticed within 1 minute shall be ignored.
Standard Viewing angle of the inspection shall be perpendicular to the display surface.
Inspection at other viewing angles shall not exceed the range of specified viewing angle.

4. VISUAL DEFECT CRITERIA

The defect categories covered in this QDS are comprised of defects in the active display area such as dot defects, blemishes and partly or completely malfunctioning displays as well as the visual appearance of the complete product and the packing of the product. The different defect categories are described below.

				COMPANY RESTRICTED	
		General Quality Description Sheet Active Matrix Liquid Crystal Display Module LTE052T-06x* family	4322 252 32890	A	99-01-25
		Supp. vers. 2.2	99-01-25	4	367 1 EN --- A4
KH		©KONINKLIJKE PHILIPS ELECTRONICS N.V. 1999			

				COMPANY RESTRICTED					
		General Quality Description Sheet Active Matrix Liquid Crystal Display Module LTE052T-06x* family			4322 252 32890		A		99-01-25
		Supp. vers. 2.2	99-01-25	4	367	2	EN	---	A4
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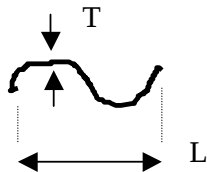
4.2.2 Long defects

Size (mm)		Acceptable number	
		Active area	Black border
$T \leq 0.03$	-	No count	No count
$0.03 < T \leq 0.08$	$L \leq 2.0$	No count	
$0.03 < T \leq 0.08$	$2.0 < L \leq 3.0$	1	
$0.03 < T \leq 0.08$	$3.0 < L$	0	
$0.08 < T$	-	0	

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T = defect thickness

L = defect contour length



4.2.3 Pinholes

Black border only.

Size (mm)	Acceptable number
	Black border
$D \leq 0.15$	No count
$0.15 < D$	0

D = diameter

4.2.4 Color blemishes

If applicable shall not exceed the accepted limit sample.

4.3 Malfunctioning

Not allowed are:

- Malfunctioning display: no picture, distinct block or line failure.
- Malfunctioning backlight.
- Excessive start up time (> 3 sec.)

					COMPANY RESTRICTED				
		General Quality Description Sheet			A		99-01-25		
		Active Matrix Liquid Crystal Display Module			4322 252 32890				
		LTE052T-06x* family							
		Supp. vers. 2.2	99-01-25	4	367	3	EN	---	A4
KH		©KONINKLIJKE PHILIPS ELECTRONICS N.V. 1999www.DataSheet4U.com							

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4.4 Appearance

Not allowed are:

- Type/serial number wrong, missing or not legible.
- Offensive surface damage.
- Connectors damaged.
- Stains within active area, such as finger prints or adhesive residues.
- Dirty appearance (can not be removed with a dry cloth).

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4.5 Packing

Not allowed are:

- Box damaged, wet, badly taped or stapled causing the product not to arrive in good condition at the Customer.
- Type or model number wrong, missing or not legible.

						COMPANY RESTRICTED	
		General Quality Description Sheet		A		99-01-25	
		Active Matrix Liquid Crystal Display Module		4322 252 32890			
		LTE052T-06x* family					
		Supp. vers. 2.2	99-01-25	4	367 4	EN	A4
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The specification of the LTE502T-9197-1 is based on the specification of the LTE052T-060.
The General Quality Description Sheet of the LTE052T-06* family is valid for the LTE502T-9197-1.

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The LTE502T-9197-1 product is almost equal to the LTE052T-060 product, exceptions are:

- Pin 22 of the interface connector became possible pixel clock output
- Mechanical drawing updated.

Details of the deviations are list as follows:

- Section 6 Pinning for electrical interface:** Pin 22 was changed to pixel clock I/O pin.

SYMBOL	PIN	I/O	DESCRIPTION
Analog interface			
H _s	1	I/O	Horizontal sync; notes 1 and 2
V _s	2	I/O	Vertical sync; notes 1 and 3
PWM	3	O	Synchronization signal for backlight
P/N	4	I	PAL/NTSC control signal, note 8
HRV	5	I	Horizontal scanning direction; note 4
VRV	6	I	Vertical scanning direction note 5
V _{sw}	7	I	RGB ₁ / RGB ₂ video signal switching; note 6
n.c.	8	-	Not connected
n.c.	9	-	Not connected
V _{DD}	10	I	Supply voltage
VBS	11	I	VBS input for sync separator
BRT	12	I	Brightness control
R ₁	13	I	Red video signal 1
G ₁	14	I	Green video signal 1
B ₁	15	I	Blue video signal 1
n.c.	16	-	Not connected
R ₂	17	I	Red video signal 2
G ₂	18	I	Green video signal 2
B ₂	19	I	Blue video signal 2
GND	20	I	Ground
CLKC	21	I	Change I/O direction of CLK, H _s and V _s ; note 7
CLK	22	I/O	Clock signal
Backlight			
V _{in}	1	I	Backlight input voltage
GND	2	I	Backlight ground connection

NOTES

- 1 CLKC= LOW: module is activated by CLK, H_s and H_s.
- 2 CLKC = HIGH: H_s is output, synchronised to VBS signal
CLKC = LOW: H_s is horizontal sync input.
- 3 CLKC = HIGH: V_s is output, synchronised to VBS signal
CLKC = LOW: V_s is vertical sync input.
- 4 HRV = HIGH: image is normal
HRV = LOW: image is reversed into horizontal direction.
- 5 VRV = HIGH: image is normal
VRV = LOW: image is reversed into vertical direction.
- 6 V_{sw} = HIGH: RGB₁ is selected
V_{sw} = LOW: RGB₂ is selected

				COMPANY RESTRICTED			
		Commercial Specification				A	05-10-27
		Active Matrix 5" colour TFT LCD Module		9360 307 56112		A	05-12-13
		LTE502T-9197-1					06-02-16
Leo Chow			05-10-24	1	190 -1	EN	A4
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- 7 CLKC = HIGH : CLK, H_s and V_s become output mode
 CLKC = LOW: CLK, H_s and V_s become input mode
 8 P/N switching when not operating

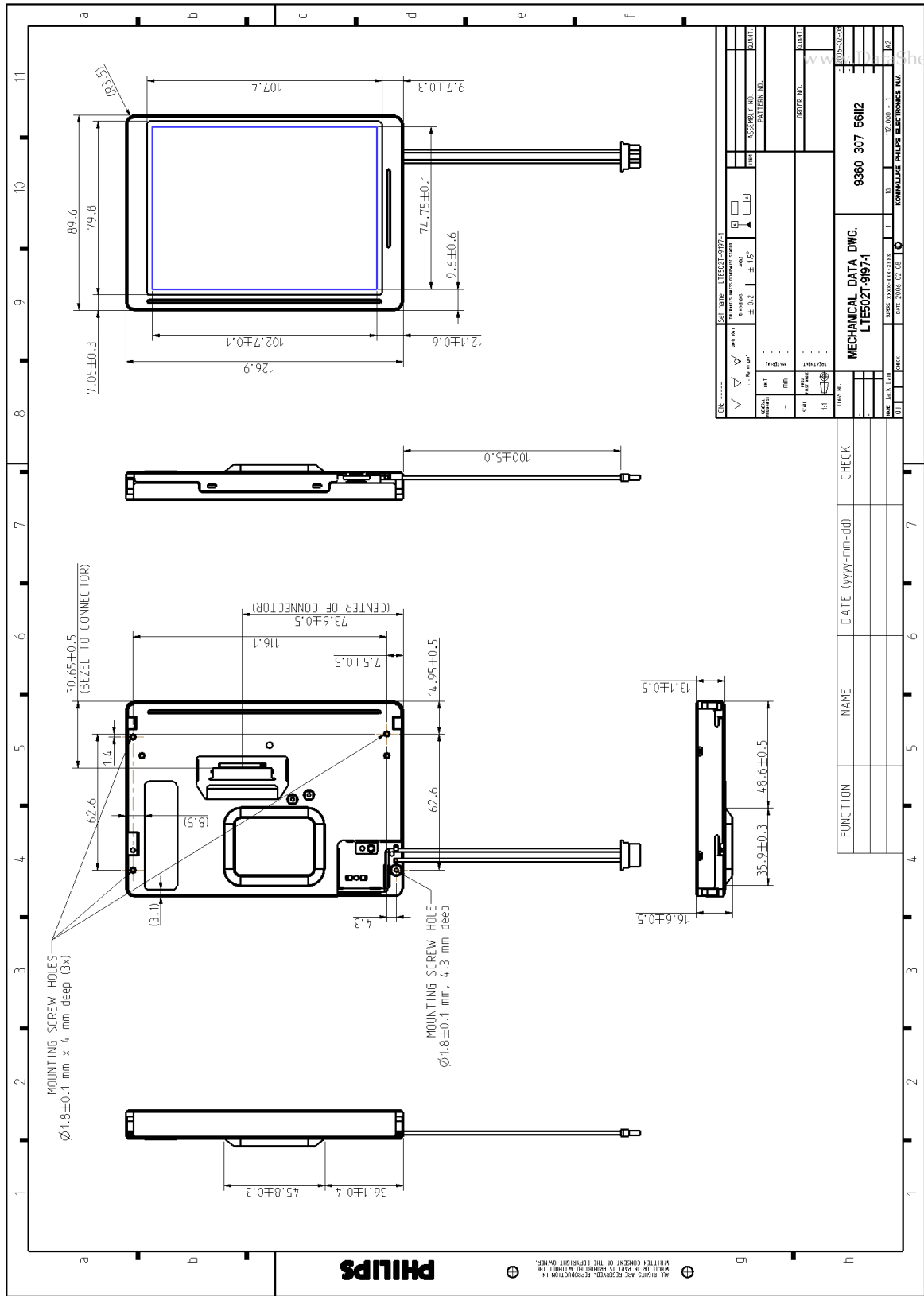
2. Section 7.4 Characteristics: Merge "Hs, Vs, PWM" and "CLK" into one related item.

GND = 0 V; T_{amb} = -30 to + 70 C; unless otherwise stated.

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
H_s, V_s, CLK, V_{sw}						
V _{IH}	HIGH-level input voltage		3.5			V
V _{IL}	LOW-level input voltage				1.5	V
P/N, VRV, CLKC, HRV						
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage				0.8	V
H_s, V_s, PWM, CLK						
V _{OH}	HIGH-level output voltage	I _{OH} = -4 mA	2.4			V
V _{OL}	LOW-level output voltage	I _{OL} = +4 mA			0.4	V
CLK, HRV						
I _{IH}	HIGH-level input current	V _I = + 5 V	-0.1		+0.1	µA
I _{IL}	LOW-level input current	V _I = 0 V			-4.5	µA
H_s, P/N, V_s, VRV, CLKC						
I _{IH}	HIGH-level input current	V _I = +5 V			+10	µA
I _{IL}	LOW-level input current	V _I = 0 V			-200	µA
VSW						
I _{IH}	HIGH-level input current	V _I = +5 V			+10	µA
	LOW-level input current	V _I = 0 V			-600	µA
R, G, B, V_{sw}, VBS						
C _I	input capacitance	f = 1 MHz		28		pF
P/N, HRV, VRV, CLK, PWM, H_s, V_s						
C _I	input capacitance	f = 1 MHz		37		pF
CLKC						
C _I	input capacitance	f = 1 MHz		10		nF

				COMPANY RESTRICTED				
		Commercial Specification				A	05-10-27	
		Active Matrix 5" colour TFT LCD Module			9360 307 56112	A	05-12-13	
		LTE502T-9197-1					06-02-16	
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3. Section 5 Mechanical Data:



COMPANY RESTRICTED			
Commercial Specification Active Matrix 5" colour TFT LCD Module LTE502T-9197-1	9360 307 56112	A	05-10-27
		A	05-12-13
			06-02-16
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