

DATA SHEET

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LTE052T-061 Active matrix 5" colour TFT LCD module

Preliminary specification

21 January 1999

**Philips Flat Panel Display Co.
(Philips FPD) B.V.**



PHILIPS

Active matrix 5" colour TFT LCD module**LTE052T-061**

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LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Flat Panel Display Co. (Philips FPD) B.V. customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Flat Panel Display Co. (Philips FPD) B.V. for any damages resulting from such improper use or sale.

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1 GENERAL DESCRIPTION

This is an active matrix LCD module which comprises:

- A 5" colour TFT panel
- Panel driver electronics
- Integrated backlight
- Integrated interface card
- Separate 1 : 30 inverter.

The 5" active area has full colour capability using $320 (3 \times \text{RGB}) \times 234$ pixels. The panel has a 4 : 3 aspect ratio and a wide viewing angle.

The module can withstand intense environments.

Outline dimensions compatible with double-DIN size for automotive use.

2 FEATURES

- RGB stripe configuration
- Two analog RGB with H_S and V_S inputs
- Two analog RGB channels with possibility of picture-in-picture
- (C)VBS for synchronization or H_S , V_S with CLK signal
- Selectable NTSC/PAL (RGB)
- Up/down and left/right control signals
- Display aspect ratio: 4 : 3
- Display resolution: 234 lines
- High-contrast TFT LCD drive system
- High-speed response
- High-brightness luminance
- Wide viewing angle
- Integrated high-efficiency backlight
- Extended temperature range
- Dimming ratio: 1 : 30.

3 APPLICATIONS

- Car navigation
- TV and VCR monitors
- Video games
- Automation and process-control monitors.

4 QUICK REFERENCE DATA

PARAMETER	VALUE	UNIT
Overall dimensions (without inverter):		
width	126.8	mm
height	89.6	mm
depth	13.0	mm
Active area dimensions:		
width	102.72	mm
height	74.76	mm
Display resolution	320×234	pixels
Pixel dimensions:		
horizontal	3×0.107	mm
vertical	0.319	mm
Pixel configuration	RGB stripe	
Supply voltage (module)	8 to 16	V
Power consumption (with inverter)	6.2	W
Dimming ratio	1 : 30	
Luminance	350	cd/m ²
Backlight life at 25 °C; $I_{\text{lamp}} = 6 \text{ mA (RMS)}$; continuous operation	min. 8000	hours
Typical viewing angle (contrast ratio >5):		
horizontal right	70	deg
horizontal left	70	deg
vertical up	50	deg
vertical down	-70	deg
Maximum operating ambient temperature	65	°C
Operating panel surface temperature range	-30 to +85	°C
Storage temperature range	-40 to +90	°C
Typical response time:		
rise time	30	ms
fall time	15	ms
Mass of the module	183 ± 10	g

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4.1 Block diagram

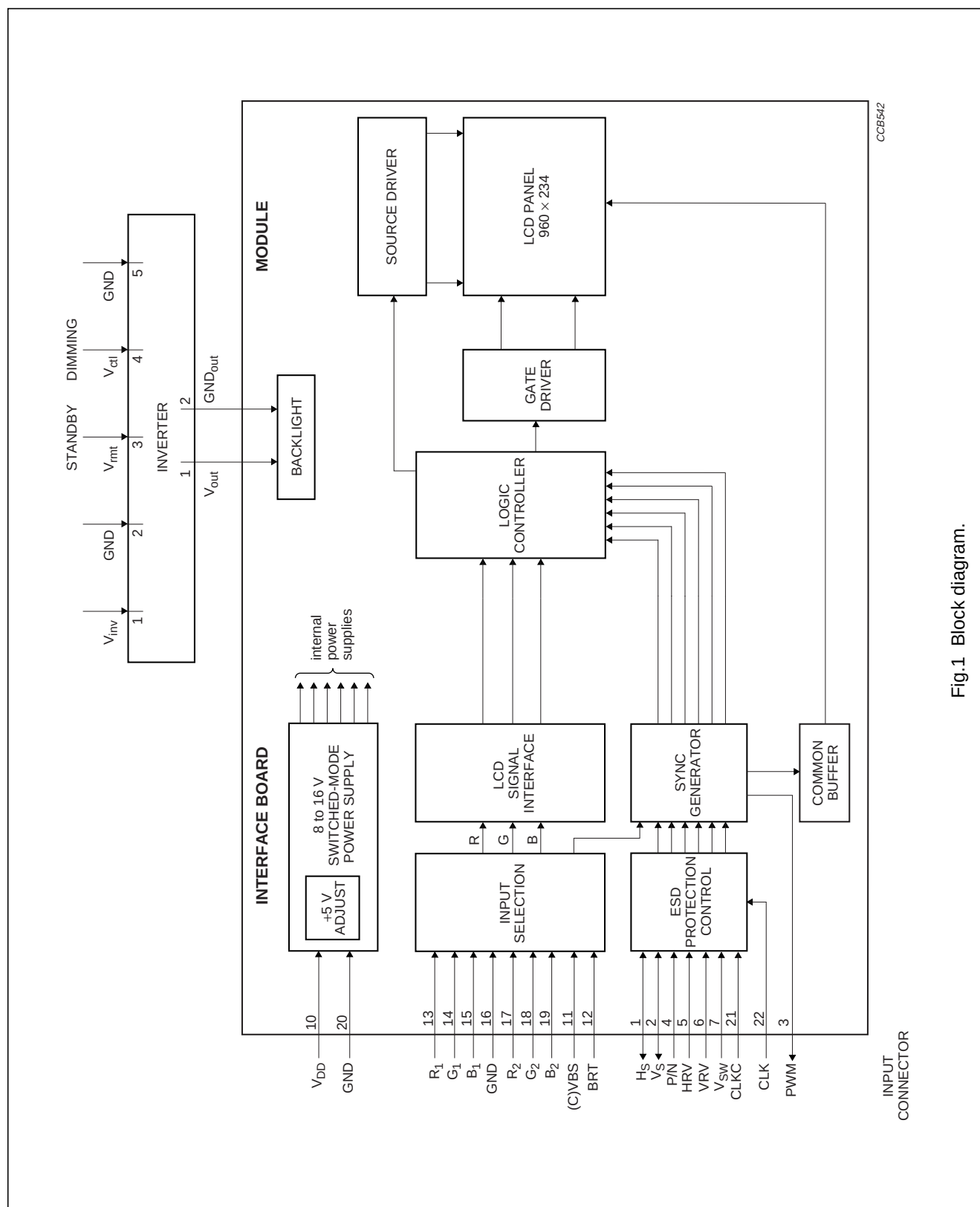


Fig.1 Block diagram.

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5 MECHANICAL DATA

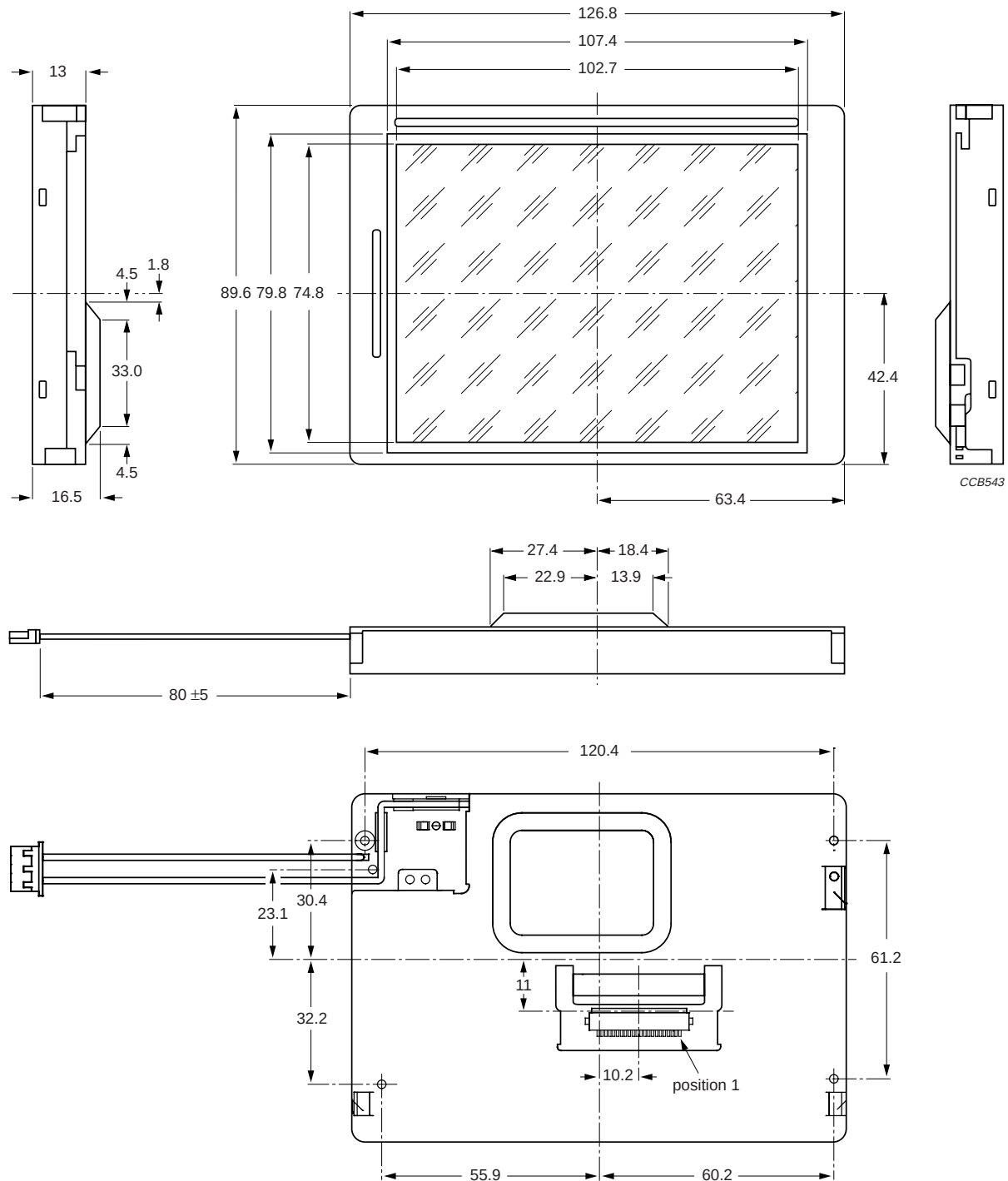


Fig.2 Mechanical outline.

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5.1 Dimensions

PARAMETER	VALUE	UNIT
Display format	$(320 \times 3) \times 234$	dots
Active area	102.72×74.76	mm
Screen size (diagonal)	127	mm
	5.0	inches
Pixel pitch:		
horizontal	3×0.107	mm
vertical	0.319	mm
Dot configuration	RGB stripe	
Overall dimensions (excluding connectors and inverter):		
width	126.8 ± 0.3	mm
height	89.6 ± 0.3	mm
depth	13.0 ± 0.3	mm
Mass of the module	183 ± 10	g

5.2 Electrical connectors

SERVICE	NUMBER OF PINS	MATING CONNECTOR
Interface	22	22-pin flex foil (1 mm pitch)
Inverter input	5	Molex 51021-0500 or equivalent
Inverter output	2	JST BHR-03VS-1 or equivalent
Backlight	2	JST SM02(8.0)B-BHS-1-TB

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6 PINNING

6.1 Module interface

SYMBOL	PIN	I/O	DESCRIPTION
H _S	1	I/O	horizontal sync; notes 1 and 2
V _S	2	I/O	vertical sync; notes 1 and 3
PWM	3	O	synchronization signal for backlight
P/N	4	I	PAL/NTSC control signal
HRV	5	I	horizontal scanning direction; note 4
VRV	6	I	vertical scanning direction; note 5
V _{SW}	7	I	RGB ₁ /RGB ₂ video signal switching; note 6
n.c.	8	–	not connected
n.c.	9	–	not connected
V _{DD}	10	I	supply voltage
VBS	11	I	VBS input for sync separator
BRT	12	I	brightness control
R ₁	13	I	red video signal 1
G ₁	14	I	green video signal 1
B ₁	15	I	blue video signal 1
n.c.	16	–	not connected
R ₂	17	I	red video signal 2
G ₂	18	I	green video signal 2
B ₂	19	I	blue video signal 2
GND	20	I	ground
CLKC	21	I	change I/O direction of CLK, H _S and V _S ; note 7
CLK	22	I	clock signal

Notes

1. CLKC = LOW: module is activated by CLK, H_S and V_S.
2. CLKC = HIGH: H_S is output, synchronized to VBS signal
CLKC = LOW: H_S is horizontal sync input.
3. CLKC = HIGH: V_S is output, synchronized to VBS signal
CLKC = LOW: V_S is vertical sync input.
4. HRV = HIGH: image is normal
HRV = LOW: image is reversed in horizontal direction.
5. VRV = HIGH: image is normal
VRV = LOW: image is reversed in vertical direction.
6. V_{SW} = HIGH: RGB₁ is selected
V_{SW} = LOW: RGB₂ is selected.
7. CLKC = HIGH: H_S and V_S become output mode
CLKC = LOW: CLK, H_S and V_S become input mode.

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6.2 Backlight

SYMBOL	PIN	DESCRIPTION
V_{in}	1	backlight input voltage
GND	2	backlight and inverter ground connection

6.3 Inverter

SYMBOL	PIN	DESCRIPTION
Input connector CN1		
V_{inv}	CN1-1	inverter input voltage (8 to 16 V)
GND	CN1-2	ground (0 V)
V_{rmt}	CN1-3	standby control voltage TTL-compatible input; HIGH = ON
V_{ctl}	CN1-4	dimming control voltage (adjust from 0 V for full dimming to 5.0 V for no dimming)
GND	CN1-5	ground
Output connector CN2		
V_{out}	CN2-1	inverter output voltage
GND_{out}	CN2-2	output ground

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7 ELECTRICAL CHARACTERISTICS

7.1 Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

 $T_{amb} = 25\text{ °C}$; GND = 0 V; unless otherwise stated.

SYMBOL	DESCRIPTION	MIN.	MAX.	UNIT
V_{DD}	power supply voltage (pin 10)	-0.3	20	V
$V_{I(analogue)}$	analog input voltage (peak-to-peak value)	-0.3	5	V
$V_{I(dig)}$	digital input voltage	-0.3	5	V
$V_{O(dig)}$	digital output voltage	-0.3	5.3	V
RH	relative humidity; note 1:			
	$T_{amb} \leq 60\text{ °C}$	–	90	%
	$T_{amb} = 60\text{ to }90\text{ °C}$	–	85	%
T_{stg}	storage temperature; note 1	-40	+90	°C
T_{amb}	operating ambient temperature	-30	+65	°C
T_{oper}	operating panel surface temperature; note 2	-30	+85	°C

Notes

1. No condensation is allowed under any condition.
2. Operating panel surface temperature range only assures panel driving.

7.2 Recommended operating conditions - module

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DD}	power supply; note 1		7.8	12.0	16.0	V
V _{I(a)}	analog input voltage; note 2:					
	AC component (peak-to-peak value)		0.7	1.0	2.0	V
	AC component video content (peak-to-peak value); note 3		–	0.7	–	V
	DC component		–1.0	0	+1.0	V
V _{I(d)}	digital input voltage; note 4		0	–	5.2	V
BRT	brightness control		0	–	5.0	V
f _H	VBS horizontal sync frequency; note 5:	CLKC = HIGH				
	NTSC		15.13	15.73	16.33	kHz
	PAL		15.03	15.63	16.23	kHz
t _{W(H)}	VBS horizontal sync pulse width; note 5:	CLKC = HIGH				
	NTSC		4.2	4.7	5.2	μs
	PAL		4.2	4.7	5.2	μs
t _{r(H)} , t _{f(H)}	VBS horizontal sync pulse rise and fall times; note 5	CLKC = HIGH	–	–	0.5	μs
f _V	vertical sync frequency; note 4:	CLKC = HIGH				
	NTSC		f _H /284	f _H /262	f _H /258	Hz
	PAL		f _H /344	f _H /312	f _H /304	Hz

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SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{W(V)}$	vertical sync pulse width; note 4: NTSC PAL	CLKC = HIGH	– –	3H 2.5H	– –	μs μs
$t_{r(V)}, t_{f(V)}$	vertical sync pulse rise and fall times; note 4	CLKC = HIGH or LOW	–	–	0.5	μs
f_{clk}	input clock frequency	CLKC = LOW	6.0	6.8	7.6	MHz
t_{WH}	input clock pulse width HIGH	CLKC = LOW	20	–	–	ns
t_{WL}	input clock pulse width LOW	CLKC = LOW	20	–	–	ns
$t_{r(\text{clk})}$	input clock rise time	CLKC = LOW	–	–	10	ns
$t_{f(\text{clk})}$	input clock fall time	CLKC = LOW	–	–	10	ns
f_{HS}	H_S input frequency	CLKC = LOW	$f_{\text{clk}}/465$	$f_{\text{clk}}/435$	$f_{\text{clk}}/405$	kHz
$t_{W(HS)}$	H_S input pulse width	CLKC = LOW	1	5	9	μs
$t_{r(HS)}, t_{f(HS)}$	H_S input pulse rise and fall times	CLKC = LOW	–	–	0.05	μs
f_{VSR}	VSR input frequency	CLKC = LOW	50	$f_H/262$	$f_H/258$	Hz
$t_{W(VSR)}$	VSR input pulse width	CLKC = LOW	1H	3H	5H	μs
t_{SU1}	V_S to H_S set-up time	CLKC = LOW	25	–	–	ns
t_{HO1}	V_S to H_S hold time	CLKC = LOW	25	–	–	ns
t_{SU2}	CLK to H_S set-up time	CLKC = LOW	1.0	–	–	μs
t_{HO2}	CLK to H_S hold time	CLKC = LOW	1.0	–	–	μs

Notes

1. The module does not have load dump, under or overvoltage protection.
2. Applies to VBS input.
3. Applies to VR_1 , VG_1 , VB_1 , VR_2 , VG_2 and VB_2 .
4. Applies to H_S , NTP, V_S , HRV, CLKC, CLK and VSW.
5. Applies to H_S .

7.3 Recommended operating conditions - inverter
 $T_{\text{amb}} = -30$ to $+85$ °C; relative humidity <90%.

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ctl}	dimming control DC voltage	note 1	0	–	5.0	V
V_{rmt}	standby voltage	note 2	TTL-compatible			
V_{in}	input voltage		8.0	12.0	16.0	V
P_{out}	output power		t.b.f.	3.5	t.b.f.	W
R_{out}	output load		t.b.f.	100	t.b.f.	k Ω

Notes

1. Adjust from 0 V for full dimming to 5.0 V for no dimming.
2. Inverter OFF: $V_{\text{rmt}} = 0 \leq V_{\text{rmt}} < 1.3$ V (logic LOW).
Inverter ON: $V_{\text{rmt}} = 1.6 < V_{\text{rmt}} \leq 5.0$ V (logic HIGH).

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7.4 Characteristics

 GND = 0 V; $T_{amb} = -30$ to $+65$ °C; unless otherwise stated.

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CLK, H_S, V_S						
V _{IH}	HIGH-level input voltage		3.5	–	–	V
V _{IL}	LOW-level input voltage		–	–	1.5	V
CLKC, NTP, VRV						
V _{IH}	HIGH-level input voltage		2.0	–	–	V
V _{IL}	LOW-level input voltage		–	–	0.8	V
CLK, H_S, V_S, PWM						
V _{OH}	HIGH-level output voltage	I _{OH} = –4 mA	2.4	–	–	V
V _{OL}	LOW-level output voltage	I _{OL} = +4 mA	–	–	0.4	V
CLK (note 1)						
V _{OL}	LOW-level output voltage	I _{OL} = +4 mA	–	–	0.4	V
CLK, HRV, VSW						
I _{IH}	HIGH-level input current	V _I = +5 V	–0.1	–	+0.1	µA
I _{IL}	LOW-level input current	V _I = 0	–	–	–4.5	µA
CLKC, H_S, V_S, NTP, VRV						
I _{IH}	HIGH-level input current	V _I = +5 V	–	–	+10	µA
I _{IL}	LOW-level input current	V _I = 0	–	–	–200	µA
VSW						
I _{IH}	HIGH-level input current	V _I = +5 V	–	–	+10	µA
I _{IL}	LOW-level input current	V _I = 0	–	–	–600	µA
R₁, G₁, B₁, R₂, G₂, B₂, VSW, VBS						
C _I	input capacitance	f = 1 MHz	–	28	–	pF
CLK, H_S, V_S, NTP, HRV, VRV, PWM						
C _I	input capacitance	f = 1 MHz	–	37	–	pF
CLKC						
C _I	input capacitance		–	10	–	nF

Note

1. At CLKC = HIGH, CLK = 0.

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7.5 Input and output timing

SYMBOL	DESCRIPTION	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{field}	field period: NTSC PAL	$f_{\text{field}} = 60 \text{ Hz}$	–	16.67	–	ms
		$f_{\text{field}} = 50 \text{ Hz}$	–	20.0	–	ms
T_{line}	line period: NTSC PAL		–	63.5	–	μs
			–	64.0	–	μs
f_{line}	line frequency: NTSC PAL		–	15.73	–	kHz
			–	15.625	–	kHz
t_{DV1}	V_S delay field 1		–	1H	–	
t_{DV2}	V_S delay field 2		–	H/2	–	
t_{VO}	vertical pulse width		–	4H	–	
t_{VID}	video signal on-display time		–	50.1	–	μs
$t_{\text{d}(\text{disp})}$	sync edge to start display delay time: NTSC PAL		–	10.6	–	μs
			–	11.1	–	μs
$t_{\text{d}(\text{HS})}$	sync edge to H_S delay time	50% level	–	1.4	–	μs
$t_{\text{W}(\text{H})}$	horizontal pulse width	50% level	–	1.2	–	μs

7.5.1 DISPLAYED LINES (PAL MODE)

Field 1 displayed line numbers:

27 to 298.

Field 2 displayed line numbers:

339 to 611.

In PAL, on average, every seventh line is skipped.

Actual lines skipped in Field 1:

 $34 + 14N$ where $N = 0, 1, \text{ to } 18$ and

 $40 + 14M$ where $M = 0, 1, \text{ to } 18$.

Actual lines skipped in Field 2:

 $344 + 14N$ where $N = 0, 1, \text{ to } 18$ and

 $350 + 14M$ where $M = 0, 1, \text{ to } 18$.

7.5.2 DISPLAYED LINES (NTSC MODE)

Field 1 displayed line numbers:

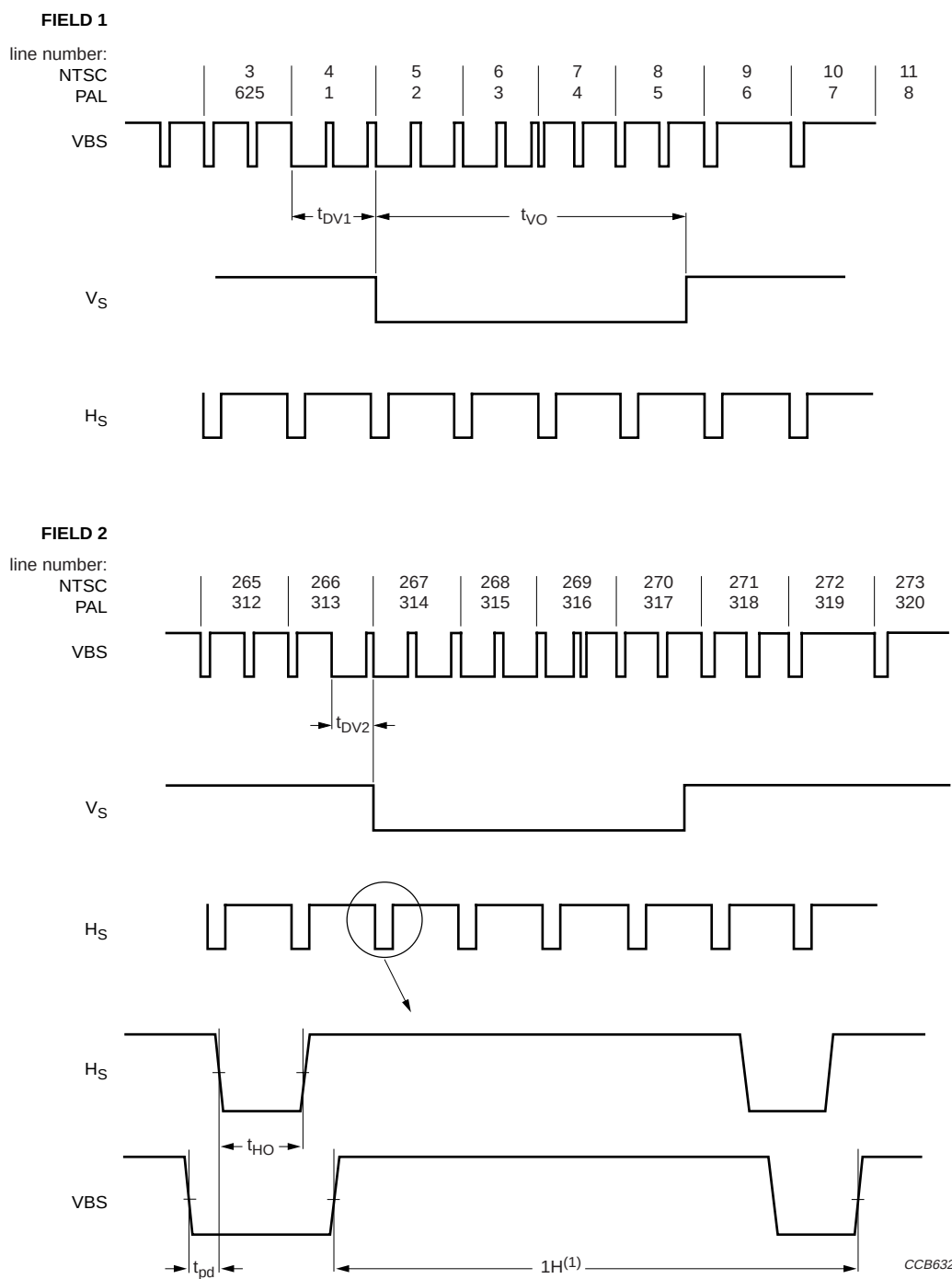
23 to 256.

Field 2 displayed line numbers:

286 to 519.

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(1) NTSC: $1H = 63.5 \mu s$ (typ.).
PAL: $1H = 64 \mu s$ (typ.).

Fig.3 Input and output signals.

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7.6 External clock

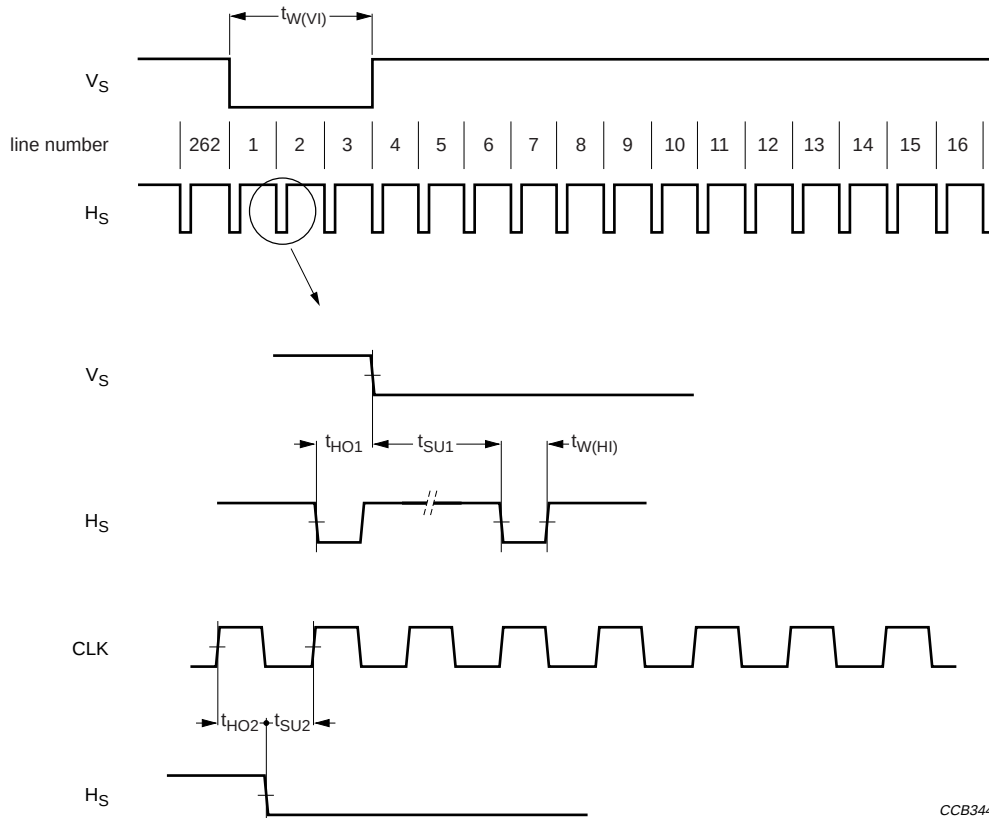


Fig.4 Definition of line and pixel numbers.

7.6.1 SYNC INPUTS

With the composite sync signal CS, the module will function correctly with signal sources such as video recorders.

The external horizontal and vertical pulses should have no disturbances for a stable picture.

Composite sync timing is according to CCIR.

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7.7 Backlight dimming

Backlight dimming should be used only with standard PAL and NTSC signals (see Fig.5).
For non-standard signals there is also a PWM signal but it is not synchronized.

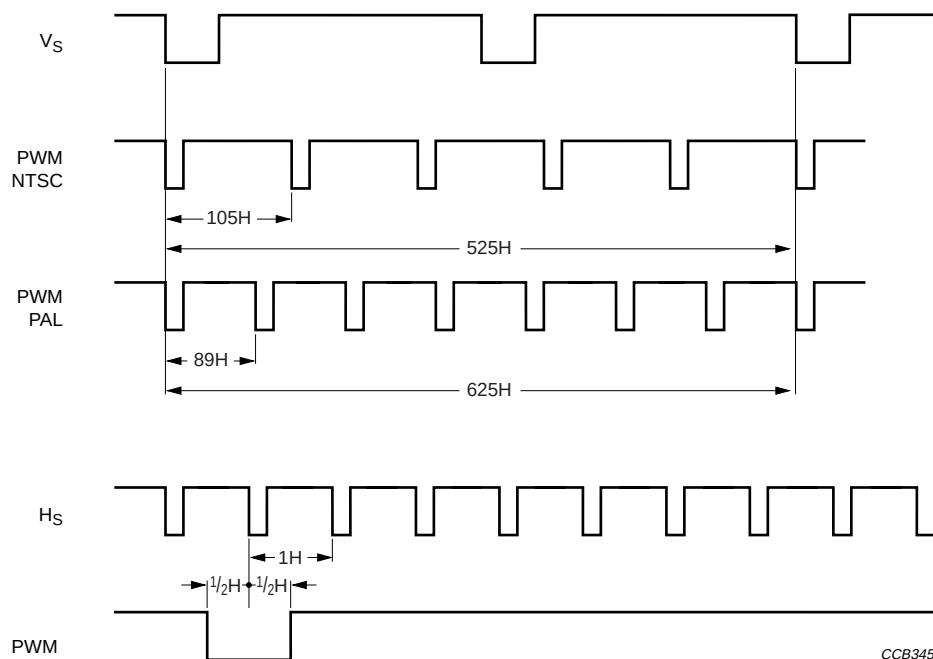


Fig.5 Generated PWM signal for PAL and NTSC.

7.8 Power-on/off sequences

Recommended sequence for power-on:

1. Switch on the video source.
2. Switch on the power supply
(maximum supply voltage rise time = 200 ms).
3. Switch on the backlight.

Recommended sequence for power-off:

1. Switch off the backlight.
2. Switch off the power supply
(minimum time to power-off = 250 ms).
3. Switch off the video source.

Power supply reset:

If the power supply voltage V_{DD} drops below 7.8 V, the module switches off.

The module can be restarted with $V_{DD} < 0.5$ V for a minimum of 250 ms followed by V_{DD} rising above 7.8 V within 200 ms.

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8 OPTICAL DATA

8.1 Optical characteristics

$T_{amb} = +22 \pm 3 \text{ }^{\circ}\text{C}$; elapsed time from switch-on is greater than 15 minutes; driving conditions are typical values; unless otherwise specified. Measurements are made perpendicular to the panel; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
L	luminance	$V_{I(RMS)} = 6.0 \text{ mA}$; note 1	300	350	—	Cd/m ²
CR _{max}	maximum contrast ratio	at optimum viewing angle; note 1	100 : 1	150 : 1	—	
DR	dimming ratio		—	1 : 30	—	
α	viewing angle: Θ = horizontal right Θ = horizontal left Θ = vertical up Θ = vertical down	CR > 5; note 1	60 60 45 45	70 70 50 70	— — — —	deg deg deg deg
t_{res}	average response time	rise time fall time	— —	30 15	— —	ms ms
x_W y_W x_R y_R x_G y_G x_B y_B	colour coordinates: white white red red green green blue blue	peak white; note 2	0.260 0.257 0.526 0.289 0.263 0.445 0.101 0.067	0.310 0.307 0.576 0.339 0.313 0.495 0.151 0.117	0.360 0.357 0.626 0.389 0.363 0.545 0.201 0.167	
α_{opt}	optimum viewing angle	$\Theta = 270^{\circ}$ (6 o'clock); notes 1 and 3	—	5	—	deg

Notes

- Brightness control input (BRT) open circuit.
- No dimming.
- Customer is advised to use the display in the 12 o'clock direction.

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8.2 Pixel organization

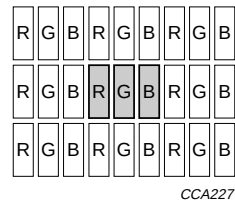


Fig.6 Dot organization.

8.3 Contrast ratio

The contrast ratio (CR) is the ratio between the transmission (τ) in a full white area ($R = G = B = 1$) and the transmission (τ_d) in a dark area ($R = G = B = 0$):

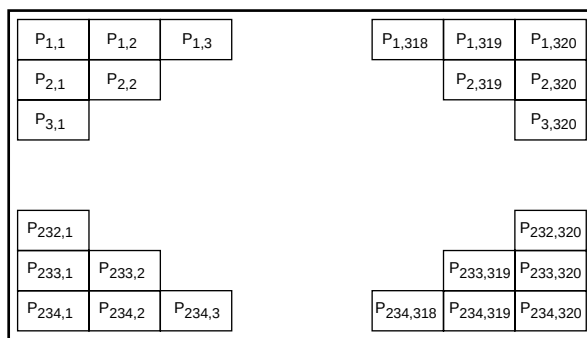
$$CR = \frac{\tau}{\tau_d}$$

8.4 Response time

Response time (t_{res}) is the mean of rise time (t_r) and fall time (t_f):

$$t_{res} = \frac{t_r + t_f}{2}$$

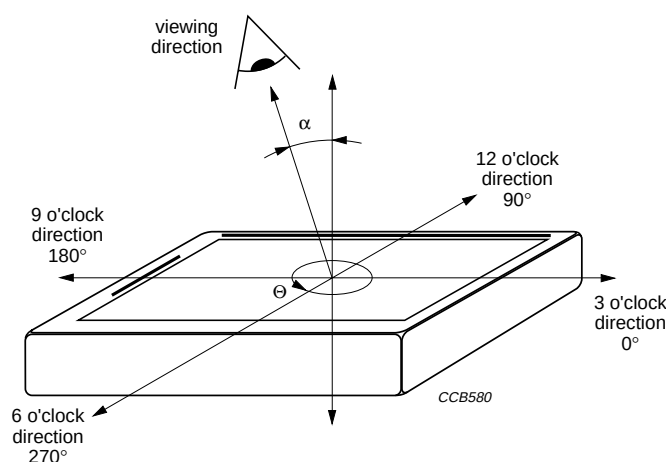
Rise time is the time for luminance to change from 10% to 90% as a result of a change of electrical condition, fall time is the time for luminance to change from 90% to 10% as a result of a change of electrical condition.



The pixels are square and are arranged in vertical stripes of red green and blue.
The pixel information is provided sequentially, row-by-row.
 $P_{1,1}$ is the upper-left pixel of the display, $P_{234,320}$ is the bottom-right pixel.

Fig.7 Pixel organization.

8.5 Viewing angle



α = declination.
 θ = azimuth.

Fig.8 Viewing angle.

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9 ENVIRONMENTAL DATA

9.1 Environmental tests

Measurements are performed after two hours in room temperature environment; unless otherwise specified.

TEST	CONDITIONS	METHOD	REMARK
High temperature, operating	$T_{\text{panel}} = +85\text{ }^{\circ}\text{C}$ for 240 hours	IEC 60068-2-2Bb	panel surface temperature
Low temperature, operating	$T_{\text{amb}} = -30\text{ }^{\circ}\text{C}$ for 240 hours	IEC 60068-2-1Ab	
High temperature storage	$T_{\text{amb}} = +90\text{ }^{\circ}\text{C}$ for 240 hours	IEC 60068-2-2Bb	module not operating
Low temperature storage	$T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ for 240 hours	IEC 60068-2-1Ab	module not operating
High temperature, high humidity, operating	$T_{\text{amb}} = +60\text{ }^{\circ}\text{C}$, RH = 90% for 240 hours	IEC 60068-2-3Ca	module operating
Thermal shock	$T_{\text{amb}} = -40$ to $+85\text{ }^{\circ}\text{C}$; 10 cycles	IEC 60068-2-14Nb	module not operating

9.2 Mechanical tests

TEST	CONDITIONS	METHOD	REMARK
Shock	3 directions: X, Y, Z axes; 6 repeats; peak acceleration = 100 G; pulse duration = 6 ms	IEC 60068-2-27Ea	not operated; not packed
Vibration	3 directions: X, Y, Z axes; 6 repeats; sweep time = 11 minutes; peak acceleration = 10 G; frequency = 10 to 150 Hz; amplitude = 1.5 mm peak-to-peak	IEC 60068-2-6Fc	not operated; not packed

9.3 Electrostatic discharge (ESD)

Under directive "89/336/EEG" conforms with "EN50082-1".

9.4 Electromagnetic compatibility (EMC)

Complies with "FCC part 15".

Under directive "89/336/EEG" conforms with "EN55022/B" and "EN61000-4-6".

9.5 Safety

Complies with "IEC 60950" and "UL1950".

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10 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

4322 252 32730

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