



Spec No. : DS-30-98-336 Effective Date: 06/23/2000

Revision: -

LITE-ON DCC

RELEASE

BNS-OD-FC001/A4

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FEATURES

- *0.56 INCH (14.22 mm) DIGIT HEIGHT.
- * WIDE SUPPLY VOLTAGE OPERATION.
- *SERIAL DATA INPUT.
- *CONSTANT CURRENT DRIVERS.
- *CONTINUOUS BRIGHTNESS CONTROL.
- *SOLID STATE RELIABILITY-LONG OPERATION LIFE.
- *WIDE VIEWING ANGLE.
- *TTL COMPATIBLE.

DESCRIPTION

The LTM-8530E is a 0.56 inch (14.22 mm) numeric display modules, and a built-in M5450 MOS integrated circuits. The integrated circuit contains serial data input, 35 bits shift register. 34 LED driver output and a brightness control. This device utilizes red orange LED chips, which are made from GaAsP on a transparent GaP substrate, and has a orange face and orange segments. The MOS integrated circuits are produced with N-channel silicon gate technology.

DEVICE

PART NO.	DESCRIPTION
RED ORANGE	2 Digit
LTM-8530E	Rt. Hand Decimal

PART NO.: LTM-8530E PAGE: 1 of 8

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PACKAGE DIMENSIONS 8.13[.320] 1.35[.053] DIGIT1 DIGIT2 А 9.05[,750] В E \mathbb{D} DP Ø1.7[D.067] 12.7[.500] PIN1 25[.984] PART NO. DATE CODE BIN CODE 0.3[.012] 0.5[.02] 15.24[.600] 2.54[.100]

NOTES: All dimensions are in millimeters. Tolerances are \pm 0.25 mm (0.01") unless otherwise noted.

PART NO.: LTM-8530E PAGE: 2 of 8

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PIN CONNECTION

No.	CONNECTION				
1	Vss				
2	VLED				
3	NO PIN				
4	NO PIN				
5	NO PIN				
6	BIT 17 OUTPUT				
7	BIT 18 OUTPUT				
8	BIT 19 OUTPUT				
9	BIT 20 OUTPUT				
10	BIT 21 OUTPUT				
11	BIT 22 OUTPUT				
12	BIT 23 OUTPUT				
13	BIT 24 OUTPUT				
14	DATA ENABLE				
15	DATA INPUT				
16	CLOCK INPUT				
17	VDD				
18	BRT. CONTROL				

PART NO.: LTM-8530E	PAGE: 3 of 8
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ABSOLUTE MAXIMUM RATING AT T_A=25°C

PARAMETER	Symbol	Min.	Max.	UNIT
Supply Voltage *1	VDD	-0.3	12	V
Input Voltage	VI	-0.3	12	V
Off State Output Voltage	Vo(off)		12	V
LED Supply Voltage	VLED	2.8	3.5	V
Power Dissipation of IC *2	PD(IC)		335	mW
Supply Current	IDD		8.5	mA
Operating Temperature Range	Тор	-20	+60	$^{\circ}\! \mathbb{C}$
Storage Temperature Range	Tstg	-20	+60	$^{\circ}\!\mathbb{C}$
Solder Temperature: max 260°℃ for max 3sec at 1.6mm below seating plane.				

Note: 1. All voltage are with respect to Vss(GND)

2. Power dissipation of IC is given by PD=(VLED-VF) • (IF) • (No. of Segments)+(8.5mA) • (VDD) *VF is LED forward voltage.

RECOMMENDED OPERATING CONDITION AT T_A=25°C

Parameter	Symbol	Min.	Тур.	Max.	Unit	Test Condition
Supply Voltage	VDD	4.75		11	V	
Input Voltage						
Logical "0" Level		-0.3		0.8	V	±10μA Input Bias
Logical "1" Level	VI	2.2		Vdd	V	4.75V < VDD < 5.25V
Logical "1" Level		VDD -2		Vdd	V	VDD > 5.25V
Brightness Input Current	IB	0		0.75	mA	
Brightness Input Voltage	VB	3		4.3	V	Input Current=750 μ A
Off State Voltage	Vo(off)			11	V	
Output Sink Current						
Segment Off				10	μ A	IB=0 μA
Segment On			3		mA	IB=100 μA
			6		mA	IB=200 μA
Input Clock Frequency	FCLOCK	0		0.5	MHZ	
Output Matching	Io			±20	%	

PART NO.: LTM-8530E	PAGE: 4 of 8
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ELECTRICAL/OPTICAL CHARACTERISTICS AT Ta=25°C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
Average Luminous Intensity	Iv	800	2400		μcd	I _B =0.4mA
Peak Emission Wavelength	λр		630		nm	I _B =0.4mA
Spectral Line Half-Width	Δλ		40		nm	I _B =0.4mA
Dominant Wavelength	λd		621		nm	I _F =20mA
Luminous Intensity Matching Ratio	Iv-m			2:1		I _B =0.4mA

FUNCTIONAL DESCRIPTION

Serial data transfer from the data source to the display driver is accomplished with 2 signals serial data and clock. Using a format of a leading "1" followed by the 35 data bits allow data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is completed, thus providing non multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

Brightness of display is determined by control the output current of LED display. A 1nF capacitor should be connected to brightness control, Pin 7 to prevent possible oscillations. The output current is typically 25 times greater than the current into Pin 7 which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

Figure 1 shows the input data format. A start bit of logical "1" proceed the 35 bits of data. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for master portion of the first register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers won't clear. When power is first applied to the chip, an internal power ON, a reset signal is generated which reset all registers and all latches. The START bit and first clock return the chip on its normal operation. Bit 1 is the first following the start bit and it will appear on the segment A of the digit 1. A logical "1" at the input will turn on the appropriate LED. Figure 2 shows the timing relationship between data, clock, and DATA ENABLE. A max. clock frequency of 0.5 MHz is assumed.

PART NO.: LTM-8530E PAGE: 5 of 8

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FIGURE 1. INTERNAL BLOCK DIAGRAM

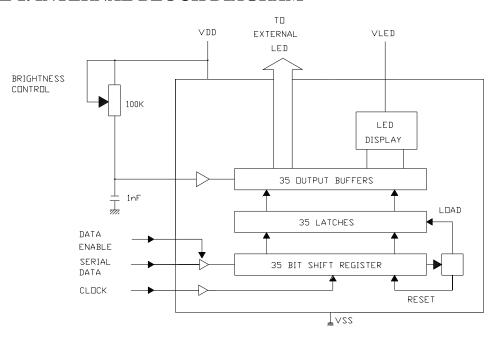


FIGURE 2. INPUT DATA FORMAT

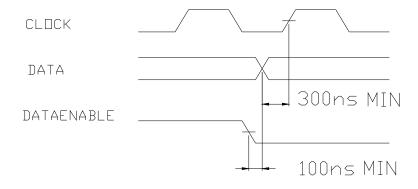
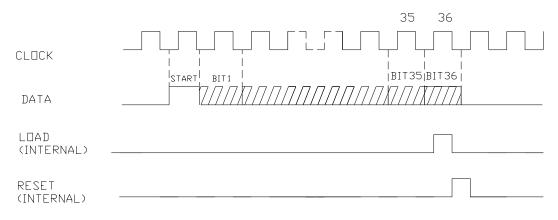


FIGURE 3. TIMING RELATIONSHIP



PART NO.: LTM-8530E PAGE: 6 of 8

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TABLE 1 SERIAL DATA INPUT SEQUENCE

	LTM-8530			
BIT	DIGIT	SEGMENT		
1	1	A		
2	1	В		
3	1	С		
4	1	D		
5	1	Е		
6	1	F		
7	1	G		
8	1	D.P.		
9	2	A		
10	2	В		
11	2	С		
12	2	D		
13	2	Е		
14	2	F		
15	2	G		
16	2	D.P.		
17		PIN 6		
18		PIN 7		
19		PIN 8		
20		PIN 9		
21		PIN 10		
22		PIN 11		
23		PIN 12		
24		PIN 13		
25		NO CONNECTION		
26		NO CONNECTION		
27		NO CONNECTION		
28		NO CONNECTION		
29		NO CONNECTION		
30		NO CONNECTION		
31		NO CONNECTION		
32		NO CONNECTION		
33		NO CONNECTION		
34		NO CONNECTION		

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NOTES: 1. Clean only in water, isopropanol, ethanol, freon TF(or equivalent).

2. Luminous intensity is measured with a light sensor and filter combination that approximates the CIE (Commision Internationale De L'Eclairage)eye-response curve.

PART NO.: LTM-8530E PAGE: 8 of 8